# Substrate and Ground Noise Interactions in Mixed-Signal Circuits

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***Abstract*— The interaction of the substrate with the inductive on-chip ground distribution network is analyzed in this paper. A transistor level approach is presented to illustrate the effects of the substrate on ground noise. The substrate can have a significant effect on ground noise due to the inductance of the ground lines. For a CMOS inverter, the substrate can reduce negative peak ground noise by 49% during the high-to-low output transition. The substrate, however, increases the positive peak ground noise by 72% during the low-to-high output transition. The effect of the substrate should therefore not be neglected if the inductance of the on-chip ground distribution network is non-negligible. Furthermore, conventional triangle or trapezoid type current demand estimations of the nonlinear circuits are shown to be significantly inaccurate if the ground lines exhibit inductive behavior.**

## I. INTRODUCTION

Technology scaling supports high speed and density integrated circuits. As the speed and density of a circuit increase, the average current required to charge the total capacitive load also increases. Due to the parasitic resistance and inductance of the on-chip power distribution network, these fast current changes produce significant voltage fluctuations on the power nodes, affecting overall signal integrity.

Techniques to reduce power noise such as the use of on-chip decoupling capacitors have been developed [1], [2], [3]. Models of a power distribution system and the dependence of power noise on different circuit parameters have also been investigated [4], [5], [6], [7]. These papers, however, do not consider the interaction of the power distribution network with the substrate. If this interaction is not modeled, the power noise analysis can be significantly inaccurate.

Power supply coupling noise is an important source of substrate noise [8], [9]. This source of noise has been analyzed assuming the substrate noise as the primary concern [10], [11]. Coupling of the substrate noise into the power supply and ground rails, however, has not received much attention.

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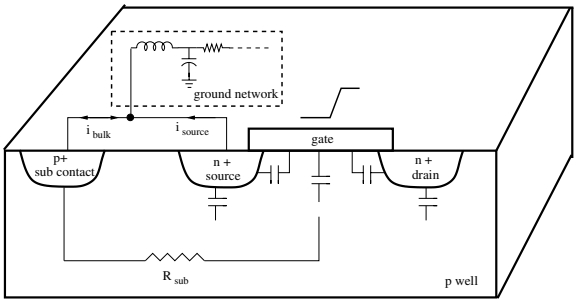


Fig. 1. Interaction of the substrate and on-chip ground distribution network within an NMOS transistor. The current flowing through the ground network is the summation of the source and bulk currents.

In [12], the effect of the substrate on the power noise is analyzed at the IC level. The system is modeled as a linear network, neglecting junction coupling and impact ionization mechanisms. Furthermore, a resistive model is used to characterize the on-chip ground distribution network, neglecting the on-chip inductance. As shown in [13], however, on-chip inductive noise will become more significant with technology scaling.

The interaction of the substrate with an inductive on-chip ground distribution network is the focus of this paper. The contribution of the substrate to the total ground noise is shown to be significant.

The paper is organized as follows. The interaction of the substrate with the ground network is described in Section II. The substrate model, on-chip ground distribution network model, and the superposition methodology are described in Section III. Simulation results illustrating the contribution of the substrate to the total ground noise are presented in Section IV. The paper is concluded in Section V.

## II. BACKGROUND

During the switching activity of the transistor, noise couples into the substrate through the junction capacitances of the transistor. The coupled noise propagates through the substrate, interacting with the ground distribution network through the substrate contact. This interaction is illustrated in Fig. 1. Note that the substrate contact is connected to the ground network. The source and bulk currents therefore flow to the ground network.

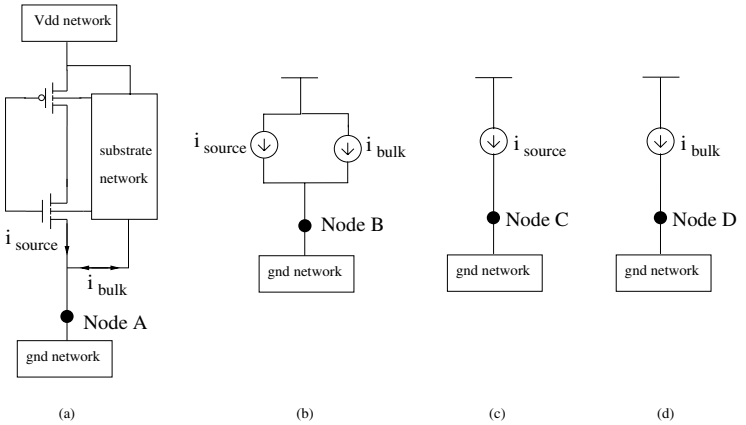


Fig. 2. Illustration of the superposition technique to analyze the effect of the substrate on the on-chip ground noise. The overall ground noise is modeled as a superposition of two noise voltages: source related ground noise and bulk related ground noise: (a) The CMOS inverter including the substrate network and the ground distribution network used to analyze the total ground noise, (b) summation of the PWL approximation of the source current and bulk current which flows through the same ground network, (c) PWL approximation of the source current to estimate the source related ground noise, and (d) PWL approximation of the bulk current to estimate the bulk related ground noise.

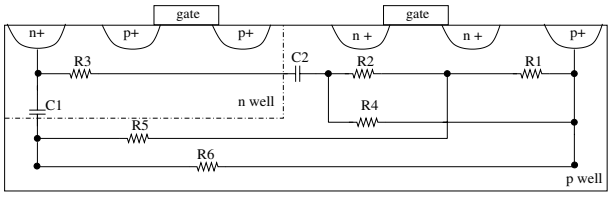


Fig. 3. A bulk-type substrate model of a CMOS structure.

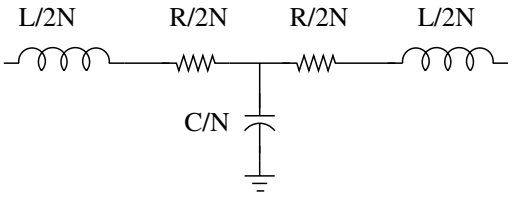


Fig. 4. One stage of a distributed *RLC* interconnect model for an on-chip ground distribution network.

Although the bulk current of the substrate is small as compared to the switching current of the transistor, the *di/dt* levels of the bulk current are sufficient to affect the overall ground noise. Therefore, if the parasitic inductance of the ground network is considered, the effect of the substrate on the ground noise cannot be neglected. Furthermore, the junction capacitances of the transistors, the substrate resistance, and the parasitic impedance of the power supply interconnect form an *RLC* circuit that contributes to the resonance of the power nodes. The effect of the substrate should therefore be considered when analyzing the on-chip power supply noise.

The purpose of this paper is to quantify the effect of the substrate on the ground noise if the ground lines exhibit inductive behavior. A transistor level approach is presented to consider each of the substrate coupling mechanisms. The total on-chip ground noise is modeled as the superposition of two different noise voltages. The first noise voltage is caused by the source current of the transistor, and the second noise voltage is caused by the bulk current of the substrate. The individual contributions of the source and bulk currents to the overall ground noise are summed based on this superposition technique.

As shown in Figs. 1 and 2(a), the total current that flows through the ground network is

$$i(t) = i_{source}(t) + i_{bulk}(t). \quad (1)$$

The bulk current in (1) is usually neglected due to the relatively small magnitude as compared to the source current. This assumption is acceptable if the ground network is modeled as a resistive-only network. If the on-chip inductance is considered, however, the total ground noise is

$$\Delta V = i_{source}(t)R + \frac{di_{source}(t)}{dt}L + i_{bulk}(t)R + \frac{di_{bulk}(t)}{dt}L, \quad (2)$$

where $R$ and $L$ are the parasitic resistance and inductance of the on-chip ground lines, respectively.

Although the absolute magnitude of the bulk current is smaller than the source current, the bulk current significantly affects the total ground noise due to the last term in (2), which represents the rate of change of the bulk current.

The effect of the substrate is quantified in this paper using superposition of the source and bulk related noise voltages. Note that in (2), the first two terms and the last two terms represent, respectively, the source related ground noise and the bulk related ground noise. Transistor level simulation results illustrate that the substrate contributes, on average, 56% of the peak ground noise. The effect of the substrate should therefore be considered for accurate analysis of the ground noise.

## III. Circuit Models and Superposition Technique

A bulk-type (high-ohmic) substrate is assumed due to isolation advantages and applicability to mixed-signal circuits. The substrate model used in the simulations is shown in Fig. 3 for a CMOS inverter. $R_1$ and $R_3$ represent the resistance between the

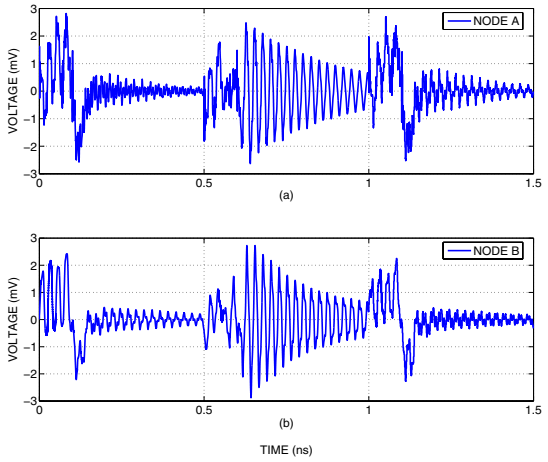


Fig. 5. Comparison of the voltage at Nodes A and B (see Fig. 2) illustrating the accuracy of the current estimations. The maximum error for the peak voltage values is less than 10% within one period.

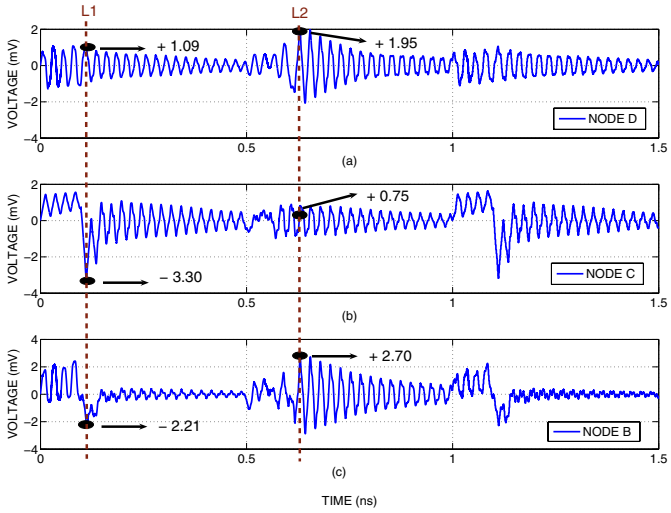


Fig. 6. Comparison of the voltage at Nodes B, C and D, (see Fig. 2). Nodes B, C, and D illustrate, respectively, the total ground noise, source related ground noise, and bulk related ground noise.

bulk nodes and the substrate contacts, and $R_2$ and $R_5$ represent the resistance between the N-Well and the bulk node of the NMOS transistor. $R_4$ and $R_6$ represent the resistance between the N-Well and the substrate contact for the ground connection. $C_1$ and $C_2$ represent the N-Well capacitance.

An impedance model composed of ten distributed *LRCRL* (*T* cell) [14] cells is used to model the on-chip ground distribution network, as shown in Fig. 4. The total resistance, inductance, and capacitance of the interconnect are assumed in this analysis to be 1 Ω, 200 pH, and 200 fF, respectively.

Simulations are based on a 0.18 $\mu$m CMOS technology using SPICE. A BSIM3v3 model is used to characterize the transistors since this model includes the effects of capacitive coupling and impact ionization as sources of substrate noise [15]. The simulation model illustrating the superposition methodology is shown in Fig. 2. A CMOS inverter is analyzed in Fig. 2(a) with the substrate and ground distribution network models. The voltage at Node A represents the on-chip ground noise. The source and bulk currents are individually approximated using piecewise linear (PWL) current sources, as shown in Fig. 2(b). The voltage at Nodes A and B is compared in order to evaluate the accuracy of these estimates of the current demand. If the voltage at Nodes A and B is sufficiently similar, the voltage at Nodes C and D is analyzed. Note that the voltage at Nodes C and D represents, respectively, the source related ground noise and bulk related ground noise. The superposition of the source and bulk currents therefore supports the analysis of the individual contributions of the source and substrate to the total ground noise.

## IV. Simulation Results

PWL current estimation results are provided in Section IV-A. The results illustrating the effect of the substrate on the ground noise are presented in Section IV-B.

### A. PWL Current Estimation

Estimating the current demand of the nonlinear circuits using linear current sources is a common approach to analyze power supply noise. Nonlinear circuits are replaced by these linear current sources in order to reduce the simulation time of the system [4]. If the inductance of the power and ground lines is considered, however, estimating the current demand becomes a difficult process. Conventional triangle or trapezoidal type current demand approximations [16] do not provide the necessary accuracy due to the inductance. In this analysis, estimates of the source and bulk currents are obtained using an iterative process. The number of time instances included in the PWL approximations is increased in each iteration until sufficient accuracy is achieved. The different rates of change in the current waveform should therefore be considered if the ground network exhibits inductive behavior.

The voltage at Nodes A and B as shown in Figs. 2(a) and 2(d) is compared in Fig. 5 to evaluate the accuracy of the approximations. The amount of error for the peak voltage values is less than 10% at any time within one period. This model therefore provides sufficient accuracy to individually analyze the source and bulk current contributions. Note that more than 50% error is obtained if a conventional triangle type approximation is used.

### B. Effect of the Substrate on Ground Noise

In order to quantify the effect of the substrate on ground noise, the voltage at Nodes B, C, and D is compared in the time domain in Fig. 6. The voltage at Nodes C and D represents, respectively, the ground noise due to the source and bulk currents. The voltage at Node B represents the total ground noise. The summation of the voltage waveforms shown in Figs. 6(a) and 6(b) results in the waveform shown in Fig. 6(c). Two different time instances are marked by the dashed vertical lines, L1 and L2, to illustrate the effect of the substrate on the ground noise. At L1, the total ground noise is -2.21 mV. At this

TABLE I

ABSOLUTE (ABS) AND RELATIVE (REL) CONTRIBUTIONS OF THE SOURCE AND BULK CURRENTS TO THE GROUND NOISE VOLTAGE FOR THREE GATES: INVERTER (INV), NAND, AND NOR. THE NEGATIVE AND POSITIVE PEAK NOISE IS LISTED FOR BOTH THE HIGH-TO-LOW AND LOW-TO-HIGH OUTPUT TRANSITIONS.

| GND Noise | High-to-low (output) | | | Low-to-high (output) | | |
|---|---|---|---|---|---|---|
| (mV) | INV | NAND | NOR | INV | NAND | NOR |
| Negative peak noise | -2.21 | -4.44 | -2.16 | -2.86 | -3.48 | -2.77 |
| Bulk contribution: abs (rel) | +1.09 (-49.3%) | +0.98 (-22%) | +0.69 (-31.9%) | -2.07 (72.4%) | -1.39 (39.9%) | -2.18 (78.7%) |
| Source contribution: abs (rel) | -3.30 (149.3%) | -5.42 (122%) | -2.85 (131.9%) | -0.79 (27.6%) | -2.09 (60.1%) | -0.59 (21.3%) |
| | | | | | | |
| Positive peak noise | +2.40 | +3.73 | +2.97 | +2.70 | +2.57 | +2.94 |
| Bulk contribution: abs (rel) | +1.0 (41.6%) | +1.95 (52.3%) | +1.61 (54.2%) | +1.95 (72.2%) | +2.46 (95.7%) | +1.8 (61.2%) |
| Source contribution: abs (rel) | +1.40 (58.4%) | +1.78 (47.7%) | +1.36 (45.8%) | +0.75 (27.8%) | +0.11 (4.3%) | +1.14 (38.8%) |

time, the noise voltage induced by the source current is -3.30 mV and the noise voltage induced by the bulk current is +1.09 mV. The substrate can therefore be used to lower the total ground noise since the source and bulk currents are temporally out-of-phase. At L2, the total ground noise is +2.70 mV, the bulk related ground noise is +1.95 mV, and the source related ground noise is +0.75 mV. At this time, therefore, the substrate degrades the total ground noise by 72% since the bulk current is in-phase with the source current. Furthermore, the resonance at Node B is primarily caused by the bulk current rather than the source current.

The proposed methodology can also be applied to a NAND and NOR gate in order to generalize the results, as listed in Table I. The positive and negative peak noise is listed for the high-to-low and low-to-high output transitions. The effect of the substrate and source are individually listed for each gate. The contribution of the substrate varies between 22% and 95%, exhibiting an average contribution to the peak ground noise voltage of 56%.

## V. CONCLUSIONS

The effect of the substrate on the ground noise is analyzed for an inverter, NAND, and NOR gate. The substrate is modeled as a resistive network and the on-chip ground network is modeled as a distributed *LRCRL* impedance. The total ground noise is considered as the superposition of two noise voltages: the source related ground noise and bulk related ground noise. It is shown that the bulk current significantly affects the ground noise due to the inductance of the ground network since the rate of change of the bulk current is not negligible. Specifically, if the source and bulk currents are in-phase, the substrate degrades the ground noise. If the source and bulk currents are out-of-phase, the substrate improves the ground noise. Based on this analysis, the substrate contributes, on average, 56% of the peak ground noise. Two primary conclusions therefore can be drawn if the ground lines exhibit inductive behavior: (1) the substrate should not be neglected in an analysis and model of the ground noise, and (2) triangle or trapezoid type current demand estimation of the nonlinear circuits is not sufficiently accurate since these models do not capture different rates of change of the current waveforms.

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