Pseudo-Random Clocking to Enhance Signal Integrity

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***Abstract*— A methodology is proposed to reduce power/ground and substrate coupling noise by randomizing the clock signal. A pseudo-random number generation algorithm is used to produce a pseudo-random clock. A probability adjustment technique is introduced to compensate for the speed loss, permitting the average frequency of the pseudo-random clock to be determined. The proposed method achieves more than 24 dB attenuation in noise at the center frequency at a cost of less than 4% reduction in speed.**

I. Introduction

Substrate coupling and power/ground noise are two important sources of noise in mixed-signal circuits. Three approaches have been proposed to manage substrate coupling and power/ground noise; 1) develop design strategies to lower the propagated noise, 2) reduce the noise sensitivity of the circuit, and 3) reduce the magnitude of the noise at the input to lower the noise at the output [1]. The third technique is the primary focus of this paper.

The supply current is a function of the clock frequency. Since the power of the clock signal is concentrated in a narrow bandwidth around the clock frequency, noise spikes occur at the primary and harmonics of the clock frequency [2], [3]. These spectral noise spikes can cause the analog portion of a circuit to malfunction when the amplitude of the analog signal becomes comparable to the amplitude of the noise signal.

Several techniques exist to mitigate the effect of the discrete noise spikes that occur at a sensitive node. Spreading the switching events of the clock signal in the time domain to reduce the amplitude of the spectral spike at the clock frequency has been proposed [1]. Clock skew optimization to partition the clock into several clock domains is another method to reduce the amplitude of the spectral noise spikes [4]–[6]. Spreading the frequency spectrum of the clock signal can also reduce electro-magnetic interference (EMI) [7], [8]. Spread spectrum clock generation was first proposed in [7] to reduce the radiated emissions within a circuit. A spread spectrum clock generation method modulates the clock signal to spread the spectrum of the clock signal around the clock frequency. Spreading the clock frequency spectrum distributes the energy around the center clock frequency, reducing the amplitude of the noise spikes. An overview of various spread spectrum clock generation techniques can be found in [9].

A clock randomization methodology to lower the maximum amplitude of the noise signal at integer multiples of the clock frequency was recently proposed in [10]. The power spectral density (PSD) of the clock signal is spread to ensure that the average frequency of the pseudo-random clock is between the original clock frequency and a lower frequency which depends upon the randomization process. In [10], 22 dB attenuation in the PSD of the clock signal is achieved with a 25% loss in speed. The method proposed in this paper produces a 24 dB attenuation with less than 4% degradation in speed. A probability adjustment unit is introduced to compensate for the speed loss. The *randomization degree* of the clock signal is adjusted through this unit, permitting tradeoffs between the noise and average speed.

The paper is organized as follows. The proposed pseudo-random clock generation methodology and some related issues are discussed in section II. In section III, simulation results for a small aggressor circuit are presented. Finally, some conclusions are offered in section IV.

II. Proposed Pseudo-Random Clock Methodology

In the proposed system, a linear feedback shift register (LFSR) produces a pseudo-random number sequence. The pseudo-random clock generator takes a pseudo-random number sequence tuned to a probability adjustment block operating at a periodic clock signal to produce a pseudo-random clock. This pseudo-random clock drives the digital circuitry rather than a standard periodic clock signal. The synchronizer unit has three inputs, a pseudo-random clock, a periodic clock, and the data synchronized to the pseudo-random clock. The synchronizer unit synchronizes the data with the periodic clock. The proposed system is illustrated in Fig. 1. The pseudo-random clock generation process is described in section II-A. In section II-B, the effect of the length of the LFSR on the pseudo-random clock is discussed. The probability adjustment unit is discussed in section II-C.

A. Pseudo-random clock generation process

The process of generating a pseudo-random clock from a pseudo-random number sequence is discussed in this section. An LFSR generates a pseudo-random number sequence. The length of the pseudo-random number sequence is adjusted by changing the size of the LFSR. The LFSR output is an input to the pseudo-random clock generator. The pseudo-random

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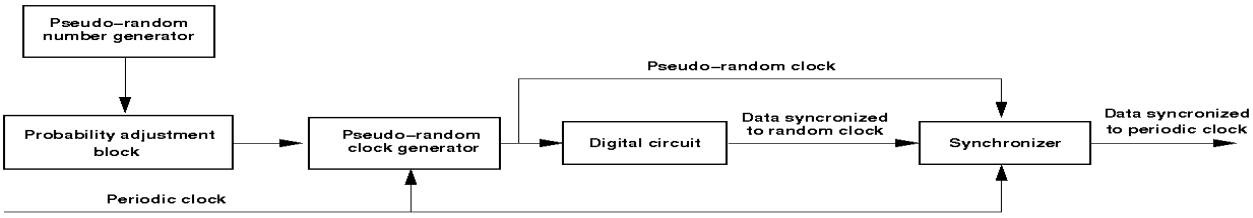

Fig. 1. Proposed pseudo-random clock generator and synchronizer circuit.

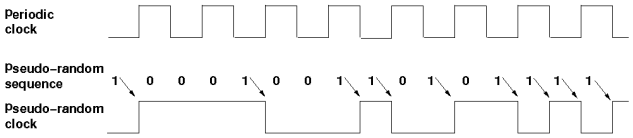

Fig. 2. Timing diagram for pseudo-random clock generation. When the pseudo-random number is "1," the pseudo-random clock is the toggled version of the pseudo-random clock signal in the previous cycle. When the pseudo-random number is "0," the pseudo-random clock is the same as during the previous cycle.

clock generator produces a pseudo-random clock signal, as follows. When the input to the pseudo-random clock generator is "1," the output of the pseudo-random clock generator is the toggled version of the previous output of the pseudo-random clock generator. When the input to the pseudo-random clock generator is "0," the output of the pseudo-random clock generator is the same as the output of the pseudo-random clock generator in the previous cycle. The timing diagram is shown in Fig. 2. The LFSR output has approximately an equal number of "1"s and "0"s. When the LFSR length is n, the output is a sequence of length $2^n - 1$ consisting of 2^{n-1} number of "1"s and $2^{n-1} - 1$ number of "0"s. The average frequency of the pseudo-random clock is therefore half of the frequency of the periodic clock, *i.e.*, a 50% loss in speed is incurred when the probability adjustment unit is not connected. The probability adjustment unit increases the average frequency of the pseudo-random clock by increasing the frequency of "1"s in the pseudo-random number sequence. The average frequency of the pseudo-random clock can be increased by properly tuning the probability adjustment unit connected to the output of the LFSR.

B. Effect of LFSR length on the PSD of the noise

In this section, the reduction in peak power of the clock source is described for different LFSR unit lengths when the probability adjustment unit is not connected. The repeating cycle of the pseudo-random number sequence produced by the LFSR depends upon the LFSR length. With increasing LFSR length, the length of the repeating cycle is also increased. When the LFSR length is excessively long, the length of the repeating cycle is also excessively long. The pseudo-random number sequence thereby converges to a random number sequence. The reduction in the amplitude of the discrete noise spikes is greatest when the pseudo-random number sequence converges to a random number sequence.

The attenuation in the PSD of a random clock relative to the periodic clock is shown in Fig. 3. The peak power

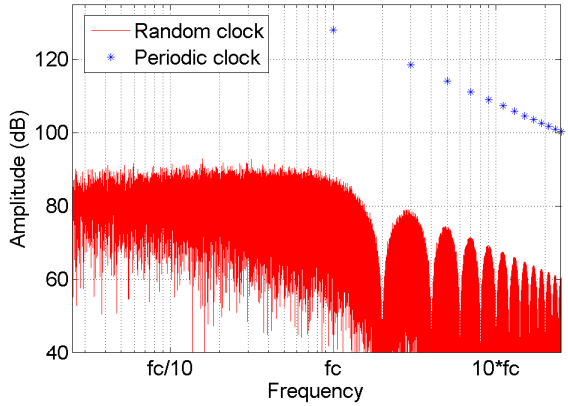

Fig. 3. Power spectral density of the periodic clock and random clock. The amplitude of the spectral component of the random clock is 38 dB lower than the spectral component of the periodic clock signal at the clock frequency.

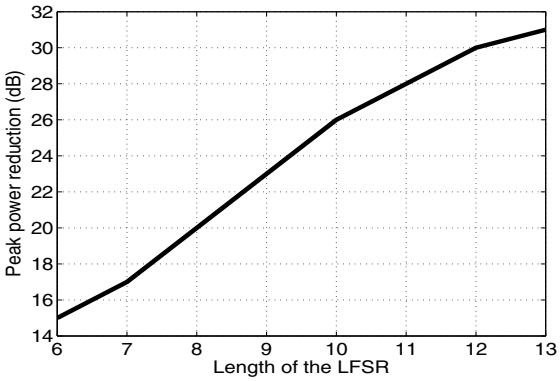

Fig. 4. Reduction in the peak power at the discrete noise spikes of the pseudo-random clock relative to the periodic clock. The reduction in the peak power spectral component increases when the LFSR length is increased.

reduction in the power spectral component is 38 dB at the periodic clock frequency. The attenuation of the peak power component depends both on the length of the clock sample and the clock frequency. The LFSR length is maintained constant. The simulation results shown in this paper are generated with the same length clock sample and clock frequency.

The attenuation of the peak power spectral component of the pseudo-random clock versus the length of the LFSR is shown in Fig. 4. When the LFSR length is increased, the peak power attenuation at the clock frequency converges to the peak power attenuation when a random sequence is applied. Even with an LFSR length of 13, a reasonable reduction of about

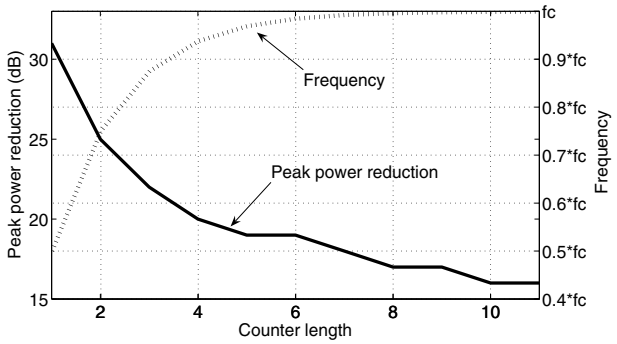

Fig. 5. Peak power reduction and frequency vs. counter length. Note that a tradeoff exists between the speed and the peak power reduction.

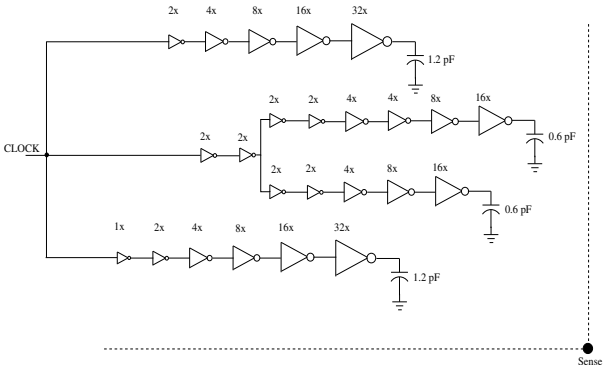

Fig. 6. A sample noise generating circuit. The output noise is measured at the sense node which is 25 μm from the closest contact.

31 dB in peak PSD can be achieved.

C. Effect of probability adjustment unit on the PSD of the noise and average clock frequency

In this section, the effect of the probability adjustment unit connected to the output of the LFSR unit is discussed. The reduction of the peak power spectral component is investigated for an LFSR length of 13. In the previous section, when no probability adjustment unit is connected to the output of the LFSR, the peak attenuation of the power spectral component is 31 dB. The frequency of the random clock however is half of the periodic clock frequency. By connecting a probability adjustment unit at the end of the LFSR, the reduction in speed can be compensated.

The probability adjustment unit produces a second pseudo-random number sequence which spreads the peak power component of the clock signal at the clock frequency. The probability adjustment unit also controls the spreading process to ensure that the speed of the pseudo-random clock is not significantly degraded. The probability adjustment unit includes a counter which counts the number of "0"s at the output of the LFSR. The probability adjustment unit operates as follows. When the counter length is n, the probability adjustment unit takes the LFSR output as an input and produces a "0" at the output for every occurrence of the n^{th} zero input. Otherwise, the output of the probability adjustment unit is "1."

The reduction of the peak power spectral component of the PSD of the random clock versus the counter length of the probability adjustment unit for an LFSR length of 13 is shown in Fig. 5. Note that reasonable attenuation of the peak power can be achieved without a significant reduction in speed, *i.e.*, for a counter length of 5, the frequency of the pseudo-random clock is 31/32 of the frequency of the periodic clock. The reduction in speed is less than 4% of the periodic clock. The frequency of the pseudo-random clock approaches the frequency of the periodic clock by increasing the counter length in the probability adjustment unit. By applying the probability adjustment unit at the end of the LFSR unit, a pseudo-random clock with any desired average clock frequency can be obtained. The relationship between the counter length in the probability adjustment unit and the

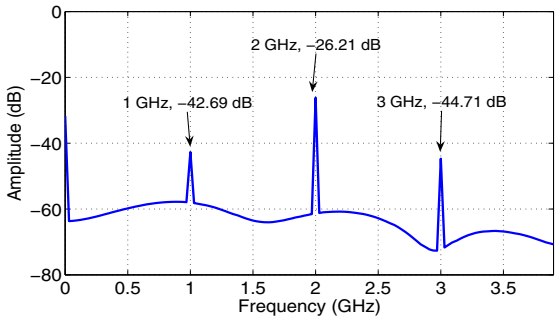

Fig. 7. Power spectral density of the output noise measured at the sense node with a periodic clock input.

frequency of the pseudo-random clock is

$$f_{PRC} = f_C * (1 - (1/2^n)), \tag{1}$$

where f_{PRC} is the average frequency of the pseudo-random clock, f_C is the frequency of the periodic clock, and n is the counter length in the probability adjustment unit.

III. Simulations Results

Cascaded buffers are extensively used in clock distribution networks [11]. A sample noise generating network with four chains of cascaded buffers, as shown in Fig. 6, is used to exemplify this technique. The circuit is designed in a 90 nm double-well CMOS technology with a bulk type (non-epi) substrate. A 1 GHz clock signal with 100 ps rise and fall times is assumed as the periodic clock signal and the pseudo-random clock signal. The layout and substrate impedances of the three circuits are extracted using Assura RCX [12] and SubstrateStorm [12], respectively, and the netlist is simulated using Spectre [12]. The substrate noise voltage is measured at the sense node, 25 μm from the closest contact.

The PSD of the noise voltage at the sense node when a periodic clock signal is applied at the input is shown in Fig. 7. Noise spikes exist at the even and odd harmonics of the periodic clock frequency. The PSD of a pseudo-random clock, constructed using an LFSR length of 13 without any probability adjustment unit (the counter length is one), is

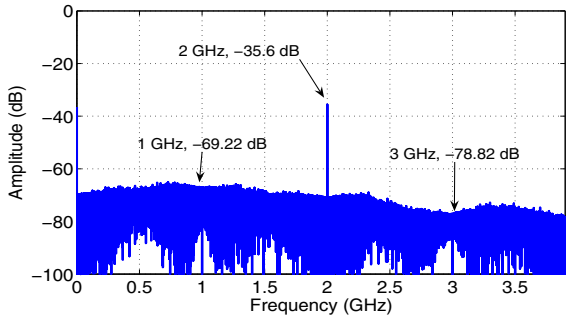

Fig. 8. Power spectral density of the output noise measured at the sense node with a pseudo-random clock input. The LFSR length is 13 and the counter length is 1.

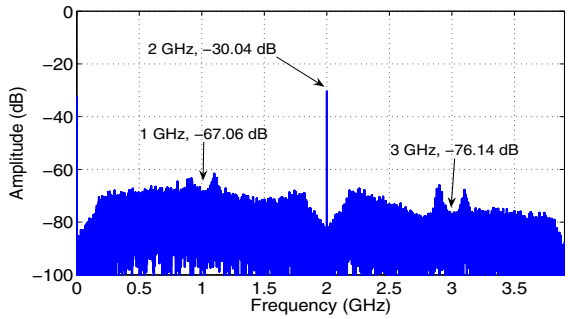

Fig. 9. Power spectral density of the output noise measured at the sense node with a pseudo-random clock input. The LFSR length is 13 and the counter length is 5.

shown in Fig. 8. The reduction in peak power at the periodic clock frequency and first odd harmonic is 26 dB and 34 dB, respectively. The reduction in the first even harmonic is 9 dB. With a longer counter length in the probability adjustment unit, the average speed of the circuit increases. The reduction in the peak power spectral component with an LFSR length of 13 and counter length of five is shown in Fig. 9. The attenuation at the first three harmonics of the clock frequency for five different counter lengths are listed in Table 1.

Simulation results obtained from MATLAB are different from the results obtained from Spectre. There are two primary reasons: 1) The reduction in the peak power from the MATLAB simulations is obtained for the PSD of the input clock signal since the output voltage noise is not known. The reduction in peak power however is obtained for the PSD of the output noise voltage in the Spectre simulations, 2) The simulation for counter lengths of one to five is performed for the same amount of time. For a counter length equal to five, the simulation time produces one repeating sequence while exhibiting five repeating sequences for a counter length of one. This difference in the number of repeating sequences therefore produces different simulation results as compared to MATLAB.

IV. Conclusions

The power concentrated at the clock frequency and related harmonics can cause signal integrity problems. A method to spread the frequency spectrum of the clock signal to distribute the peak spectral power at the clock frequency and related harmonics with a speed loss of less than 4% is proposed. The pseudo-random sequence is changed with a probability adjustment unit to significantly reduce the spectral noise spikes without a significant loss in speed. A 24 dB reduction in the spectral noise component at the periodic clock frequency is achieved with less than 4% degradation in speed. A tradeoff therefore exists between the noise and operating frequency, as illustrated in Fig. 5.

TABLE I

PEAK POWER REDUCTION VS COUNTER LENGTH

	Peak power reduction (dB)		
Counter length	1 GHz	2 GHz	3 GHz
1	26.5	9.4	34.1
2	26.1	7.9	33.5
3	25.3	5.9	33
4	24.8	4.5	32
5	24.4	3.8	31.4

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