A Higher-Order Mismatch-Shaping Method for Multi-Bit Sigma-Delta Modulators

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***Abstract*—Mismatch-shaping Dynamic Element Matching (DEM) methods are extensively used in multi-bit Sigma-Delta Modulators (SDM) to reduce the effects of element mismatches. To date, only first and second-order mismatch-shaping DEM techniques have been reported in the literature. In this paper, a higher-order mismatch-shaping DEM method is reported, which is an extension of the *known* vector-feedback mismatch-shaping technique. Example simulation results are presented for third-order and fourth-order mismatch-shaping DEMs.**

I. INTRODUCTION

The major flaw of multi-bit Sigma-Delta Analog-to-Digital Converters (ADC) is that the internal Digital-to-Analog Converter (DAC) in the feedback path should have the same linearity and accuracy requirements of the overall data converter. Unfortunately, due to inevitable mismatches in the circuit components, multi-bit DACs with high linearity performance (typically, 16 to 20 bit) cannot easily be manufactured. A slight mismatch among the unit elements of a multi-bit DAC raises the noise floor and produces non-linearity, which in turn cause harmonic distortions and spurious tones in the output spectrum. Thus, the Signal-to-Noise Ratio (SNR) performance of a multi-bit SDM ADC is significantly dependent on the degree of matching among the unit elements inside the DAC, making the circuit vulnerable to the manufacturing imperfections.

In order to overcome the undesirable effects of unit element mismatches, mismatch-shaping Dynamic Element Matching (DEM) techniques have been developed [1]-[3]. These techniques manipulate the usage of elements of a multi-bit DAC in such a way that the error caused by mismatches is being filtered and spectrally shaped. Individual Level Averaging (ILA) [1] and Data-Weighted Averaging (DWA) [2] are two well-known techniques reported in the literature that can provide first-order mismatch-shaping DEMs. Second-order mismatch-shaping DEMs have also been reported in the literature, among which the Vector-Feedback mismatch-shaping (VFMS) [3], [4] and Tree-Structure mismatch-shaping (TSMS) [5], [6] algorithms are the ones that are most commonly used.

Generally speaking, in a higher-order multi-bit SDM, the mismatch-shaping algorithm must have the same order as the SDM itself to fully preserve the higher-order noise shaping properties. For instance, a third-order and a fourth-order SDM may need a third-order and a fourth-order mismatch-shaping algortihm, respectively. Otherwise, the noise shaping properties that can be achieved from a higher-order SDM may only be limited to the order of the DEM. Theoretically, both the VFMS and TSMS can achieve any order of filtering. However, due to practical reasons, the design of third or higher-order DEMs has not been reported so far. The TSMS is limited by its complex logic circuit. One needs to find an appropriate higher-order switching-sequence generator for successfully extending the TSMS to third or higher-order cases. The VFMS is constrained by the stability of its filters, which can cause unstable operation for orders of greater than two.

This paper attempts to extend the VFMS algorithm to higher-order cases by employing Infinite Impulse Response (IIR) filters with specific structural properties. The organization of the rest of the paper is as follows. Section II describes the architecture of the proposed higher-order VFMS. Simulation results are shown in Section III followed by a conclusion in Section IV.

II. HIGHER-ORDER VECTOR-FEEDBACK MISMATCH SHAPING

As shown in Fig. 1, an M-level mismatch-shaping DAC consist of a digital encoder, a bank of M-1 one-bit unit-element DACs, and a summation block. The main function of the DAC is to receive a digital signal, x[n], from the M-level quantizer inside the SDM and generate an analog equivalent signal y[n] that will be fed back around the loop of the SDM. The digital signal, x[n], generated by the M-level quantizer inside the SDM is a sequence of nonnegative integers less than or equal to M-1. At each sample time of n, the digital encoder in Fig. 1 receives x[n] as its input signal and generates a vector of one-bit output sequences, $x_i[n]$ $\{i=1,2,\ldots,M-1\}$, which control the unit-element DACs. Each control sequence, $x_i[n]$, generated in the encoder, has a value of "logic one" or "logic

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zero", which turns the corresponding unit-element DAC "on" or "off", respectively. According to the equivalence principle, the summation of M-1 one-bit signals, $x_i[n]$ {i=1,2,…,M-1}, generated by the digital encoder should equal to x[n]. Each one-bit output of the digital encoder is converted into analog domain separately by a one-bit unit-element DAC implemented either using a unit current source or a unit switched-capacitor. The outputs of the M-1 unit-element DACs are summed together to produce an analog signal, y[n], which is representative of the original digital signal x[n].

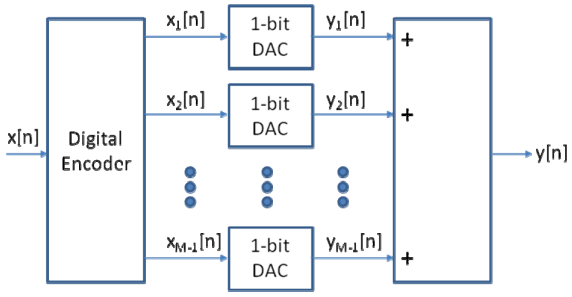


Figure 1. General mismatch-shaping DEM DAC

In a mismatch-shaping DEM, the digital encoder selects its outputs in such a way that the errors produced by mismatches among the unit-element DACs are being spectrally shaped. The spectral shaping of the mismatch errors is achieved by pushing as much mismatch error power to higher frequency locations as possible. Similarly to the quantization noise shaping, the mismatch error power can be reduced within the SDM signal bandwidth by filtering the mismatch errors with a high-pass filter. However, as opposed to the quantization noise shaping, high-pass filtering of the mismatch errors in a DEM is accomplished by appropriately selecting the usage of the unit-elements from a collection of possible sets, which arise from the fact that a given analog output level is dependent on how many, and not which, unit-element DACs are used.

As illustrated in Fig. 2, the proposed digital encoder in this paper resembles to the encoder in the VFMS architecture [3]. It includes a Vector Quantizer (VQ) and a bank of M-1 "SDM-like" IIR filters.

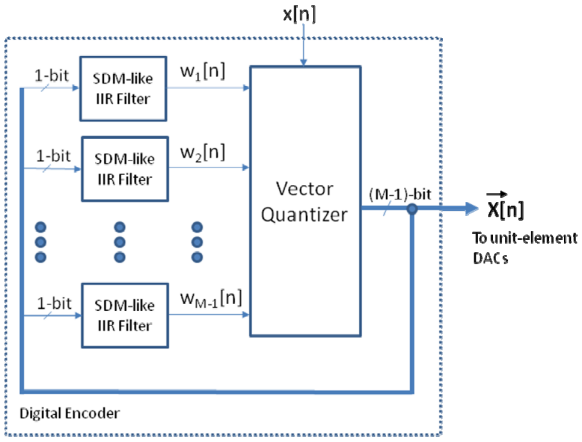


Figure 2. Block diagram of the digital encoder

Each SDM-like IIR filter in Fig. 2 is a digital SDM formed out of Cascade of Resonator with Distributed Feedback (CRFB) topology. These SDMs in the digital encoder do not have quantizers, and hence the name "SDM-like" IIR filter is adopted. Instead, the VQ acts as a common quantizer. The VQ determines the x[n] largest elements of its input vector, $w_i[n]$ {i=1,2,…,M-1}, then sets the associated elements of its output vector, $x_i[n]$ {i=1,2,…,M-1}, to "one" and the rest to "zero". The operation of the VQ in this paper is the same as the conventional VFMS architecture.

The main difference between the conventional VFMS in [3] and this paper is that the mismatch-shaping loops are built out of different SDM topologies. In [3], each of the SDM-like filters is built using an error-feedback topology. It has been observed by the authors via simulations that the error-feedback topology results in an unstable DEM, when the order of the mismatch-shaping loops are three or higher. The stability problem is the main reason why the conventional VFMS algorithm has been limited to only first and second-order filtering. This paper attempts to overcome this problem by using the CRFB topology for the mismatch-shaping loops.

Examples structures of the SDM-like IIR filters used in the digital encoder of Fig. 2 are shown in Fig. 3(a) and (b), for third-order and fourth-order cases, respectively. For the fourth-order case, the input signal to the filters is zero. For the third-order case, however, there is a common input to each filter, denoted as f[n]. In order to stabilize the third-order VFMS DEM, the outputs of the first integrators from each SDM-like filter, $t_i[n]$, are extracted and processed by a "smallest element selector" block, which compares all $t_i[n]$'s and outputs the signal $f[n] = -\min\{t_i[n]\}$ for {i=1,2,…,M-1}. The signal f[n] is fed to the IIR filters as a common input signal to eliminate the indefinite growth of the output of the integrators.

It should also be noted that the authors have tried the Cascade of Integrators with Distributed Feedback (CIFB) topology as well to implement the IIR filters. Unfortunately, it was observed that the stabilization of the overall VFMS DEM is compromised in this case. Therefore, the results reported in this paper are based on the SDM-like IIR filters with CRFB topology only.

III. Simulation Results

In this section, behavioral simulation results for third-order and fourth-order SDMs that employ third-order and fourth-order VFMS will be shown and compared to previously published DEM methods. The main SDMs are designed using the CIFB topology, whereas the SDM-like IIR filters in VFMS DEM employ CRFB topology.

Both two-bit and three-bit quantization is investigated to assess the effectiveness and usefulness of the proposed higher-order VFMS DEM. A 1% artificial mismatch is introduced among the unit-elements of each multi-bit DAC. In all reported simulations in this section, an input signal of 1250Hz with a -3dBFS (dB with respect to Full Scale) amplitude is applied to all SDMs. The oversampling (OSR) ratio is set to OSR=64 and the sampling rate of each SDM is designated as fs=2.56MHz resulting in a 20KHz input signal bandwidth.

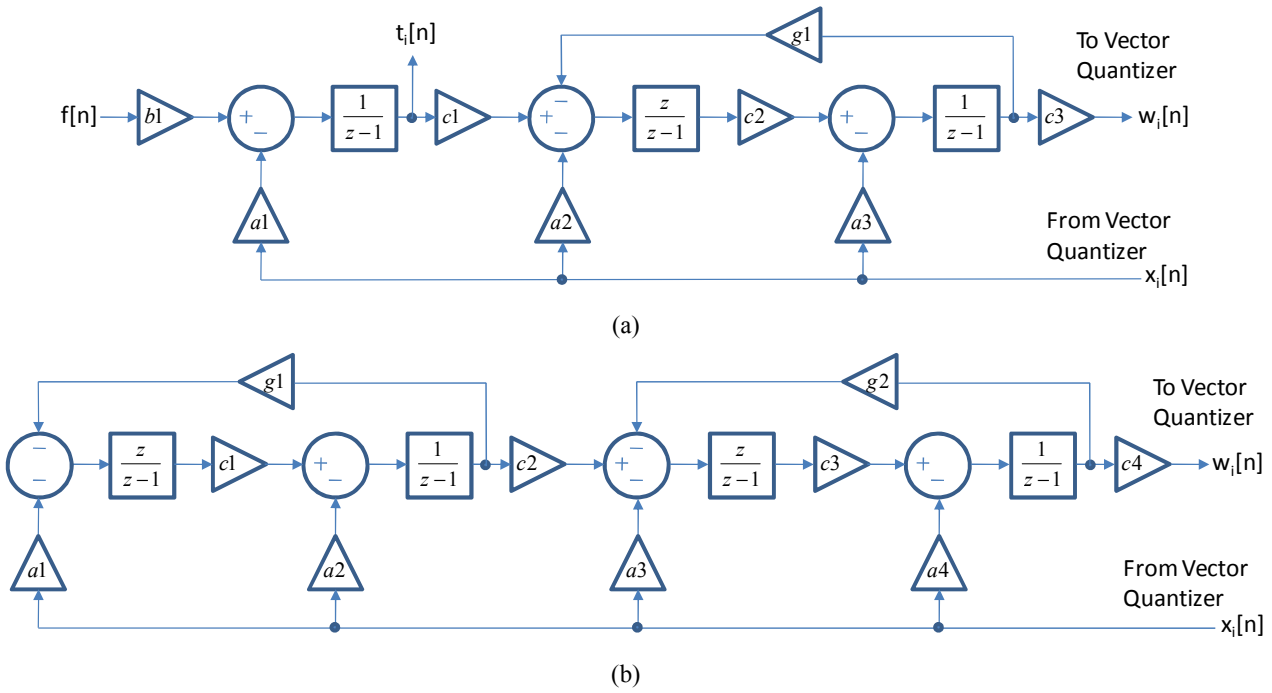


Figure 3. SDM-like IIR filters used in the digital encoder of Fig. 2; (a) third-order, (b) fourth-order

The Noise Transfer function (NTF) for the SDM-like IIR filters is designed is such a way that their maximum NTF gain (H_{inf}) is set to 1.5 and 1.4 for third-order and fourth-order cases, respectively. The SNR values obtained from different mismatch-shaping DEM algorithms are summarized in Table I in the case of 1% mismatch error. Specifically, DWA [2], first-order and second-order VFMS [3] (denoted as VFMS1 and VFMS2), first-order and second-order TSMS [6] (denoted as TSMS1 and TSMS2), and the proposed third-order and fourth-order VFMS (denoted as VFMS3 and VFMS4) are simulated and compared.

Example power spectral density (PSD) plots for the three-bit third-order SDM are shown in Fig. 4(a), (b), and (c) for the ideal DAC, second-order VFMS [3], and the third-order VFMS reported in this paper, respectively. In the ideal case, the SDM achieves 122dB SNR. Under a 1% mismatch condition, the second-order VFMS provides an SNR 104dB, whereas the third-order VFMS results in 122dB preserving the original noise shaping of the SDM despite the existence of the mismatch errors. Note that the plots in Fig, 4(b) and 4(c) have DC offsets, as expected. The offset and gain errors in a non-ideal multi-bit DAC are inevitable and there is no DEM algorithm that can correct these errors.

PSD plots for the two-bit fourth-order SDM are illustrated in Fig. 5(a) and (b) for the ideal DAC and fourth-order VFMS with 1% mismatch error. As can be seen in Fig. 5, the fourth-order VFMS produce almost the same noise shaping as the ideal DAC.

TABLE I. SNR VALUES (IN DB)

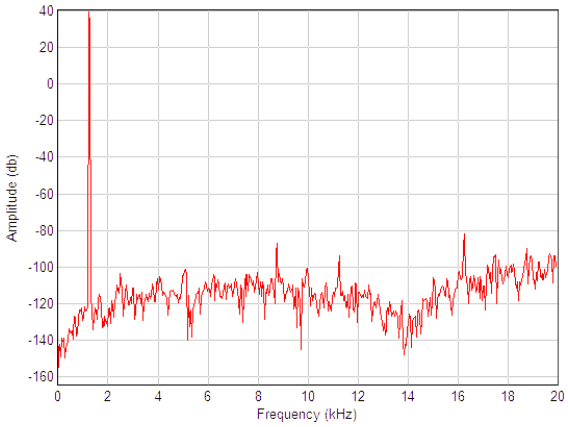
	SDM order	3	3	4	4
	# of bits	2	3	2	3
DEM Methods	Ideal DAC	109	122	127	155
	No DEM	66	62	65	62
	DWA	101	98	103	97
	VFMS1	101	94	103	97
	TSMS1	103	94	105	93
	VFMS2	100	104	105	102
	TSMS2	97	97	105	102
	VFMS3	110	122	124	122
	VFMS4	107	121	126	124

All SNR values are in dB

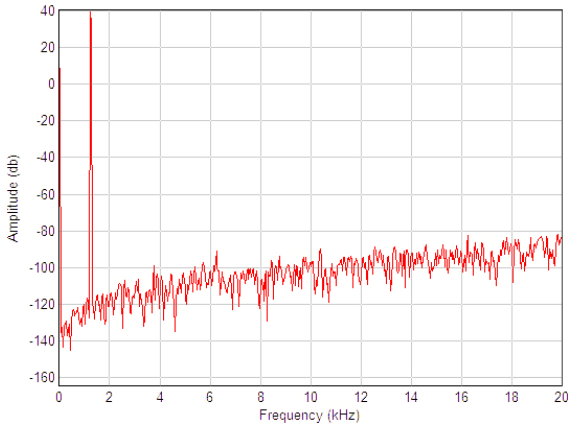
IV. CONCLUSION

In this paper, vector-feedback mismatch-shaping DEM technique is extended to higher-order case. The proposed technique utilizes a bank of SDM-like IIR filters in the digital encoder. Behavioral simulation results are presented for third-order and fourth-order SDMs employing third-order and

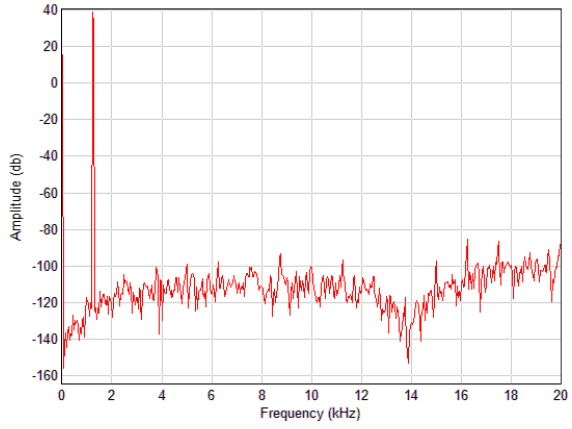
fourth-order VFMS. The simulation results show that higher-order VFMS can provide between 10 to 20dB improvement over the existing second-order DEMs, depending on the SDM order and number of bits in the quantizer.



(a)

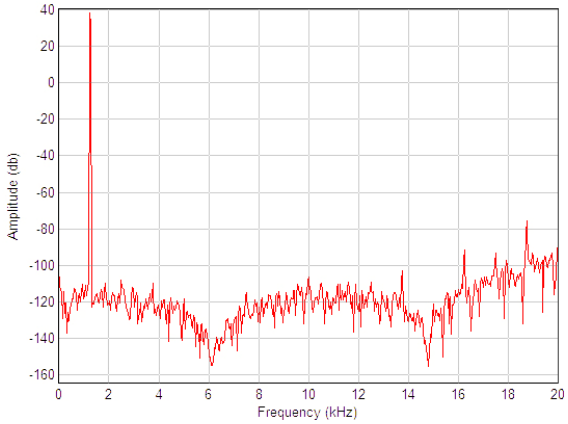


(b)

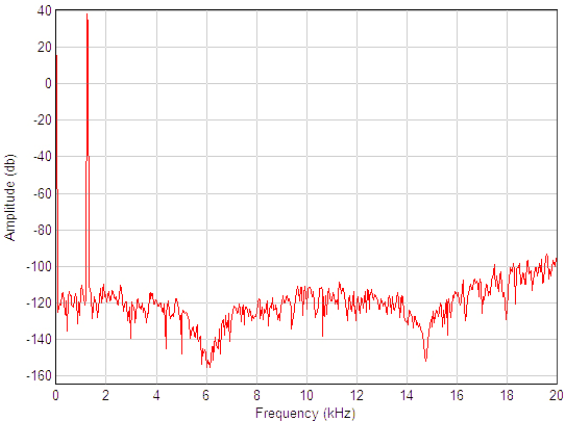


(c)

Figure 4. PSD plots for the three-bit third-order SDM; (a) with ideal DAC, (b) with VFMS2, and (c) with VFMS3



(a)



(b)

Figure 5. PSD plots for the two-bit fourth-order SDM; (a) with ideal DAC, and (b) with VFMS4

REFERENCES

[1] F. Chen and B. H. Leung, "A High Resolution Multi-bit Sigma-delta Modulator with Individual Level Averaging," IEEE Journal of Solid-State Circuits, vol. 30, no. 4, pp. 453-460, Apr. 1995.

[2] R.T. Baird and T. S. Fiez, "Linearity Enhancement of Multi-bit Delta-sigma A/D and D/A Converters Using Data Weighted Averaging," IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 42, no. 12, pp. 753-762, Dec. 1995.

[3] R. Schreier and B. Zhang, "Noise Shaped Multi-bit D/A Converter Employing Unit Elements," Electronics Letters, vol. 31, no. 20, pp. 1712-1713, Sep. 1995.

[4] A. Yasuda, H. Tanimoto, and T. Iida, "A Third-order Delta-sigma Modulator Using Second-order Noise Shaping Dynamic Element Matching," IEEE Journal of Solid-State Circuits, vol. 33, no. 12, pp. 1879-1886, Dec. 1998.

[5] E. Fogleman, J. Welz, and I. Galton, "An Audio ADC Delta-sigma Modulator with 100-dB Peak SINAD and 102-dB DR Using a Second-order Mismatch Shaping DAC," IEEE Journal of Solid-State Circuits, vol. 36, no. 3, pp. 339-348, Mar. 2001.

[6] J. Welz, I. Galton, and E. Fogleman, "Simplified Logic for First-order and Second-order Mismatch Shaping Digital-to-analog Converters," IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 48, no. 11, pp. 1014-1026, Nov. 2001.