STT-MRAM Memory Cells with Enhanced On/Off Ratio

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***Abstract*—Resistive memory technologies are a path to high density, low static power on-chip memories. One such technology, STT-MRAM, exhibits high endurance and is capable of operating as a cache with high write activity. The typically small on/off resistance ratio of the device, however, complicates the sensing process. Two STT-MRAM memory cells are proposed to alleviate this issue. Of the three cells, the diode connected cell increases the resistance ratio by greater than 5x while consuming energy comparable to a standard memory cell during reads.**

I. Introduction

Spin torque transfer magnetoresistive RAM (STT-MRAM) has emerged as a competitive CMOS compatible technology capable of replacing traditional on-chip CMOS memory. With the features of non-volatility, no static power consumption, and nearly unlimited write endurance, STT-MRAM has unique advantages over traditional memory circuits. The Achilles heel of STT-MRAM, however, is the small on/off resistance ratio. This limitation requires sophisticated read circuitry, which leads to greater sensitivity to noise.

To address these limitations, two memory cells are proposed that significantly improve the output read ratio while requiring marginally more area and delivering comparable energy efficiency under high bias. In Section II, background information describing STT-MRAM technology is provided. In Section III, the standard one transistor, one storage element memory cell as well as the proposed cells are described. In Section IV, a circuit model of the STT device, the experimental procedure, and the performance of the memory cells are presented. The article is concluded in Section V.

II. Behavior of spin torque transfer magnetoresistive RAM

Spin torque transfer magnetic tunnel junctions (STT-MTJ), the storage elements in STT-MRAM, are two terminal devices that operate on the principle of spin dependent conduction through magnetic domains [1]–[5]. The device is structured as a stack of thin films where a thin oxide layer separates two, typically $CoFeB$, ferromagnetic layers. Of these ferromagnetic layers, one has a fixed spin polarity (the *fixed* layer) that transmits electrons of the same spin direction and reflects back electrons with the opposite spin; the other layer (the *free* layer) has a bistable magnetic polarity that is affected by the spin of the incoming electrons. By controlling the direction of current through the device, either the transmitted electrons or the reflected electrons influence the free layer. Applying large bias currents to the STT-MTJ (approximately 35 μA to 300 μA) can switch the polarity of the device.

STT-MTJs are structured to ensure that the polarity of the free layer is always either parallel or anti-parallel to the polarity of the fixed layer. The tunneling current through the MTJ, *i.e.* the resistance of the device, is minimized in the parallel state (R_{on}) and maximized in the anti-parallel state (R_{off}). In the parallel state, the electrons transmitted through the fixed layer have the same spin as the free layer, which minimizes the resistance through the device. Alternatively, an anti-parallel alignment causes the current from the polarizer to be reflected off the free layer. This reflection manifests as an increase in resistance.

The key figure of merit of an STT-MTJ describing the change in resistance is the tunneling magnetoresistance ratio (TMR),

$$TMR = \frac{R_{OFF} - R_{ON}}{R_{ON}}, \tag{1}$$

where R_{ON} and R_{OFF} describe the minimum and maximum resistance of an MTJ. An STT-MTJ typically exhibits a peak TMR ratio between 80% to 150%, corresponding to roughly a 100% (or 2x) change in resistance. The peak TMR is determined with a near zero voltage bias across the MTJ, which decreases with increasing voltage across the device [6]. The primary goal of the proposed circuits is to increase the TMR at the memory cell level by improving the current ratio (I_{ON}/I_{OFF}) observed by the sensing circuitry.

III. Cell types

Three basic cell types, proposed for use in memories based on STT-MTJs as well as other resistive memory technologies, are outlined in this section. The standard 1T - 1MTJ memory cell is initially described, followed by the proposed 2T - 1MTJ diode and gate connected memory cells.

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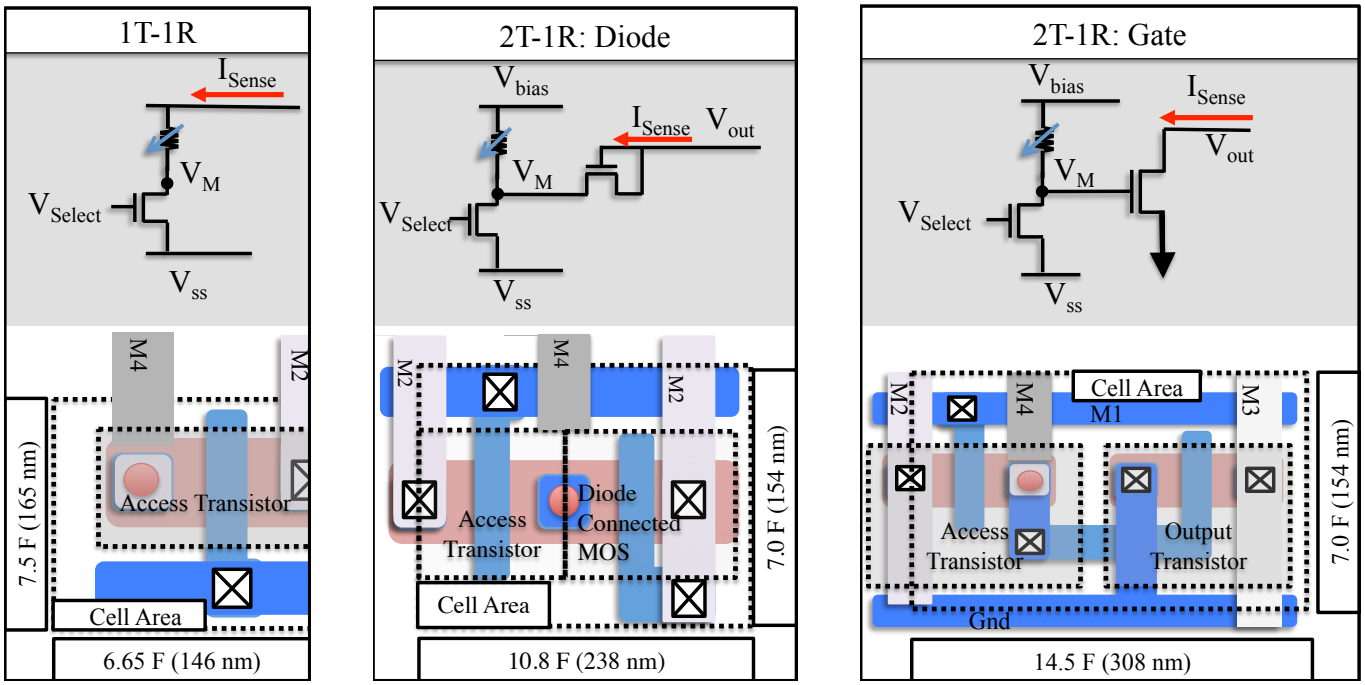

(a) (b) (c)

Fig. 1. Circuit diagram of STT-MTJ memory cells: (a) standard 1T - 1MTJ, (b) 2T - 1MTJ diode cell, and (c) 2T - 1MTJ gate cell. The physical layout is based on the FreePDK45 where F represents the feature size of the technology [7].

A. 1T - 1MTJ cell

Due to the simplicity and relatively high density, a one transistor, one magnetic tunnel junction (1T - 1MTJ) cell is the most commonly used cell type in STT-MTJ memories (see Figure 1(a)). A single transistor controls which cell is connected to a bit line shared across a column. The small TMR of the MTJ, however, complicates reads as the available sensing margin is low (approximately 2x). Moreover, the series bit line resistance reduces the resistance ratio seen by the sensing circuitry in larger arrays. Furthermore, MTJ devices exhibit a bias dependence whereby increasing the voltage across the device has the adverse effect of lowering the TMR. This reduction, at high voltage bias, further lowers the sense margin and leads to an increased likelihood of an erroneous read [8]. A model describing this effect is presented in Section IV-A.

B. 2T - 1MTJ diode cell

The addition of a diode connected transistor within the memory cell lowers I_{OFF}, producing a larger I_{ON}/I_{OFF} ratio. As shown in Figure 1(b), the diode connected MOSFET within the 2T - 1MTJ cell is connected at node M (note V_M in Figure 1(b)). The change in the MTJ state shifts the voltage V_M ($\Delta V_M = V_{M(ON)} - V_{M(OFF)}$), which turns on the diode connected transistor. Intuitively, increasing ΔV_M enhances the change in current through the diode. At higher bias, ΔV_M can be increased, leading to a greater change in the on/off ratio of the memory cell.

C. 2T - 1MTJ gate cell

The MTJ gate cell differs from the diode connected cell in that this cell provides isolation between the sensed bit line and the bias line. Additional output transistors can be added in parallel to node M (note V_M in Figure 1(c)) to produce additional read ports without affecting the MTJ branch of the cell. The primary difference between the two proposed cells is that the gate connected cell requires the average value of V_M to be approximately equivalent to the threshold voltage of the transistor. This constraint necessitates either increasing V_{bias} or raising the resistance of the select transistor. As a result, there is a tradeoff between the magnitude of ΔV_M and the average value of V_M for the on and off states. In the diode connected cell, the output voltage is lowered to adjust the voltage at which the output transistor turns on. The input and output of the gate cell are, however, independent. Additionally, V_{bias} is bounded by the minimum write voltage of the MTJ.

IV. Comparison of Cell Performance

Assessing the performance of each cell type requires bias constraints that maximize the output resistance ratio for each cell. The following section outlines the modeling strategy and compares the characteristics of each memory cell type.

A. Circuit model

The ideal reference threshold voltage for maximizing the noise margin of a resistive memory occurs at the geometric

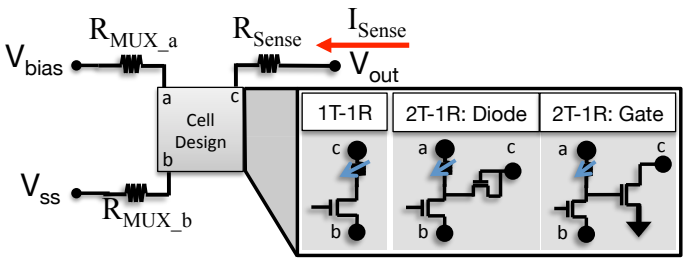

Fig. 2. Framework for evaluating memory cell types. R_{MUX} represents the resistance attributable to the access multiplexers and the output resistance of the supply circuitry. R_{Sense} is the input resistance of the sense amplifier. In the 1T - 1MTJ cell, R_{MUX_a} is ignored as only two terminals are available for the device. Both the diode cell and gate cell are connected to all three terminals.

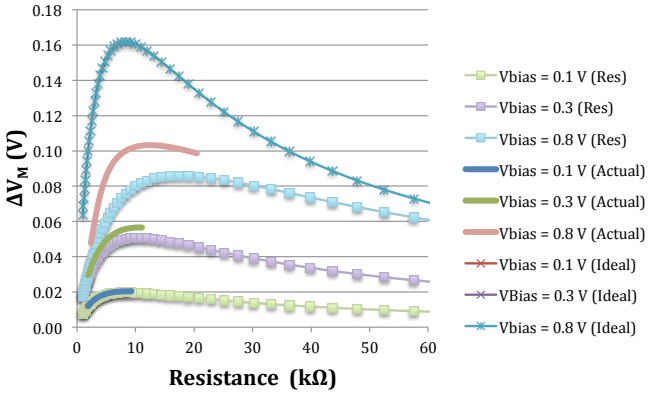

Fig. 3. On-off voltage signal for different device resistances of the select transistor at node V_M (see Figure 1(a)). The curves labeled ideal represent the expected performance of the 1T - 1MTJ cell without the reduced bias dependence. The curves (Res) illustrate the operation of a linearized model of a transistor and the bias dependence of the MTJ.

mean of the maximum and minimum resistances [9]. Incorporating this threshold voltage, the memory access circuitry is sized to improve the sensing margin within the cell,

$$R_t + R_{ret} = \sqrt{R_{ON} + R_{fwd}}\sqrt{R_{OFF} + R_{fwd}}, \quad (2)$$

where R_{fwd} is the resistance from the voltage supply to the cell, R_{ret} is the resistance of the return path to ground, and R_t is the linearized resistance of the transistor at which ΔV_M is maximum. This expression assumes the access transistor operates in the linear mode. This assumption is valid for read operations where the bias across the access transistor is low relative to the power supply.

An STT-MTJ, however, cannot be treated as an ideal resistor. These devices maintain a voltage dependent resistance that significantly lowers R_{OFF} with increasing bias. Expression (2) therefore becomes

$$R_t + R_{ret} = \sqrt{R_{ON} + R_{fwd}} \sqrt{R_{ON}(TMR(V_{MTJ}) + 1) + R_{fwd}}, \quad (3)$$

where the TMR is

$$TMR(V_{MTJ}) = \frac{TMR_0}{1 + \frac{V_{MTJ}^2}{V_h^2}}. \quad (4)$$

V_{MTJ} is the voltage across the device, and V_h is the voltage when the TMR is degraded by 50% [10]. The bias degradation in the TMR is primarily observed when the device is in the anti-parallel state (R_{OFF}); therefore, R_{ON} is assumed constant. This model captures the DC operation of the MTJ and is valid in all cases where V_{MTJ} is less than the minimum write voltage of an MTJ device. Due to the bias dependence, the sense margin is degraded as compared to the ideal case.

Interestingly, comparing the linearized model of a transistor to a simulation of a full transistor model (see Figure 3), ΔV_M is larger than expected, permitting the cell transistor to be conservatively approximated as a resistor. As depicted in Figure 3, the linearized model is a good approximation under low bias conditions. When the diode connected cell is biased to ensure that the change in V_M occurs around the threshold voltage of the diode, the difference in the current through the diode reaches the maximum.

The aforementioned model has been applied to optimize the bias conditions for each memory cell. The circuit shown in Figure 2 illustrates the model. The SPICE simulations are based on the 22 nm Predictive Technology Model (PTM) [11]. The parasitic impedances are determined for a 32 x 32 bit array based on the cell layouts depicted in Figure 1. These layouts utilize design rules from the FreePDK45 that are scaled to a 22 nm feature size [7]. The MTJ parameters are from the ITRS [5].

Each cell contains the same basic structure of a 1T - 1MTJ cell. The primary sizing constraint is due to the minimum write current of the MTJ. Optimizing this cell requires adjusting the bias voltage of the select and output transistors to match the resistance of the MTJ. In the 1T - 1MTJ memory cell, no separate output branch exists. The ratio is determined by the ratio of the currents passing through the MTJ. The diode and gate cells are normalized to the average of I_{ON} and I_{OFF} within the 1T - 1MTJ cell. While the bias conditions often produce a maximum on/off current ratio exceeding 100x, the absolute magnitude of the currents is limited to several picoamps. As a result, a minimum sense current of 1 μA is maintained for each bias condition. In the case of the gate cell, an iterative approach is applied to maximize the current ratio due to the aforementioned threshold voltage constraint on the output transistor. The transistor is linearized, as outlined in

TABLE I
PARAMETERS OF TRANSISTOR AND MTJ

W_{access}	50 nm
W_{out}	50 nm
$MTJR_{ON}$	5 $k\Omega$
$MTJR_{OFF}$	12.5 $k\Omega$
TMR	150%

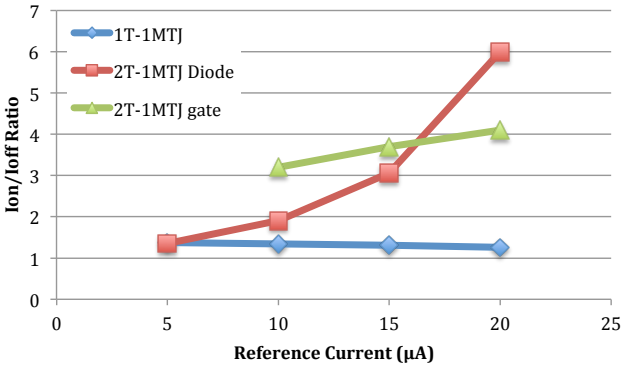

Fig. 4. Ratio of I_{ON} and I_{OFF} for each cell type for different reference currents.

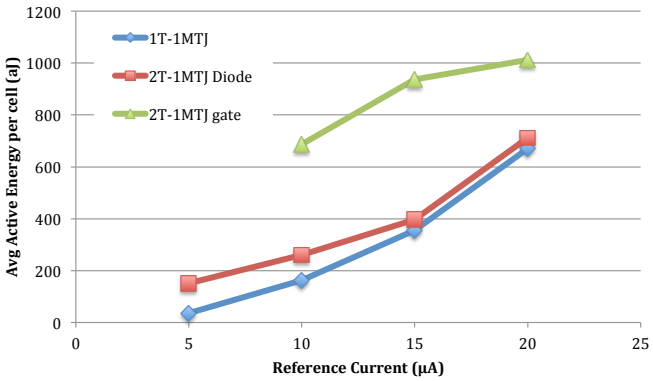

Fig. 5. Average active energy of each cell type

Section IV-A, and each terminal is evaluated to maximize the output current ratio.

B. Output current ratio

The output current ratio for each cell type is listed in Table II. The diode connected cell performs better than the standard cell and gate cell in terms of the output current ratio at high current bias (see Figure 4). Moreover, the diode cell expends active energy comparable to the 1T - 1MTJ cell at all observed current biases. The diode cell outperforms the gate cell since the bias voltage of the diode cell is not constrained by the transistor threshold voltage. A gate cell requires the average value of V_M to be approximately equal to the transistor threshold voltage to maximize the change in output current. This choice of V_M is difficult to achieve, as a higher V_{bias} lowers the TMR of the MTJ and may inadvertently write to the device. At low bias conditions, the diode cell has a lower output current ratio than the gate cell. The iterative approach to optimizing a gate cell utilizes the nonlinearity of the select transistor to boost the observed output current ratio. As mentioned in Section IV-A, linearizing the transistor model is a conservative approximation when optimizing the cell. A diode cell would enjoy this advantage as well.

C. Physical area

The diode connected and gate connected cells consume more area than the standard 1T - 1MTJ cell. Each proposed memory cell type requires, respectively, a 1.54x and 2.03x increase in area. The gate cell requires significantly more area than the diode cell because of the extra poly-to-metal contact as well as the required space between the select and output transistor (see Figure 1). The diode cell merges the select and output transistors using a single two finger transistor layout for reduced area.

D. Variational effects

Of the two proposed memory cells, the gate connected cell is more sensitive to variational effects. A shift in the threshold voltage of the output transistor drastically affects the operating point of the device. The diode connected cell is more tolerant to threshold variations, as a change in the threshold voltage of the device can be compensated by a change in the voltage V_{out}.

E. Cell writes

In the 1T - 1MTJ cell, writes are applied by either forward biasing or reverse biasing the bit lines. In the forward bias case, where the MTJ terminal is biased to V_{DD}, the cell access transistor operates in the linear region and does not limit the current through the MTJ. In the reverse bias case, however, the access transistor operates in a diode connected manner and thus the threshold drop across the access device limits the voltage drop across the MTJ. This voltage drop places an upper limit on the switching current that can be applied to the cell.

The addition of a gate connected read port has little effect on writes indicating that the gate connected cell is also limited by the maximum reverse bias current. The diode connected cell, however, acts as a parallel transistor to the cell access transistor when applying a reverse bias to the MTJ. Intuitively, biasing the diode connected read port to V_{DD} increases the effective width of the cell access transistor, leading to a linear increase in the current applied to the MTJ. Since the diode connected transistor and the access transistor have the same width, the reverse biased current through the MTJ can be increased by a factor of two. This situation presents an additional opportunity to reduce either the cell area or the write latency of the array.

F. Applications

As introduced in Section I, STT-MTJ based memories are advantageous for highly active caches because of the high endurance and durability exhibited by this technology. These small caches, typically optimized for speed, are dominated by the large peripheral circuitry required to operate the circuit at high speed [12]. The diode connected and gate connected cells, which consume more area as compared to the standard 1T - 1MTJ cell, are more effective in active caches that operate more frequently than large, dense caches. At low bias conditions, however, the gate cell is less preferable since the on current does not provide 1 μA under any bias conditions. The

TABLE II
CELL BIAS AND OPERATION

	1T - 1MTJ	2T - 1MTJ Diode	2T - 1MTJ gate
I_{ON}/I_{OFF}	1.26	5.98	4.06
I_{ON} (μA)	23.2	21	21
I_{Sense} (μA)	—	1	1
ΔV_M (mV)	43	65	69
Avg. active energy (aJ)	670	712	1013
Cell area (F^2)	49.9	75.6	101.5

diode cell, except in extremely low bias conditions, is therefore preferable due to the improved current ratio and comparable active energy.

V. CONCLUSIONS

Two alternative memory cells are presented and contrasted with a standard 1T - 1MTJ cell. These additional cell types demonstrate a greater then 5x improvement in the output current on/off ratio. The gate connected cell, which offers the ability to add additional read ports, requires greater energy and exhibits a reduced resistance ratio as compared to the diode connected cell. The diode cell, due to the small area and high output current ratio, is therefore the most effective memory cell of the three cells under consideration.

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