Delay and Power Expressions for a CMOS Inverter Driving a Resistive-Capacitive Load

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Abstract – A delay and power model of a CMOS inverter driving a resistive-capacitive load is presented. The model is derived from Sakurai's alpha power law and exhibits good accuracy. The model can be used to design and analyze those inverters that drive a large *RC* load when considering both speed and power. Expressions are provided for estimating the propagation delay, transition time, and short circuit power dissipation for a CMOS inverter driving resistive-capacitive interconnect lines.

I. Introduction

As the size of CMOS integrated circuits continues to increase, interconnections have become increasingly significant. With a linear increase in length, interconnect delay increases quadratically due to a linear increase in both interconnect resistance and capacitance [1]. Also, large interconnect loads not only affect performance but cause excess power to be dissipated. A large *RC* load degrades the waveform shape, dissipating excessive short circuit power in the following stages loading a CMOS logic gate.

Several methods have been introduced to reduce interconnect delay so that these impedances do not dominate the delay of a critical path [1–4]. Furthermore, with the introduction of portable computers, power has become an increasingly important factor in the circuit design process. Thus, power consumption must be accurately estimated when considering techniques for improving the speed of long interconnections.

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In this paper, an analytical expression for the transient response of a CMOS inverter driving a lumped *RC* load is presented. The approach is different from Kayssi *et al.* [5] in that a lumped *RC* load is considered rather than a lossless capacitive load. Furthermore, Sakurai's alpha power law [6] is used to describe the circuit operation of the CMOS transistors rather than the classical Shichman-Hodges model [7]. The alpha power law model considers short channel behavior, permitting increased accuracy and generality in the delay and power expressions. These expressions are used to estimate the propagation delay and the rise and fall times (or transition times) of a CMOS inverter. Since the output waveform is accurately calculated, the short circuit power dissipated by the following stage can also be estimated. Furthermore, due to its relative simplicity, this expression permits linear programming techniques to be used when optimizing the placement of buffers for both speed and power.

The paper is organized as follows: expressions for an inverter driving a lumped *RC* load are derived, and characteristic delay equations are presented and compared with SPICE in Section II. Error bounds are discussed in Section III. In Section IV, the short circuit power dissipation of a CMOS inverter following a lumped *RC* load is introduced and compared with SPICE. Finally, some concluding remarks are offered in Section V.

II. General Solution

An analytical expression describing the behavior of an inverter driving a lumped *RC* load (shown in Figure 1) based on Sakurai's alpha power law model [6] is presented. The alpha power law model more accurately describes short-channel behavior, such as velocity saturation, while providing a tractable equa-

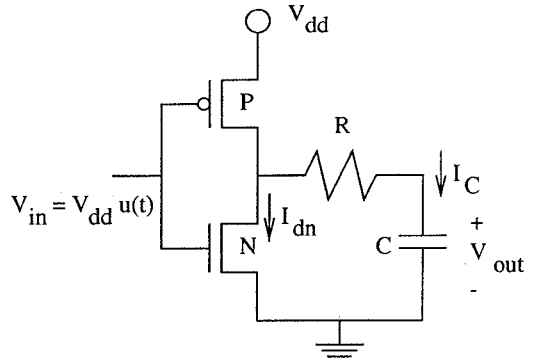

Figure 1. CMOS inverter driving an *RC* load

tion. Specifically, the linear region of the ON transistor is used, since a large portion of the circuit operation occurs within this region under the assumption of a step input signal. When the input to the inverter is a unit step or fast ramp, V_{out} is initially larger than V_{GS}—V_T for a shorter period of time than if the input to the inverter is a slow ramp. Therefore, the circuit operates in the linear region for a greater portion of the total transition time for a large *RC* load. If the input waveform increases more slowly or the load impedance is small, the inverter operates in the saturation region for a longer time before switching into the linear region.

Only the falling output (rising input) waveform is considered. The following analysis, however, is equally applicable to a rising output (falling input) waveform. The lumped load is modeled as a resistor in series with a capacitor. The current through the output load capacitance is the same magnitude and opposite sign as the N-channel drain current. The capacitive current is

$$i_C = C\frac{dV_{out}}{dt} = -i_d, \qquad (1)$$

where C is the output capacitance, V_{out} is the voltage across that capacitance, i_C is the current through the capacitor, and i_d is the drain current through the N-channel device.

The N-channel linear drain current is given by

$$-C\frac{dV_{out}}{dt} = i_d = \frac{I_{do}}{V_{do}}\left(\frac{V_{gs}-V_T}{V_{DD}-V_T}\right)^{\alpha} V_{ds}, \qquad (2)$$

$$for \quad V_{gs} \geq V_T, V_{gs} - V_T \geq V_{ds} \ .$$

In the alpha power law model, I_{do} represents the drive current of the MOS device and is proportional to W/L, V_{do} represents the drain-to-source voltage at which velocity saturation occurs with $V_{GS} = V_{DD}$ and is a process dependent constant, and α models the process dependent degree to which the velocity saturation affects the drain-to-source current. α is within the range $1 \leq \alpha \leq 2$, where $\alpha = 1$ corresponds to a device operating strongly under velocity saturation, while $\alpha = 2$ represents a device where there is negligible velocity saturation. V_{DD} is the supply voltage, and V_T is the MOS threshold voltage (where V_{TN} (V_{TP}) is the N-channel (P-channel) threshold voltage).

Assuming a unit step input is applied to the circuit shown in Figure 1, V_{out} can be derived from (2). The linear equation, rewritten in Laplace form, is

$$SCV_{out} + S\mho_{do}RCV_{out} + \mho_{do}V_{out} = CV_o(0) + \mho_{do}RCV_{out}(0) \ , \qquad (3)$$

where $\mho_{do} = \frac{I_{do}}{V_{do}}$ is the saturation conductance.

Equation (3) yields

$$V_{out}(t) = V_{out}(0)e^{\frac{-\mho_{do}}{\mho_{do}RC+\frac{C}{K}}t} \ . \qquad (4)$$

When $K = 2$, (4) closely approximates SPICE. This empirical value for K is stable for a wide range of *RC* loads and across several short-channel technologies. Graphs of V_{out} versus time for several values of resistance and capacitance are shown in Figure 2. The analytical expression shown in (4) closely approximates SPICE for most of the region of operation for a range of load impedances from 10 Ω to 1000 Ω and from 10 fF to 1 pF. The maximum error over this range, shown in Table I, is 27% for a .8 μm CMOS technology.

From (4), the propagation delay of a CMOS inverter calculated at the 50% point t_{PD} is

$$t_{PD} = .693\frac{\frac{C}{K}+\mho_{do}RC}{\mho_{do}} \ . \qquad (5)$$

The transition time of a CMOS inverter driving a lumped *RC* load calculated at the 90% point t_t is

$$t_t = 2.3\frac{\frac{C}{K}+\mho_{do}RC}{\mho_{do}} \ . \qquad (6)$$

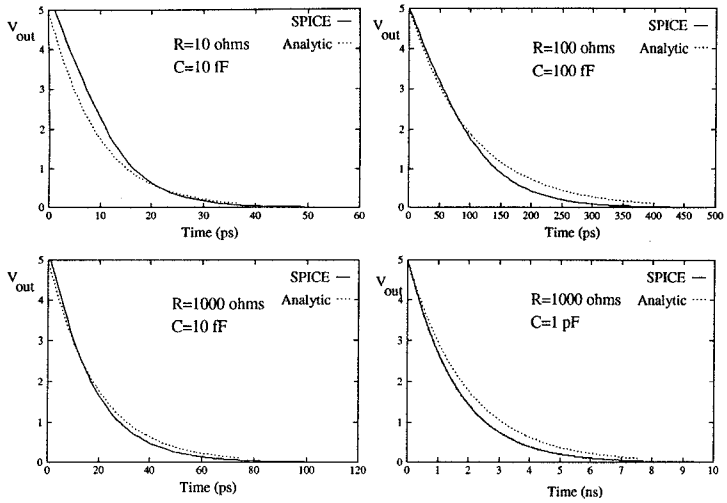

Figure 2. Output response of a CMOS inverter driving an *RC* load

The accuracy of the analytic model versus SPICE is tabulated in Table I for a wide variety of output load resistances and capacitances. Note that both the 50% propagation delay and the transition time are shown. The maximum error of the transition time t_t as compared with SPICE is 27%, and the maximum error of the propagation delay t_{PD} as compared with SPICE is 25% for a .8 μm CMOS technology.

Equations (5) and (6) can be used to estimate the propagation delay and transition time of a CMOS inverter driving a long resistive interconnect line. Since the shape of the output waveform is known, these expressions can also be used to estimate the short circuit power dissipation of the CMOS gate loading the high impedance interconnect line, as described in Section IV.

Table I. Propagation delay and rise time of an inverter driving an *RC* load (.8 μm CMOS technology).

Load Resistance	Load Capacitance	t_t		t_{PD}		Error	
		Analytic	SPICE	Analytic	SPICE	t_t	t_{PD}
10 Ω	.01 pF	21 ps	22 ps	6.5 ps	8.7 ps	4%	25%
10 Ω	.1 pF	215 ps	176 ps	65 ps	70 ps	22%	7%
10 Ω	1 pF	2.2 ns	1.7 ns	649 ps	680 ps	27%	4%
100 Ω	.01 pF	24 ps	22 ps	7.2 ps	8.8 ps	6%	19%
100 Ω	.1 pF	235 ps	187 ps	71 ps	73 ps	25%	2 %
100 Ω	1 pF	2.4 ns	1.9 ns	712 ps	711 ps	25%	0 %
1000 Ω	.01 pF	44 ps	39 ps	13 ps	13 ps	13%	0 %
1000 Ω	.1 pF	444 ps	365 ps	133 ps	115 ps	15%	16%
1000 Ω	1 pF	4.4 ns	3.6 ns	1.3 ns	1.1 ns	22%	18%

III. Error Bounds

The maximum error for the transition time for *RC* loads ranging from 10 Ω to 1000 Ω and 10 fF to 1 pF and for three different technologies (.8 μm, 1.2 μm, and 1.6 μm CMOS) is 57%. The maximum error for the propagation delay is 43% over the same ranges and technologies. As the capacitance increases to 1 pF, the error of the propagation delay generally decreases to less than 20%. A similar decrease occurs for the transition time. Furthermore, both errors generally decrease with increasing load resistance.

The improved accuracy with increasing load resistance and capacitance is due to the effect of the *RC* load on the inverter delay characteristics dominating the device parasitics, thus improving the accuracy of the transistor I-V model. This behavior also explains why the accuracy improves as the geometric size of the transistors and the parasitic device resistances and capacitances get smaller. Thus, these delay expressions become more accurate for higher *RC* loads and more aggressive technologies.

IV. Power Estimation

There are two primary contributions to the total power dissipated by a CMOS inverter, dynamic CV^2f power dissipation and short-circuit power dissipation [8,9]. The logic stage following a large *RC* load will dissipate significant amounts of short-circuit power due to the degraded waveform originating from the initial CMOS inverter. During the region where the input signal is between V_{TN} and $V_{DD}+V_{TP}$, a DC current path exists between V_{DD} and ground. This excess current is called short-circuit (or crossover) current [9]. The short-circuit power dissipation of the following stage for one transition (either rising or falling edge) can be approximated by

$$P_{SC} = \frac{1}{2} V_{DD} I_{peak} t_t f \quad , \qquad (7)$$

where f is the frequency of operation, t_t is the transition time of the input waveform, and I_{peak} is the maximum saturation current of the load transistor. I_{peak} depends on both V_{GS} and V_{DS}, therefore it is both input waveform and load dependent.

Table II. Estimate of short-circuit power dissipated by a CMOS inverter loading a CMOS inverter driving an *RC* load (.8 μm CMOS technology).

Load Resistance	Load Capacitance	Power (μW) f=10 Mhz		Error
		Analytic	SPICE	
10 Ω	.3 pF	1.70	.99	42%
10 Ω	.5 pF	4.86	3.22	34%
10 Ω	1 pF	15.4	11.1	28%
100 Ω	.3 pF	2.09	1.23	41%
100 Ω	.5 pF	5.68	3.83	32%
100 Ω	1 pF	17.1	12.7	26%
1000 Ω	.3 pF	7.18	5.2	28%
1000 Ω	.5 pF	15.8	12.2	23%
1000 Ω	1 pF	41.7	3.38	19%

By inserting the transition time from (6) into (7), the short circuit power dissipation of a CMOS inverter following a lumped *RC* load over both the rising and falling transitions is

$$P_{SC} = 2.3 V_{DD} I_{peak} f \frac{\frac{C}{K} + \upsilon_{do} RC}{\upsilon_{do}} \quad . \qquad (8)$$

The short-circuit power for a wide variety of *RC* loads between the CMOS inverter stages derived from the analytical expression is compared to that of SPICE in Table II. For smaller loads, hence, faster transition times, there is neglible short circuit power since a direct path from the power supply to ground does not exist for any significant time. The short circuit power becomes non-neglible when larger interconnect loads between stages cause a transition time of significant magnitude, such as greater than .5 ns for a .8 μm CMOS inverter. At this borderline value, SPICE departs from the analytical value by a maximum of 42%. As the *RC* load and transition time increase, the error decreases to less than 20%. With the longer transition times, the analytically derived short circuit power closely approximates the short circuit power dissipation derived from SPICE. Furthermore, the short circuit power becomes significant when the CMOS inverter is loaded by larger *RC* loads, creating long transition times. It is this condition that is of greatest interest when considering short circuit power in resistively loaded CMOS inverters.

V. Conclusions

A simple yet accurate expression for the output voltage of a CMOS inverter as a function of time driving a resistive-capacitive load is presented. With this expression, equations characterizing the propagation delay and transition time of a CMOS inverter driving an *RC* load are presented. Furthermore, since the output waveform of this circuit is accurately modeled, the short-circuit power dissipation of the following CMOS stage loading the interconnect line can be estimated within 42%, and typically under 20% for highly resistive lines. Therefore, due to the simplicity and accuracy of these expressions, the delay and power characteristics of a CMOS inverter driving a high impedance *RC* interconnect line can be efficiently estimated.

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