A Cadence-Based Design Environment for Single Flux Quantum Circuits

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***Abstract*—The semiconductor industry standard computer-aided-design (CAD) tool Cadence has been calibrated for a 3 μm Niobium technology in order to design and build superconductive single flux quantum (SFQ) circuits. The top-down design methodology includes Verilog functional simulation, schematic capture, graphic layout, functional verification, design rule checking, electrical rule checking, and layout-vs.-schematic verification. This design framework has been used successfully at the University of Rochester in designing more than 15 elementary SFQ cells and three large scale digital and mixed-signal SFQ circuits, demonstrating significant improvement in both design efficiency and accuracy.**

I. Introduction

With a junction switching speed on the order of picoseconds and power consumption of approximately 0.2 μW/junction, SFQ circuits have superior performance characteristics as compared with semiconductor technologies [1]. However, due to the immaturity of this technology, both the process complexity and the lack of a design infrastructure have slowed the development of practical SFQ circuits.

Until very recently, most work in CAD for superconductive circuits has focused on specific elements of the design process, *e.g.*, circuit-level simulation [2], inductance extraction [3],[4], operating margin optimization [5] and logic level simulation [6]. More complete design environments for superconductive circuits exist for only voltage-state logic [7],[8], though not for SFQ technology. In order to more efficiently and accurately develop SFQ circuits, the infrastructure for designing these circuits must be enhanced. In response to these needs, the industry standard IC CAD tool, Cadence DFII™, has been calibrated based on the Hypres $Nb/Al_2O_3/Nb$ tri-layer 3 μm junction technology [9] to provide an integrated high performance design environment for developing SFQ circuits.

A top-down circuit design methodology that operates from behavioral description through physical layout (see Fig. 1) has been developed [10]. Highlights of this methodology include: behavioral, logic, and circuit simulation; layout-versus-schematic (LVS) verification; electrical rule verification; design rule verification; and graphic layout synthesis. Using this Cadence-based design environment, an 11 GHz 8 bit FIR filter and A/D converter, comprised of 112 clocked gates and a 128 bit circular shift register [11]–[14], is currently being built.

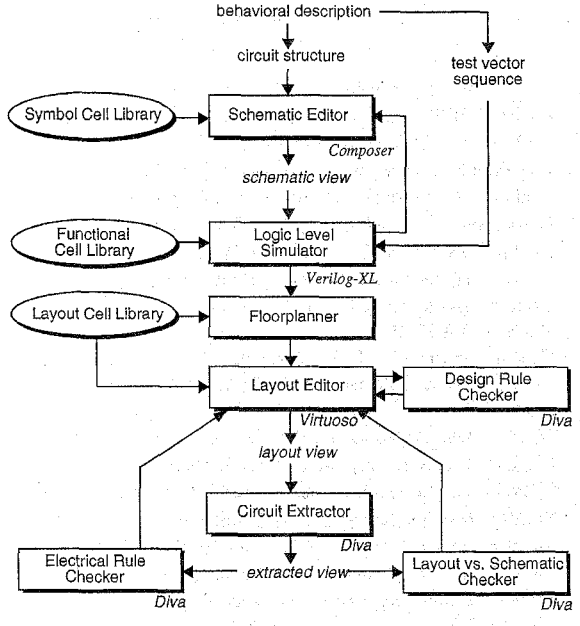

Fig. 1. Flow chart of top-down design process for SFQ circuits.

Selected phases of this design methodology in the calibrated Cadence environment are shown in Fig. 1 and reviewed in this paper in the order in which each phase occurs in the design process. In Section II, the process for behaviorally simulating these SFQ circuits is discussed. The capability for schematic capture is described in Section III. Layout synthesis is described in Section IV. In Section V, additional verification techniques are reviewed. The final results are summarized in Section VI.

II. Verilog HDL for SFQ circuits HDL for SFQ Circuits

As the size of SFQ circuits continues to increase, it has become increasingly difficult to use circuit level simulators to verify the circuit functionality and timing. For small circuits, the behavioral description may be informal, using text specification, mathematical formulas, or a C program. However, for more complex circuits, the behavioral description must be more formal. To overcome this problem, a standard approach for describing circuit function, Verilog® has been

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adopted from semiconductor-based logic design and applied to SFQ technology.

Verilog is a hardware description language (HDL) that has become an industry standard tool for behavioral and functional simulation [15]. With Verilog, the operation of a large circuit is delineated at the beginning of the design process. Initially, a function is described in Verilog and tested for the appropriate outputs for a given set of inputs. Once the function has been determined to be correct, additional information such as timing can be detailed and analyzed using Verilog.

Implementing Verilog in SFQ technology does not have a one-to-one correspondence with semiconductor technology due to some inherent differences between superconductor and semiconductor technologies. One of the fundamental differences between a semiconductor technology such as CMOS static logic and the superconductive SFQ technology is that CMOS is based on voltage-level logic whereas SFQ circuits operate on voltage or current pulses occurring within a specified period. Additionally, the SFQ convention for representing a logic state requires that most of the logic components, including basic gates such as NOT, AND, and OR, must be synchronous (or clocked), *i.e.*, the logic function must be combined with the storage capability. Therefore, SFQ signals are modeled in Verilog as pulses by latching signals into asynchronous registers. If the set-up and hold times of each logic element are satisfied, then the data are latched out of the registers. A fragment of Verilog code describing an SFQ AND gate is shown in Fig. 2. Note that in addition to the variables for register states and outputs describing the function, variables for describing the hold time, set-up time, and clock delay are also declared.

Creating behavioral descriptions (often called functional views) in Verilog for SFQ circuits is a multi-step process. Once the internal circuit structure is developed and optimized, exact values of timing parameters specific for each implementation of a cell can be extracted [6]. This information is then included in the behavioral description for each separate implementation of a logic gate. When this more detailed information is included in the behavioral description of a large circuit-under-test, correct functionality and optimum timing can be determined about two orders of magnitude faster than with a circuit level simulator [16].

Near-term plans include automatically synthesizing a description of the SFQ circuit at the logic level from the Verilog input format. Once a standard library of SFQ cells is developed, automatic logic synthesis from a high level description is possible. This capability will further reduce design cycle time.

III. Schematic Description for Simulation and Verification

Once the circuit behavior and timing have been functionally verified, a more detailed description of the circuit is necessary. A schematic description provides that detail.

```
module and_gate (a, b, clk, out);

input
   a, b, clk;
output
   out;
reg
   out;
parameter
   t_hold  = 12,
   t_setup =  1,
   delay   = 25,
   warning_file=3;
reg
   a_internal, b_internal, clk_internal,
   a_state, b_state,  // internal state at inputs a and b
   a_set, b_set;      // signals determining the moment
                      // the state of the a,b inputs changes
integer
   data_delay, // delay between a (b) and a_internal
   clk_delay,       // delay between clk and clk_internal
   out_delay,       // delay between clk_internal and out
   out_value,       // output value in a given clock cycle
   last_clk_time;  // time when the last clock pulse

initial
   begin
        if(t_hold<0)
            begin
                data_delay = -t_hold;
                clk_delay = 0;
                out_delay = delay;

                a_state = 1;
            else
....
```

Fig. 2. Sample Verilog code describing an SFQ AND gate.

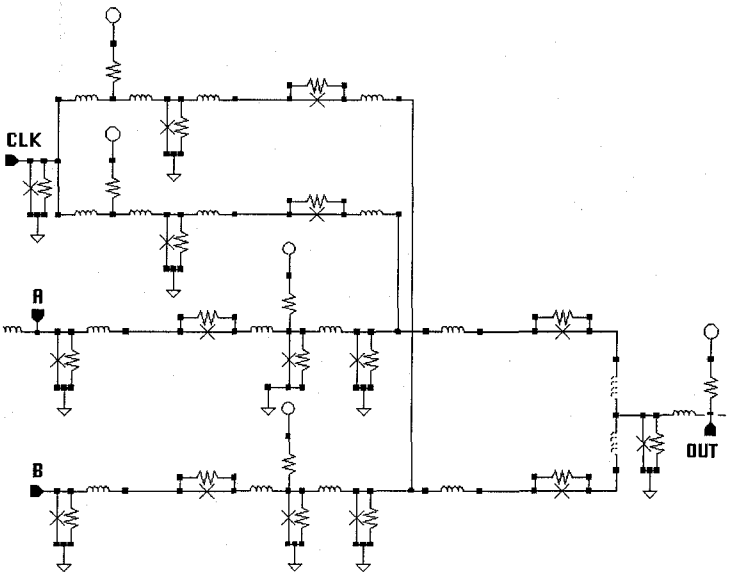

Fig. 3. The schematic diagram of an AND gate in SFQ technology composed of JJs, resistors, and inductors.

In a schematic description, the circuit is described hierarchically. At the bottom level of this hierarchy are the fundamental building blocks of all SFQ circuits— Josephson junctions (JJs), resistors, and inductors. These basic components comprise the next level in the hierarchy, simple logic gates such as AND and NOT (see Fig. 3). In turn, these simple gates comprise more complex functional circuits.

A circuit netlist is extracted from the schematic description. This netlist provides detailed information describing each de-

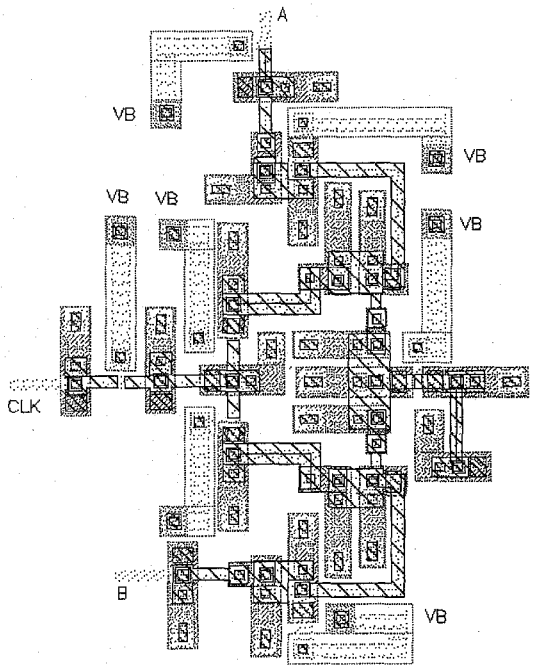

Fig. 4. The physical layout of an AND circuit in superconductive SFQ technology.

vice in the circuit, *e.g.*, junction area, resistance, and inductance. The netlist and the input stimuli together constitute a complete test file for the circuit level simulator Jspice3. In addition to providing circuit simulation information, a functionally verified schematic description of the circuit provides the reference information necessary for verifying the final geometric data. This process is discussed in section V.

IV. Graphic Layout and Circuit Extraction

Graphic layout is the lowest level used to describe a circuit. At this level, the circuit is described in terms of the physical geometric data used to produce the individual masks for lithography. The superconducting technology used to manufacture the circuits is provided by Hypres Inc. This technology is a four wire layer, ten level, all Niobium $Nb/Al_2O_3/Nb$ tri-layer process. Therefore, the graphic layout environment supported by Cadence DIVA™ [17] has been calibrated based on this superconductive technology. A sample layout of an AND gate in this technology is illustrated in Fig. 4.

Once the circuit has been physically laid out, certain characteristics can be extracted from the graphical data. The device extraction process recognizes specific junctions, resistors, or inductors by combinations of mask layers. The location of each device is noted and a circuit netlist is created, describing the circuit connectivity. During the extraction process, the physical parameters of each device are attached to its instance using additional calibrated features of DIVA. Two additional graphic layout layers have been added to the standard ten layer mask set in order to identify significant inductors. In the SFQ technology, only wires which pass AC current are considered as inductors. Wires which pass only DC current are considered to be simple connections. Therefore, those metal lines that are intended to be inductors are specified.

One of the more important steps in developing a CAD-based design infrastructure for SFQ circuits is parasitic device extraction. Parasitic impedances are always present in integrated circuits, whether superconductive or semiconductor, and typically cannot be ignored. In the case of SFQ technology, the parasitic inductance of the superconductive layers is of primary concern. After the first draft of the circuit layout is drawn, points of obvious parasitic inductance are marked with the additional mask layers and are extracted in a similar fashion as desired inductances. The circuit schematic is updated accordingly.

V. Techniques for Circuit Verification

In order to assure proper circuit operation before fabrication, the circuit must be fully verified. Circuit verification occurs throughout the entire design process. As discussed in section II, Verilog permits the functional and high-level timing of a circuit to be verified. Based on the schematic description, the circuit timing can be simulated using Jspice3. However, preventable fatal errors may still appear in the lowest levels of the design hierarchy, the physical layout.

Assurance that the physical layout meets the specifications defined by the fabrication process is performed with design rule checking (DRC). DRC is used to evaluate the graphic layout data for any physical design rule violations. In an interactive process, errors are flagged during physical layout, permitting the violations to be immediately corrected. The design rules are calibrated for same-layer spacing, different-layer spacing, minimum width, on-grid alignment, and layer enclosure. An example of a DRC violation is shown in Fig. 5.

Another step in the verification process is electrical rule checking (ERC). The circuit that is extracted from the physical layout is checked by ERC to assure that the circuit does not contain any electrical errors (*e.g.*, power/ground shorts or unconnected floating nodes). ERC is a precursor to layout-versus-schematic (LVS) verification. With LVS, the physical (or extracted) layout is compared directly against a schematic description by a comparison of netlists generated from both the schematic and its corresponding physical layout. This process permits a circuit at the schematic level to be directly compared with the physical layout to ensure that the connectivity of the circuit netlist has been properly implemented. Furthermore, the desired parameter values are compared to ensure that the physical layout satisfies the specific design criteria. Currently, recognition of design errors with the precision of 1% for junction areas, 2% for shunt and bias resistors, and 10% for significant inductors is permitted.

The verification of a large scale circuit with DRC, ERC, and LVS is performed using the same tools and technology files as for a singe cell; however, the circuit is verified hierarchically, meaning that if a single cell appears in the layout several times, its layout need be verified only once.

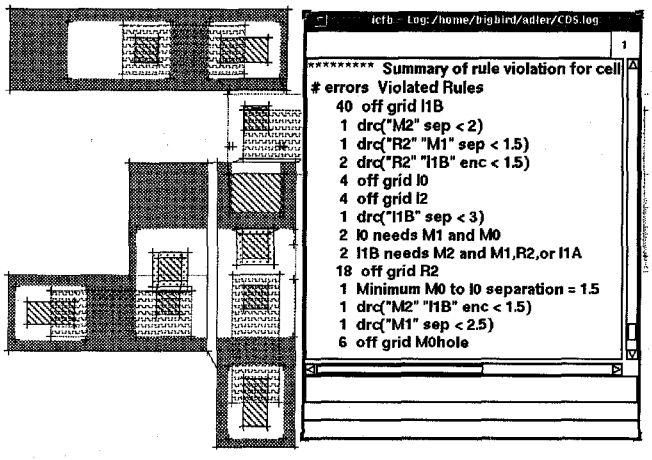

Fig. 5. DRC errors are marked in the layout and explained in the information window.

VI. Results and Conclusions

A top-down design methodology has been presented. The industry standard CAD tool Cadence has been calibrated for a 3 μm superconductive SFQ technology. The design methodology includes Verilog functional simulation, schematic capture, and physical layout. In order to verify the circuit design, tools for behavioral verification, design rule verification, electrical rule checking, and layout-vs.-schematic verification have been calibrated within the Cadence design environment. This design environment has been used successfully on more than 15 basic cells and three large scale SFQ circuits, dramatically reducing the number of errors and significantly improving design efficiency.

Acknowledgments

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