Design for Testability of SFQ Circuits

Gleb Krylov, *Student Member, IEEE*, and Eby G. Friedman, *Fellow, IEEE*

***Abstract*—Test point insertion and set/scan techniques for enhanced testability in superconductive single-flux-quantum (SFQ) logic are proposed here. Test point insertion reduces the overhead of a set/scan chain while maintaining most of the functionality. Multiple ways of replacing costly (in terms of the number of Josephson junctions) SFQ multiplexers with mergers and blocking gates are proposed. The multiplexer control signals are replaced with a gated clock signal or separate bias networks for both functional and test paths. Clocked blocking gates or current-controlled Josephson transmission line segments are used to disable undesired data inputs. The clocked blocking gates for test point insertion in a 64-bit register requires 35% fewer Josephson junctions as compared to multiplexers. This advantage further increases for current-controlled blocking gates. Set/scan chain and test point insertion techniques are applied to several SFQ circuits to evaluate error characteristics and to provide built-in self-test of SFQ-compatible memory systems.**

***Index Terms*—Design for testability (DFT), single flux quantum (SFQ), superconducting integrated circuits, superconductor digital electronics.**

I. Introduction

THE end of CMOS scaling and the advancement of cloud computing applications have led to considerable interest in large-scale superconductive circuits. Rapid single-flux-quantum (RSFQ) logic is a superconductive technology for low-power high-performance cryogenic computing, first introduced in 1985 [1]. In this technology, information is represented as the presence or absence of a magnetic flux quantum in a superconducting loop, consisting of inductors and Josephson junctions (JJs). The movement of a flux quantum through a loop produces a voltage pulse across a JJ, called a single-flux-quantum (SFQ) pulse.

SFQ circuit fabrication and technology development have enabled complex integrated circuits achieving approximately 11 000 JJs for RSFQ digital single processors of practical significance [2] and similar complexity RSFQ prototype microprocessors [3]. Recently, SFQ circuits with regular layout structures such as an ac-biased SFQ shift register used for fabrication process benchmarking reached 800 000 JJs [4]. Subterahertz clock frequencies achievable by SFQ circuits operating in a cryogenic environment make it difficult to generate and externally control test inputs via probing. Prototype testing of these circuits, therefore, requires advanced testing methodologies.

The testability of superconductive electronics, emphasizing defect oriented and structural testing, has been previously considered [5]. The authors discuss possible defects that can be introduced into a circuit during fabrication based on the physical layout and methods to detect these defects. An approach for built-in self-test (BIST) in RSFQ circuits was proposed [6]. In this paper, a different approach is proposed to include a design for testability (DFT) capability within the SFQ logic. Testability features are introduced during the circuit design process, where these features are not dependent on the defect type.

With the complexity and integration of conventional CMOS circuits, multiple automated testing techniques have been developed including BIST and automated test pattern generation (ATPG) [7]. A standard method to insert and control the test inputs and outputs produced by an arbitrarily complex circuit is the use of set/scan chain circuits [8].

Set/scan chains insert and observe information in serially connected flip flops [9]. The sequential circuits are disconnected from the combinatorial logic to form a long shift register through which test patterns are shifted by a clock signal (scan-in phase). After the state of a register is asserted, combinatorial logic is reconnected to produce an output state (capture phase). This output is read from the flip flops by connecting the flip flops into a shift register, and the data are shifted out of the register (scan-out phase). The data are compared with the expected output.

While the full-scan approach provides observability and controllability to all of the flip flops in a chain, set/scan chains also introduce significant overhead. Each flip flop requires a multiplexer as well as additional area for routing. To reduce this overhead, a modified test methodology has been proposed for CMOS-based scan chains, called *test point insertion* [10]. In this methodology, the combinatorial logic is included within the set/scan chain. The multiplexers are replaced with AND or OR gates and placed at the chain boundaries, greatly reducing the overhead of the structure.

Several notable differences between conventional CMOS logic and SFQ logic, however, exist, requiring standard CMOS-based DFT techniques to be modified to support SFQ logic. Traditional CMOS-based set/scan chains rely on a multiplexer to choose between normal operation and set/scan mode operation. In SFQ logic, however, a standard

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The authors are with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY 14627 USA (e-mail: gkrylov@ece.rochester.edu).

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multiplexer requires 14 JJs for each bit [11], as compared to only four transistors in CMOS.

Unlike conventional CMOS logic, SFQ logic gates are inherently clocked and latched. Most SFQ logic gates consist of at least one storage loop. Moreover, each logic stage between sequentially adjacent registers [12] may require several clock cycles to produce an output. The test controller, therefore, needs to be aware of the number of cycles. Distinguishing between the combinatorial logic and the sequential blocks in SFQ logic is, therefore, more complex than in CMOS.

Another issue when applying set/scan chains to SFQ logic is the limited fan-out of the gates and flip flops. The fan-out of a standard SFQ logic gate and flip flop is one. Providing an additional output for a register requires a splitter cell (one splitter for each bit). The test outputs in a set/scan chain should, therefore, be placed sparingly to avoid this significant overhead.

While these issues are disadvantageous for the application of both full set/scan chains and test point insertion, SFQ logic also exhibits certain benefits. The power dissipated by SFQ circuits is extremely small. The additional DFT circuits, therefore, dissipate negligible power.

Test point insertion is, therefore, a preferable method when applying a black box approach to circuit testing, where only the input/output interfaces of a block are controllable. Set/scan chains are preferable when each logic stage is overly complex to ensure optimal coverage while only controlling the circuit interfaces.

In Section II, several SFQ specific modifications for the DFT are proposed. In Sections III and IV, these improvements are applied, respectively, to the test point insertion technique and set/scan chains. In Section V, the results are summarized.

II. Reducing DFT Overhead

The pulse-based nature of SFQ logic provides inherent isolation of the inputs from the different sources of data: if two outputs are connected to one via through a confluence buffer (CB), and no pulses arrive at one of the inputs (logic zero), the logic element functions correctly with only one input without requiring additional multiplexing circuitry. As a CB only requires five JJs as compared to 14 JJs for a typical multiplexer, a CB is preferable for test point operation. In the following subsections, several methods for replacing multiplexers with CBs are proposed.

A. Replacing the Multiplexers

To replace the multiplexers with CBs, it is necessary to ensure that no input pulses arrive at an inactive port of a CB. One method to ensure the absence of an input signal is to terminate any upstream signal generation by turning OFF the logic elements feeding data to the circuit under test (CUT). For the test path, this capability is achieved by a test controller, which supplies predefined test vectors during the test mode and supplies logic zero during normal circuit operation. A regular logic path is, however, more difficult to turn OFF. When the controller initiates the test mode, the outputs of the upstream logic should be turned OFF to prevent these signals from affecting the test vectors. This capability requires test modes to disable the outputs from the upstream logic and introduces significant overhead. Furthermore, the test inputs cannot be inserted at arbitrary nodes within a logic path, and the test modes are not utilized during normal circuit operation.

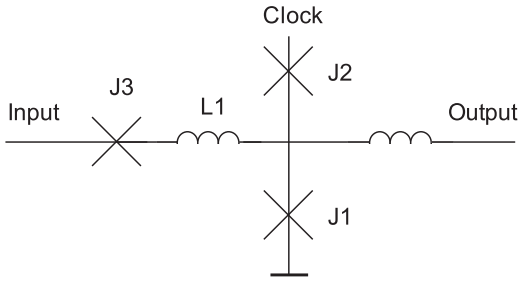

Fig. 1. DFF as a clocked blocking gate.

Another method of disabling an undesired data path is to use special blocking gates that block an incoming signal or allow the signal to further propagate based on certain control signals. Multiple methods can be used to achieve this capability, where the choice depends upon the controller and circuit complexity. This approach, while also requiring considerable overhead, relaxes the requirements on the upstream logic, allowing a test input to be inserted at any point within a logic path.

B. Blocking Gates

In the following subsections, several possible forms of blocking gates are proposed. These gates can be divided into two groups based on the control signal: clocked or current controlled.

1) Clocked Blocking Gate: This type of blocking gate is depicted in Fig. 1. This gate, essentially a D flip flop (DFF), consists of a decision making pair [13] combined with an auxiliary escape junction at the data input. All of the JJs are shunted, where the Stewart–McCumber parameter [14] β_c is set to 1. Depending upon the persistent current within the J3-L1-J1 loop, the arriving clock pulse either produces a 2π phase change in J2, leading to the absence of an SFQ pulse at the output, or triggers an output SFQ pulse by producing a 2π phase change in J1. Escape junction J3 prevents the blocking gate from being switched by two consecutive input pulses without a clock pulse. In this case, J3 initially switches, preventing a 2π phase change in J1. An output pulse is, therefore, not produced.

When the clock input is first enabled after the test mode is initiated, a flux quantum may be present within the J3-L1-J1 loop. In this case, the flux quantum will escape and produce an output pulse, which should be discarded. While this spurious output can be detrimental when the gate is used in logical operations, for DFT purposes, this pulse only extends the test mode by one clock cycle and, therefore, has a negligible effect on the test operation.

The clocked blocking gate is combined with each bit of the normal data path and is enabled by a clock signal. This clock is gated during the test mode. When the clock is enabled at this gate, the data path is transparent to any incoming SFQ pulses.

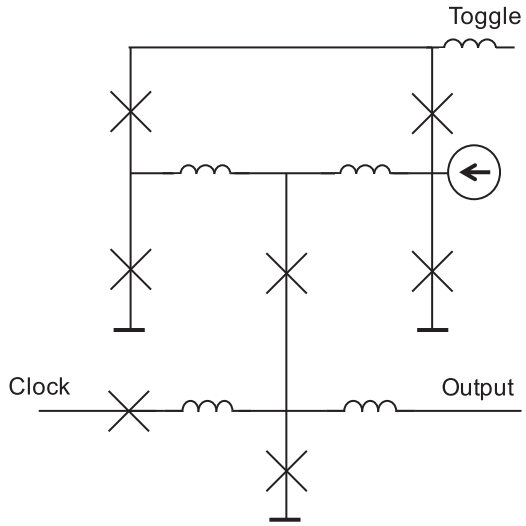

Fig. 2. NDRO T flip flop.

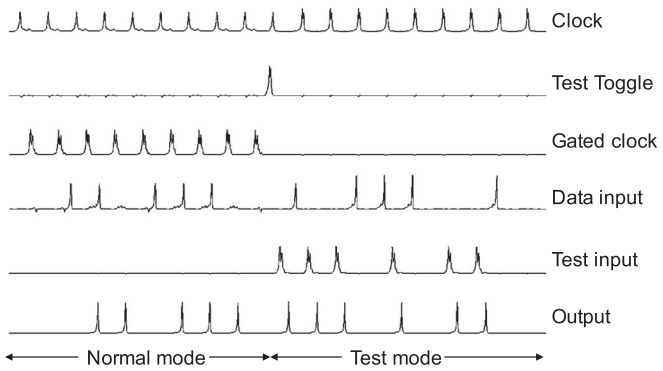

Fig. 3. Waveforms illustrating multiplexer operation performed by a blocking gate and a merger.

When the clock is disabled, no output is produced. The gated clock train can be produced by a nondestructive readout (NDRO) T flip flop attached to a clock output. Alternatively, an NDRO DFF can be used. An NDRO T flip flop is shown in Fig. 2 and consists of a T flip flop and an NDRO DFF [11].

With a T flip flop toggle input, the circuit switches between the functional and test modes. A clock signal passes from a nearby register through an SFQ pulse splitter. The clock skew between the upstream logic and the blocking gate can be tuned to minimize the delay introduced by the blocking gate during normal operation [15], [16].

The temporal behavior of the combination of a clocked blocking gate with a merger is shown in Fig. 3. The circuit evaluated in this simulation is shown in Fig. 4. Correct multiplexing of data and test inputs is achieved, provided no signals originate from the test controller when not operating in the test mode. By attaching clocked blocking gates to both inputs of the merger, the full functionality of a multiplexer is duplicated independent of the data inputs while requiring only 11 JJs.

2) Current-Controlled Blocking Gates: Another possible method for a blocking gate is to reduce the bias current of the input JTL in front of the CB, thereby preventing propagation of an incoming SFQ pulse. This method requires a controllable

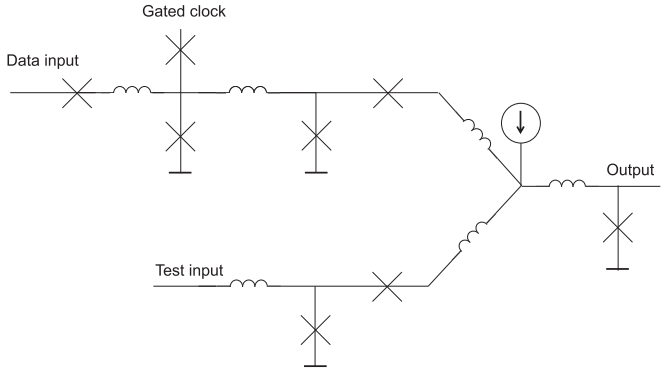

Fig. 4. Combination of a clocked blocking gate and a merger used for test point insertion.

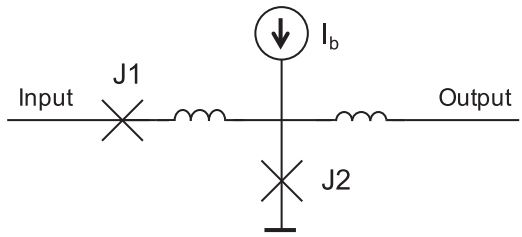

Fig. 5. Current-controlled blocking gate.

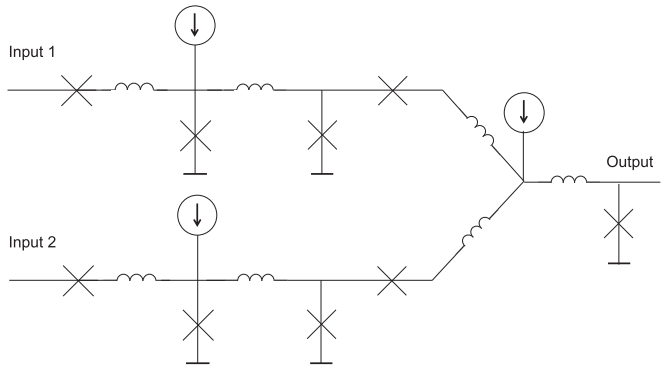

Fig. 6. Multiplexer composed of two current-controlled blocking gates and a CB.

current, either provided by a source within the test controller or supplied externally. A blocking gate for this method is shown in Fig. 5. The current I_b controls the bias conditions of junction J2. When this current is low, J1 is closer to switching, allowing an incoming input pulse to switch J1, producing no output. When I_b is high, however, J2 is closer to switching, and the input pulse propagates along the path. The combination of two blocking gates and a CB, shown in Fig. 6, can multiplex two inputs depending upon the control current. Waveforms describing the operation of this circuit are shown in Fig. 7.

The primary benefit of this approach is greatly reduced area, since no additional circuitry is required within the chain other than the blocking gate shown in Fig. 5. Two separate bias distribution networks for both the functional and test paths with the ability to control the bias current are, however, required. The externally supplied current also requires additional pins to control the different test points and set/scan chains. Alternatively,

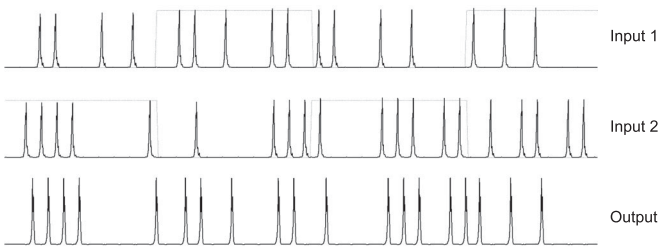

Fig. 7. Waveforms illustrating multiplexer operation performed by a current-controlled blocking gate and a CB. The bias current levels are shown as dotted lines overlapping the corresponding channel inputs.

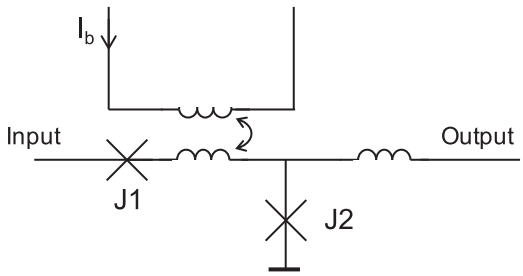

Fig. 8. Current-controlled blocking gate with inductively coupled flux bias [17].

the bias current can be generated and controlled internally by other SFQ circuits by supplying stored current from the NDRO flip flops to the blocking gates.

A similar method inductively couples the flux bias into the JTL input loop. An inductor inside a JTL segment is coupled to a controlled bias line. When a current is supplied through this line, additional magnetic flux is introduced into the loop, which can, depending upon the direction, either prevent or assist the propagation of an incoming SFQ pulse by bringing either J1 or J2 closer to switching. The blocking gate for this method is depicted in Fig. 8.

In the following two sections, both test point insertion and set/scan chain techniques are discussed. The proposed SFQ specific methods for reducing the overhead are demonstrated on these two DFT techniques.

III. Test Point Insertion for SFQ Circuits

A modified test point insertion method targeted to SFQ circuits is described in this section. This method utilizes test inputs and outputs along the most error prone critical logic paths or those logic paths where a black box testing approach is adequate. The test path contains both registers and logic gates; thus, correct operation of the combinatorial logic can be verified. By sparingly placing the test inputs and outputs, the overhead of the test circuits is reduced as compared to a set/scan chain. As these test points are inserted only at the input/output interfaces of the CUT; however, it is more difficult to modify the internal state of the CUT and achieve complete coverage.

The overall structure of the proposed method is schematically shown in Fig. 9. At the input, the CBs combine a normal data path with the test data path. Normal operation is disabled by a clocked blocking gate, as described in the following section. The test output consists of SFQ pulse splitters at the output of the CUT.

A. Test Process

After blocking the normal data path, the CUT is supplied with test vectors. These vectors are chosen to provide sufficient coverage of the circuit functionality [9]. As each logic element requires multiple clock cycles to process the entire set/scan chain, the timing characteristics are included within the expected result by adding the correct number of clock cycles between output data.

The precise implementation of the test controller largely depends upon the complexity of the CUT. Depending upon the complexity of the test controller, the test controller can either include predetermined test vectors or the test vectors can be supplied by an external BIST/ATPG controller. Similarly, the output for the predetermined test vectors can be either stored on-chip in a ROM or stored externally. For current SFQ circuits, an on-chip controller is unfeasible due to the large overhead. To reduce the number of pin outs required by the DFT in the case of an external controller, serial shift registers can load the test vectors and read out the results.

After the CUT produces a set of output responses for a set of input test vectors, the output response is passed to the test controller using splitter gates and transmission lines. These signals are compared with the expected results from the controller. Alternatively, the outputs can be compared off-chip.

B. Comparison to Multiplexers

Test point insertion in SFQ can be achieved with multiplexers. The proposed blocking gates are compared here to a multiplexer. The number of required JJs is used as a crude estimate of the total circuit area overhead, while clocking and routing overheads are assumed to be similar.

An SFQ multiplexer consists of 14 JJs switched by set/reset inputs [11]. The SFQ pulse mergers are combined with clocked blocking gates, requiring fewer JJs for the gates, and only one control signal for the clock with $\log_2 n$ splitters (as opposed to two networks, set and reset, required by a multiplexer).

The following expressions describe the number of JJs required for each test point as a function of the data bus width. The number of required junctions J_m if regular multiplexers are used is

$$J_m = (M + S) * n + 2S * \log_2(n). \tag{1}$$

The number of required junctions J_c by the clocked blocking gates and CBs is

$$J_c = (B_1 + C + S) * n + S * \log_2(n) + T + S. \tag{2}$$

The number of required junctions J_b for the current-controlled blocking gates and CBs is

$$J_b = (B_2 + C) * n, \tag{3}$$

where n is the width of a data path, M is the number of JJs in a multiplexer gate, and S and C are, respectively, the number of JJs in a splitter and CB. T is the number of JJs in an NDRO T flip

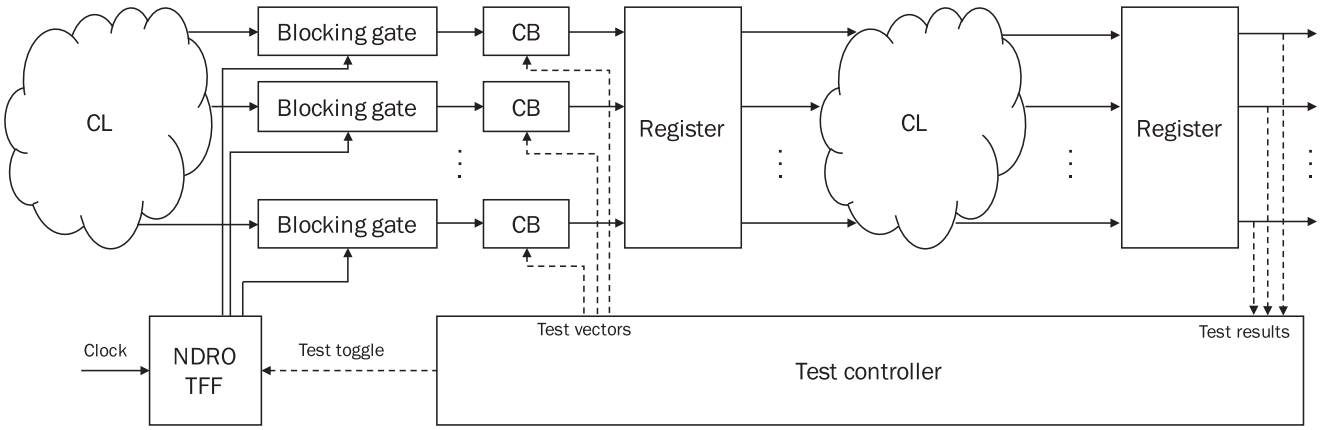

Fig. 9. Proposed test point insertion method. The dashed lines are active connections during the test mode. A test point consists of blocking gates and a CB (similar to the circuits shown in Figs. 4 and 6) on every bit of a data path. In this figure, the clocked method is depicted, where the blocking gates are supplied with a regular clock signal. This clock signal is gated by an NDRO T flip flop controlled by a test controller.

TABLE I
NUMBER OF JUNCTIONS PER FUNCTION; SEE (1)–(6) [11]

Parameter	Description	Number of JJs
M	Multiplexer	14
S	Splitter	3
B_1	Clocked blocking gate	3
B_2	Current-controlled blocking gate	2
C	Confluence buffer	5
T	NDRO T flip flop	7
I	Inverter	5

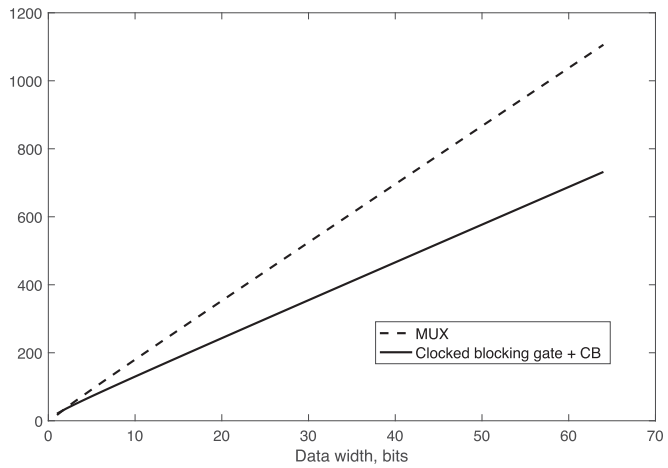

Fig. 10. Number of junctions in clocked blocking gates and CBs as compared to multiplexers for different data widths.

flop. B_1 and B_2 are, respectively, the number of JJs in a clocked blocking gate segment and a current-controlled blocking gate. The number of JJs for each of these gates is listed in Table I.

A comparison of the number of JJs required by the multiplexers and clocked blocking gates for increasing bus width is shown in Fig. 10. The advantages of the proposed technique increase with wider data paths. For a 64-bit register, the use of multiplexers for test point insertion requires 1,124 JJs, while the use of clocked blocking gates requires only 732 JJs, a 35% improvement. With current-controlled blocking gates, this overhead is further reduced to only 448 JJs.

C. Advantages and Disadvantages of Test Point Insertion

As compared to the traditional set/scan chain approach widely used in CMOS, this technique does not place data in arbitrary registers, restricting the set of testable circuits. As there is no requirement for a circuit to be synchronous, however, this technique can also enhance testability in asynchronous and wave-pipelined systems [18], [19]. Multiple logic stages between registers are not bypassed, requiring changes in the input data to provide sufficient coverage. As this method involves sequential test pattern generation, similar to CMOS, considerable computational resources are required to choose an optimal set of test vectors and to determine the expected outputs, particularly with those logic paths that contain feedback [20].

IV. SET/SCAN CHAINS FOR SFQ CIRCUITS

The test point insertion method can be logically extended to complete set/scan chains. As compared to test point insertion, a complete set/scan chain adds a separate path for the test data along the regular data path, requiring a multiplexer with each register. While this approach adds overhead and complexity, set/scan chains also provide numerous benefits: specifically, the ability to set and read each register in a chain and enhanced fault coverage of the logic gates, making set/scan chains effective in locating the precise source of an error.

Modification of test point insertion for complete set/scan chains is shown in Fig. 11. For each logic block in a chain, an alternative path through a JTL is introduced. Regular SFQ multiplexers or a combination of blocking gates and CBs choose between inputs. Blocking gates are placed on both the regular and test inputs of a CB, effectively forming a multiplexer. The blocking gates are switched by complementary control signals. Whenever one input is enabled, another input is disabled. In Fig. 11, clocked blocking gates are used as blocking gates to depict the additional circuitry required to produce the complemen-

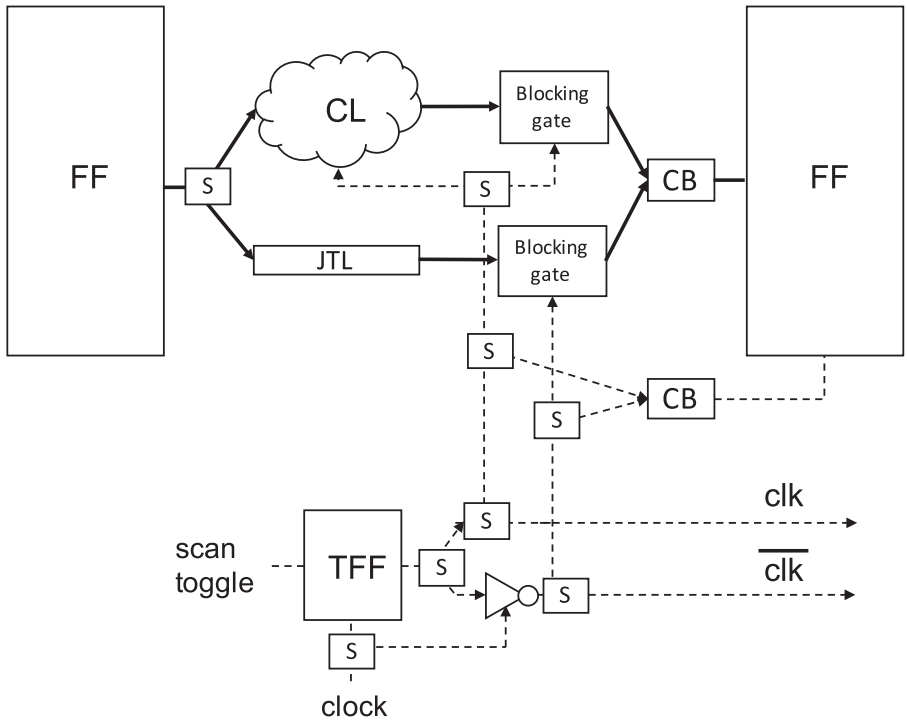

Fig. 11. Set/scan chain insertion method. The blocking gates are realized as clocked blocking gates. A T flip flop and inverter generate complementary clock signals, clk and $\overline{clk}$. At any time, only one of the logic paths is active—either regular (upper) or set/scan (lower). The data connections are shown as bold lines, and the control signals are shown as dashed lines.

tary clock signals. Utilization of clock signals as control signals reduces the overhead as compared to the separate control signals required by the multiplexers. Clock distribution networks for clocked blocking gates can be reused by combinatorial logic or flip flops, as shown in Fig. 11. If current-controlled blocking gates are used, the complementary clock distribution networks are replaced with two bias distribution networks—one network for the normal data path and one network for the test path.

Similar to (1)–(3), each register in a set/scan chain using multiplexers requires J_m junctions, which is a function of the data bus width,

$$J_m = (M + S) * n + 2S * \log_2(n). \tag{4}$$

For set/scan chains using blocking gates and CBs, J_c junctions are required per register, which are given by

$$J_c = (2B_1 + C + S) * n + 2S * \log_2(n) + 2S + T + I. \tag{5}$$

For scan chains using current-controlled blocking gates and CBs, J_b junctions per register are required, which are given by

$$J_b = (2B_2 + C) * n, \tag{6}$$

where n is the width of the data path. The total number of junctions of a set/scan chain is scaled by the length of the chain. For this technique, current-controlled blocking gates further lower the overhead.

The primary issue with set/scan chains for SFQ is that each logic gate is typically clocked. Each logic block requires an arbitrary number of clock cycles to execute. While this behavior does not affect the scan-in and scan-out phases, the capture phase is further complicated. It is, therefore, desirable to insert set/scan chains into the normal logic paths, where each stage requires the same number of clock cycles.

V. Conclusion

Applications of test point insertion and set/scan chain techniques for SFQ circuits are proposed. These applications are compatible with the RSFQ logic family and energy-efficient modifications [21]. While both test point insertion and set/scan chains can use multiplexers, the number of required JJs can be greatly reduced by substituting multiplexers with CBs and blocking gates.

Test point insertion can be used to evaluate critical and error-prone logic paths and is particularly useful for testing complex operations on wide data buses. In addition, this method can be used with a memory BIST controller with negligible overhead to provide access to the address, data, and control lines within a memory block. As the internal structure of the circuit is not modified, and synchronization is not required to operate correctly, test point insertion is also applicable to asynchronous and wave-pipelined circuits. Set/scan chains can be used for those circuits where fine control of the data within the registers is desired.

Acknowledgment

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Gleb Krylov, (S'16) received the Specialist degree in computer engineering from the National Research Nuclear University MEPhI, Moscow, Russia, in 2014, and the M.S. degree in electrical engineering from the University of Rochester, Rochester, NY, USA, in 2017, where he is currently working toward the Ph.D. degree.

He was a Hardware Verification Engineer with Moscow Center of SPARC Technologies from 2012 to 2014 and then with Baikal Electronics, Moscow, from 2014 to 2015. In 2017, he interned with Hypres Inc., Elmsford, NY, USA. His current research interests include superconducting digital electronics and electronic design automation.

Eby G. Friedman, received the B.S. degree from Lafayette College, PA, USA, in 1979, and the M.S. and Ph.D. degrees from the University of California, Irvine, CA, USA, in 1981 and 1989, respectively, all in electrical engineering.

From 1979 to 1991, he was with Hughes Aircraft Company, rising to the position of Manager of the Signal Processing Design and Test Department, responsible for the design and test of high performance digital and analog IC's. He has been with the Department of Electrical and Computer Engineering, University of Rochester since 1991, where he is a Distinguished Professor, and the Director of the High Performance VLSI/IC Design and Analysis Laboratory. He is also a Visiting Professor at the Technion - Israel Institute of Technology, Haifa, Israel. His current research and teaching interests include highperformance synchronous digital and mixed-signal microelectronic design and analysis with application to high speed portable processors, low power wireless communications, and high performance server farms. He is the author of more than 500 papers and book chapters, 13 patents, and the author or editor of 18 books in the fields of high speed and low power CMOS design techniques, 3-D design methodologies, high speed interconnect, and the theory and application of synchronous clock and power distribution networks.

Dr. Friedman is the Editor-in-Chief of the *Microelectronics Journal*, a Member of the editorial boards of the *Journal of Low Power Electronics* and *Journal of Low Power Electronics and Applications*, and a Member of the technical program committee of numerous conferences. He previously was the Editor-in-Chief and Chair of the steering committee of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, the Regional Editor of the *Journal of Circuits, Systems and Computers*, a Member of the editorial board of the Proceedings of the IEEE, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: ANALOG AND DIGITAL SIGNAL PROCESSING, IEEE *Journal on Emerging and Selected Topics in Circuits and Systems*, Analog Integrated Circuits and Signal Processing, and the *Journal of Signal Processing Systems*, a Member of the Circuits and Systems (CAS) Society Board of Governors, Program, and Technical Chair of several IEEE conferences, and received the IEEE Circuits and Systems Charles A. Desoer Technical Achievement Award, the University of Rochester Graduate Teaching Award, and the College of Engineering Teaching Excellence Award. He is a Senior Fulbright Fellow and an IEEE Fellow.