Interconnect Routing for Large-Scale RSFQ Circuits

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***Abstract*—The increasing complexity of modern rapid single flux quantum (RSFQ) circuits has made on-chip signal routing, an issue of growing importance. In this paper, several methods for routing large-scale RSFQ circuits are described, and a process is presented for determining when to use passive microstrip transmission lines (PTL) and active Josephson transmission lines (JTL). The effect of the size of the JTL inductor and Josephson junctions on the length of a JTL chain for a target delay is also discussed. The dependence of the JTL inductance on the physical layout is evaluated, and the effects of the primary PTL parameters on delay are characterized. A novel PTL driver and receiver configuration is also proposed. Tradeoffs among the number of JJs, inductance, and length of a PTL stripline in the receiver and driver circuits are reported. The energy dissipation is evaluated for two different interconnects. A tradeoff between the proposed PTL circuits and an optimized JTL in terms of energy dissipation and delay is discussed. Guidelines for choosing the optimal element values are determined, and a simulated bias margin of $\pm$ 29% for the bias current of the proposed receiver operating at 20 GHz in a 10 kA/cm^2 technology for a 1-mm transmission line is achieved. Summarizing, guidelines and design tradeoffs appropriate for automated layout and synthesis are provided for driving long interconnect in SFQ VLSI circuits.**

***Index Terms*—Single flux quantum, superconducting integrated circuits, superconductive digital electronics.**

I. Introduction

RECENT developments in very large scale rapid single flux quantum (RSFQ) superconductive circuits target high performance, energy efficient computing. In this cryogenic technology, information is represented in the form of picosecond voltage pulses with quantized area, called single flux quantum (SFQ) pulses.

With only a modest number of researchers worldwide, significant progress has been achieved in enhancing RSFQ circuit performance and operational frequencies [1]. Complex RSFQ circuits have been experimentally tested [2], and high operating clock frequencies in microprocessors [3], [4] and network switches [5] beyond 20 GHz [6] have been successfully demonstrated. RSFQ digital RF receiver circuits with tens of thousands of Josephson junctions (JJ) have been experimentally verified up to an operating frequency of 30 GHz [7]. Furthermore, recent progress in SFQ manufacturing processes has resulted in device densities of over 600,000 JJ/cm^2 [8]. Combined with recent efforts to develop EDA tools for superconductive electronics [9], [10], the complexity of RSFQ circuits is expected to greatly increase. Current *ad hoc* practices in many stages of the SFQ circuit design process need to be replaced with quantitative guidelines. Automated layout and clock tree synthesis (CTS) are examples of these practices, where methodologies for signal and clock routing are currently not well established.

While general synchronization principles and techniques commonly used in CMOS are applicable to SFQ technology, several notable differences exist. Sub-terahertz clock frequencies and pulse-based logic in SFQ present unique challenges for providing an accurate and stable clock signal [11]. One of the primary concerns of automated layout and CTS in conventional integrated circuits is the interconnect characteristics. Different interconnect methodologies require different types of interconnect. SFQ-based automated layout and clock tree synthesis tools require guidelines to determine the optimal interconnect structure for each line. Furthermore, in a standard cell flow, the optimal configuration of the driver and receiver needs to be determined for the interconnect lines. For signal propagation within the interconnect between RSFQ gates, Josephson transmission lines (JTL) or passive transmission lines (PTL) are typically used [12].

A JTL is an active interconnect, which can transfer an SFQ pulse without reflections, providing noise discrimination by regenerating the pulse at each stage. Utilization of JTLs for long wires, however, increases the propagation delay and power consumption due to the added Josephson junctions.

A PTL consists of a passive stripline with an active driver and receiver. SFQ pulses ballistically propagate along a PTL at the speed of light within the medium. The PTL delay therefore scales linearly with length. For long lines, it is therefore desirable to use PTLs rather than JTLs, as a PTL only requires active JJs in the driver and receiver. Furthermore, the power consumed by a PTL line is independent of length [13]–[15]; thus, less power is consumed in long lines. Unlike JTL interconnect, a PTL offers greater flexibility and less routing congestion [16].

Since the delay of a PTL only depends on the length of the line and not the capacitance, and the pulse propagation speed in

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PTLs approaches the speed of light, standard CMOS-like techniques [17], [18] are likely to be inefficient in superconductive electronics. If necessary, pulses can be delayed by inserting JTL segments into the signal and clock lines.

In this paper, SFQ interconnects are described in Section II. The effect of linewidth on the interconnect structures, PTL and JTL, is discussed, respectively, in Section II and III. The dependence of the JTL inductance on the physical layout is also described in Section II. Different PTL driver and receiver circuit configurations are presented in Section II to provide guidelines for driving long interconnect. A novel PTL receiver is introduced in Section III. Furthermore, the physical characteristics of a PTL stripline when inserting a repeater (driver/receiver pair) or a JTL segment are also discussed in Section III. The paper is concluded in Section IV.

II. SFQ Interconnect

The propagation of SFQ pulses plays an important role in the performance of complex RSFQ circuits. Two different components are used for SFQ interconnect: active Josephson transmission lines and passive transmission lines. Each SFQ interconnect type is described in this section. Properties of the interconnects such as delay for a constant length, physical area, energy dissipation, and reflections determine when to use PTL and JTL interconnect. The properties of the Josephson transmission line interconnect and the effect of the JTL linewidth on area are discussed in Subsection II-A. Utilization of standard PTLs in VLSI oriented SFQ circuits, and the effects of different number of JJs and receiver inductance are discussed in Subsection II-B.

A. Josephson Transmission Lines

Josephson transmission lines are typically used as basic cells to connect RSFQ gates. A JTL is typically composed of uniformly sized Josephson junctions with uniform inductances L between junctions. Consequently, the length and area of a JTL within a standard cell library only change in terms of the number of stages. In this subsection, the length and area of a JTL for different number of stages are described for different line widths of the the niobium (Nb) inductor, where the inductance parameters are based on MIT Lincoln Laboratory SFQ5ee design rules [19], [20]. The geometric parameters, such as the shape of the Josephson junction layout (orientation of the shunt resistor) and the width of the inductor, affect the area of a JTL. Two different layouts of a JJ with an external shunt resistor are shown in Figure 1. A straight line layout is assumed for the shape of a JTL for all shunt resistors and inductors, as shown in Figure 1(a). Increasing the linewidth of the stripline affects the length and area of the JTL. The area of a standard cell-based circuit in an active layer can be decreased by utilizing bends in the layout of the superconductive inductors and JJs (see Figure 1(b)). By maintaining a constant inductance and increasing the linewidth, the length of a stripline and JTL increase. A constant inductance with two different linewidths and layout with the same JJs within a JTL produces the same output delay. The dependence of the area, length, and delay of a JTL on inductance is discussed below.

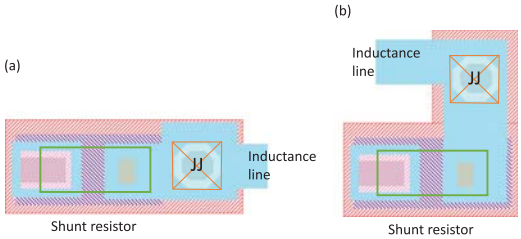

Fig. 1. Layout of a Josephson junction with a shunt resistor: (a) straight line, and (b) bent line.

Consider a linewidth of a JTL inductor ranging from 350 nm to 1 μm (see Figure 1). The length and area of a JTL are, respectively, on the order of 20 to 32 μm and 55 to 80 μm^2 for one JTL stage. The inductance L between stages is 2 pH. The minimum linewidth is 350 nm, based on SFQ5ee design rules, while the maximum linewidth depends upon the JTL layout, and is chosen, somewhat arbitrarily, to be 1 μm.

The delay of a JTL with two JJs ($I_C = 250$ μA) is about 5 ps. The delay of a chain of JTLs increases linearly with the number of JTLs. For a constant inductance and therefore constant delay, the length and area of the JTL significantly increase with wider inductors.

As a JTL consists of actively switching JJs in the top layer, JTL-based SFQ interconnect consumes additional area, power, and delay. Although not a significant issue in current medium scale integration RSFQ circuits, the greater area, power, and delay pose a significant challenge in future RSFQ VLSI circuits. To lower the area, power, and delay in large scale circuits, PTLs are used to connect RSFQ gates.

B. Passive Transmission Lines

Utilizing PTLs rather than JTLs in long lines reduces the output delay, power consumption, and active area in the top layer. The primary parameters of a PTL line and the effects of these parameters on delay are characterized here. A typical PTL consists of a superconductive stripline, one JJ, and a small inductance in the driving circuit, and two JJs with a small inductance in the receiving circuit [21]. For these topologies, the limits of usefulness of PTL and JTL wiring are discussed. The parameters affecting the pulse propagation characteristics are the bias current, size of the internal inductance, number and size of the JJs, and length and width of the stripline between the driver and receiver.

The number of bias points for a PTL driver and receiver depends upon the number of JJs in these circuits. By using three bias current sources for a typical PTL driver and receiver, additional area and energy dissipation are introduced into the bias network. Decreasing the number of JJs and the linewidth of the inductor and interconnect within a PTL receiver reduces the area of the PTL interconnect as well as the delay.

III. Novel SFQ PTL Driver/Receiver

A topology for PTL interconnect in a 10 kA/cm^2 technology is proposed in this section. The proposed PTL circuits are shown in Fig. 2. An extra driver circuit is removed from the proposed

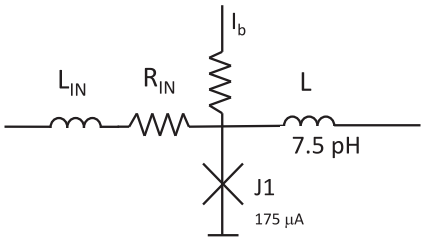

Fig. 2. Proposed receiver circuit.

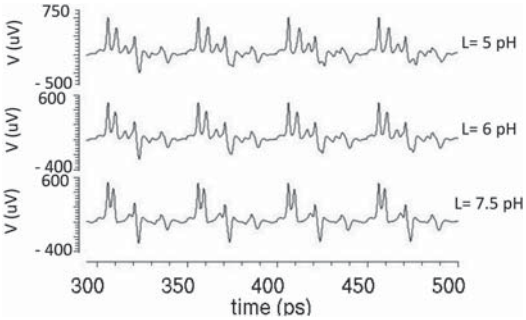

Fig. 3. Reflection of the receiver for different inductances.

configuration. The last JJ of the driving gate/cell connected to a PTL line drives an SFQ pulse onto a PTL line. The PTL driver consists of the JJ of the previous RSFQ gate and a small parasitic inductance due to the via between the active JJ layer and the routing layer, and no additional Josephson junctions. The PTL receiver consists of one JJ with a Stewart-McCumber parameter (β) [22] corresponding to a slightly underdamped state and a large inductance. The input inductor in the receiver is a parasitic inductance due to the via from the logic gate layers to the PTL routing layer. A transmission line with a stripline topology exhibits an impedance in the range of 8 to 12.5 ohms and a linewidth ranging from 3.6 to 2.2 μm (assuming a straight line structure) [23]. The driver and receiver provide sufficient signal power and impedance matching between the PTL and the load at 20 GHz. Removing the JJ in the driver decreases the output delay, area, and energy dissipated by the PTL, while degrading the matching characteristics. A larger β improves the impedance matching characteristics and raises the amplitude of the SFQ voltage pulse. Furthermore, a large inductance and input resistor within the receiver improve the impedance characteristics while lowering reflections and increasing the delay. The effect of the inductance on the reflection characteristics are illustrated in Figure 3. In the proposed PTL receiver, the effect of the large inductance on delay is shown in Figure 4. A larger inductance increases the delay. The preferable inductance to lower reflections for the proposed receiver is 7.5 pH.

The input resistor in the receiver dissipates additional energy within the PTL. The energy dissipated by the proposed PTL is described in Subsection III-A. The number and size of the JJs in the PTL affect the output delay and physical characteristics of the interconnect. The effects of the proposed topology on area and delay are discussed in Subsection III-B. The properties of the PTL interconnect described in this section and the JTL described in Section II determine when

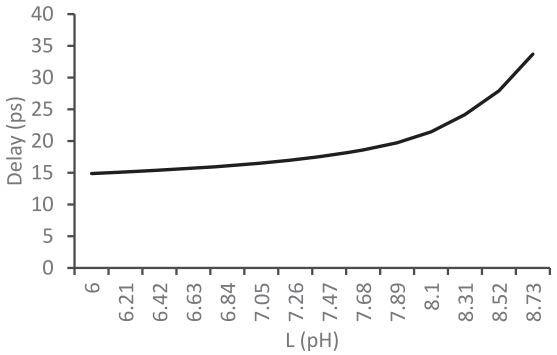

Fig. 4. Effect of inductance on propagation delay.

to use a PTL or JTL. The input inductance affects the bias margins of the PTL. Furthermore, the input resistor within the receiver causes a negligible drop in the bias margins. Margins for the different PTL interconnect types are discussed in Subsection III-C.

A. Energy

Resistors are typically inserted into a PTL to improve the matching characteristics, prevent current redistribution and flux trapping in long superconductive loops, and provide additional damping for signal reflections. The resistors in a PTL, however, also reduce the signal power available at the receiver, and dissipate additional energy. In the operational range of resistances, the maximum dissipated energy in the PTL resistors is approximately $10^{-19}J$ per SFQ pulse, five times lower than the switching energy of $\Phi_0 \times I_C = 5.17 \times 10^{-19}$ J for a 250 μA Josephson junction. The resistive energy dissipation is therefore negligible and can be ignored when selecting between a PTL and a JTL. The energy of a PTL, composed of an ideal transmission line, input resistor, and one JJ, is approximately 6×10^{-19} J. The PTL line exhibits a constant energy independent of length. The energy of a JTL, composed of two JJs, is approximately 10×10^{-19} J. The energy of a chain of JTLs increases linearly with the number of JTLs.

B. Length and Area of Interconnect

The effect of two different PTL receiver topologies (two JJs and one smaller inductance, and one JJ and a large inductance) on the length and delay of the interconnect is compared to the JTL interconnect shown in Figure 5. The length of the driver and receiver within the proposed PTL and a typical PTL in the active gate layer are, respectively, 19 and 40 μm. The length of the line within the routing layer is dependent upon the distance between the two gates. The minimum length of the proposed PTL interconnect including the vias, receiver, and routing line is 21 μm. The minimum length of a single stage JTL within the active gate layers is about 20 μm. In Figure 5, the delay of both PTL interconnects is the propagation delay of a PTL line and the input-to-output delay of the receiver and driver. The delay of the proposed PTL and JTL is, respectively, about 8 and 5 ps. For a complex RSFQ circuit, automated routing and CTS algorithms need to choose between different interconnect types, depending

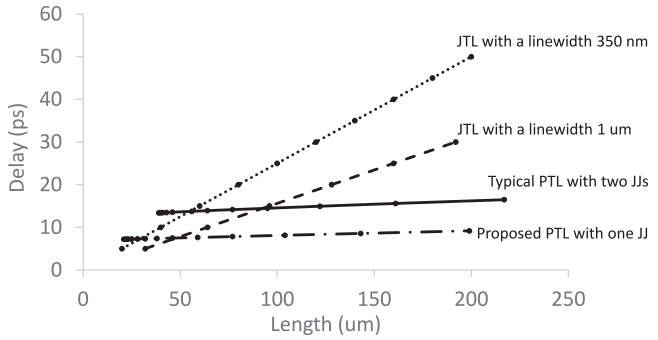

Fig. 5. Delay vs. length of JTL with a linewidth of 350 nm (dotted line) and 1 μm (dash line), and typical PTL with two JJs (solid line) and proposed PTL with one JJ (dash-dotted line) in the receiver.

upon the physical characteristics of the interconnect within the active gate (JJ) layers or the routing layers. The PTL interconnect requires the length and area on both the JJ layer and the routing layer. The JTL interconnect only exhibits an area overhead in the JJ layer. Congestion in the routing layer, when space within the cell layers is available, can make a JTL the preferable choice for interconnect despite the greater area and power overhead.

The area of the proposed PTL in the active gate layer can be reduced by removing the JJ in the driver and the number of JJs and bias current in the receiver. The area of the PTL line in the routing layer is dependent upon the length of the PTL. The minimum area of the PTL in the routing layer is on the order of 4 to 25 μm^2 for a linewidth ranging from 2 to 5 μm. Considering the minimum length of a PTL in the routing layer and the area of the driver and receiver in the active gate layer, the area of the proposed PTL is about 40 to 60 μm^2 for two different PTL linewidths in the routing layer, 2 and 5 μm. The minimum area of a typical PTL is about 80 to 100 μm^2.

By lowering the overhead of the driver/receiver circuits, a PTL can more effectively drive a shorter line. The proposed PTL exhibits a lower delay for the same area for long interconnect. Unlike typical PTL circuits, the proposed circuit requires only one bias current source. This feature reduces complexity and the area of the bias network.

The delay of a typical PTL is less than the delay of a JTL for long interconnect. For short interconnect, however, the PTL requires greater area than a chain of JTLs. For a very short line, a JTL with a 350 nm linewidth requires less area with the same delay as compared to both a JTL with a 1 μm linewidth and a standard PTL. For the same interconnect length, the proposed PTL exhibits a lower delay.

C. Margin

A margin analysis to determine the optimal parameters is discussed in this subsection. The parameters that affect the bias margins include the input impedance of the receiver, the length of the transmission line, the impedance of the transmission line, and the RSFQ gate connected to the PTL. The simulated bias margins of a PTL with one JJ and two JJs in the receiver are, respectively, approximately 29% and 12% for a 1 mm transmission line in a 10 kA/cm^2 technology, where the PTL is connected to the JTL buffers on both sides. The margins of the proposed receiver are larger than the margins of a standard PTL with two JJs in the receiver for all lengths, despite the larger inductance in the receiver. The delay increases with a larger inductance in the receiver. The current bias margins depend upon the input impedance of the receiver including the effects of the JJ and inductance when the inductance is in the range of 5 to 8.5 pH. The delay with a smaller inductance in the proposed receiver is about 8% less than a large inductance for the same bias current. By increasing the inductance, the impedance matching characteristics are enhanced.

The proposed driver/receiver configuration exhibits good margins when connected to the JTL stage on both sides, exploiting the notion that standard cell libraries often include JTL buffers at the input and output of the standard cells. Nevertheless, this analysis can be overly optimistic, as a JTL itself behaves as a buffer element, further improving the margins.

The bias margins of the proposed PTL configuration are therefore further evaluated by connecting a PTL to a D flip flop (DFF). Due to reflections between the PTL and the DFF output, the delay of the receiver increases and the bias margin of the receiver decreases. The bias margins of a PTL directly connected to a DFF are approximately -10%, $+29\%$. To improve the bias margins, a single JJ and bias current source (half of a JTL stage) can be placed after the DFF. This stage decreases the load on the PTL line and lowers the reflections, while increasing the delay and area. With this added stage, the bias margins are approximately -23%, $+28\%$.

The proposed PTL line is also connected to an OR gate to determine the margins of the proposed PTL when used for routing between logic gates. Significant reflections occur when connected directly to an OR gate that can cause the circuit to not function properly. The bias margins of the proposed PTL with a single buffer JJ at the output of the OR gate are approximately -21%, $+29\%$ with low reflections at the output of the OR gate. Using two JJs as a buffer instead of one JJ produces slightly better margins, but significantly greater area and delay.

IV. Conclusion

Different routing approaches for RSFQ VLSI circuits are discussed in this paper. Specific guidelines are required for different RSFQ interconnect structures (PTL and JTL) for use in EDA tools such as automated layout and clock tree synthesis. In this paper, different PTL and JTL configurations are presented, and tradeoffs and limitations of the different configurations are discussed. A PTL with no driving circuit and one JJ in the receiver is proposed. The proposed PTL exhibits a higher margin as compared to a standard PTL. A margin of 29% for the bias current of the proposed receiver operating at 20 GHz in 10 kA/cm^2 technology is achieved. The delay of the proposed PTL is lower than the delay of a JTL interconnect for long interconnect. The proposed PTL interconnect has lower complexity, area, power, and delay, making the structure appropriate for automated layout and clock tree synthesis in RSFQ VLSI circuits.

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