Sense Amplifier for Spin-Based Cryogenic Memory Cells

Gleb Krylov, *Student Member, IEEE*, and Eby G. Friedman, *Fellow, IEEE*

***Abstract*—A clocked DC-to-SFQ converter is used as a sense amplifier to resolve small differences in the output current of a nanocryotron (nTron). The sense amplifier produces a variable number of SFQ pulses to represent different analog states by passing or blocking input clock pulses. This clock is derived from the system clock by synchronizing the read pulse to the same clock signal. These output pulses are counted and converted into a binary form. The sense amplifier exploits the specific shape of the nTron output waveform characterized by an L/R time constant to achieve the resolution of low magnetoresistance (MR) memory cells, and is adaptable to different nTron sizes, bias currents, and spin-based devices. The dynamic power dissipation and resolution of the sense amplifier can be adjusted by the frequency of the applied clock signal, allowing the resolution to be reduced for high MR devices. The sense amplifier consists of two Josephson junctions and occupies small area, particularly in comparison to a standard nTron device, and can therefore be connected to each column of the memory array.**

***Index Terms*—Single flux quantum, superconducting-integrated circuits, superconductor digital electronics.**

I. Introduction

SINGLE flux quantum (SFQ) technology is a promising superconductive circuit family suitable for energy efficient, high performance data centers and supercomputers [1]. One of the primary drawbacks limiting the use of this technology, however, is the lack of a fast and dense memory capable of operating within a cryogenic environment.

In an SFQ logic family, information is represented and processed in the form of magnetic flux quanta. Flip flops and logic gates store an internal state until a clock signal releases the data for further processing. The storage of magnetic flux can be viewed as the circulation of a persistent current through a SQUID loop within a logic gate or flip flop. As these loops are in a superconductive state, the storage elements dissipate no static power–a highly desirable feature for memory applications.

Several circuit topologies have been proposed for SFQ-based memory arrays [2], [3]. The primary drawback of these topologies, however, is low density. A state-of-the-art SQUID-based memory cell [2] requires an area of 15 μm^2, limiting the practical size of the on-chip memory array to hundreds of kilobits. Another approach to enable high density RAM for a cryogenic supercomputer is to use conventional CMOS-based memory and SFQ-to-CMOS interfaces. In this approach, SFQ pulses are amplified in two steps. One to two millivolt SFQ voltage signals are initially amplified to tens of millivolts using Suzuki stacks [4]. The amplitude of the resulting signal is increased to single volts using clocked CMOS comparators. The signal drives a conventional CMOS SRAM or DRAM cell. The DRAM cells also benefit from operating within a cryogenic environment – the retention time is drastically increased, enabling the use of DRAM cells as a static memory. A hybrid 64k SFQ/CMOS memory has been demonstrated [5], however, the density, delay, and need for wirebonding the separate SFQ and CMOS dies limit the applications of this hybrid SFQ/CMOS technology.

Recent research suggests the use of cryogenic spin-based memory - magnetic tunnel junctions (MTJ) and spin valves (SV) [6]. These device consist of a stack of different ferromagnetic and insulator materials, where the resistance of these devices can be varied by changing the orientation of the magnetization of the different layers. These spin-based devices can serve as memory elements, however, the devices require relatively high drive currents as compared to currents typically used in SFQ circuits. As SFQ logic cannot directly supply these high currents, special driver devices, controllable by SFQ pulses, are necessary. A recently developed driver device, compatible with SFQ circuits and suitable for supplying high currents, is a nanocryotron (nTron)–an electrothermal switch that can be controlled by an SFQ pulse.

In this paper, a sense amplifier topology for a spin-based cryogenic memory cell is proposed. In Section II, the circuit and device components of the memory cell and sense amplifier are described. In Section III, simulation results are presented. In Section IV, some conclusions are offered.

II. Circuit Components

In this section, the circuit and device components of the memory cell are introduced, and the topology of the sense amplifier is described. In Subsection II-A, existing cryogenic spin-based memory devices are discussed. In Subsection II-B, nanocryotron device operation is reviewed. In Subsection II-C, a memory cell combining these devices is introduced. In Subsection II-D, an SFQ flash A/D converter and a clocked DC-to-SFQ converter are presented, the advantages and disadvantages of these converters are discussed, and a clocked DC-to-SFQ converter is proposed

Manuscript received October 30, 2018; accepted April 5, 2019. Date of publication April 19, 2019; date of current version May 13, 2019. This work was supported by the Department of Defense (DoD) Agency—Intelligence Advanced Research Projects Activity (IARPA) through the U.S. Army Research Office under Contract W911NF-14-C-0089. *(Corresponding author: Gleb Krylov.)*

The authors are with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY 14627 USA (e-mail: gleb.krylov@rochester.edu; friedman@ece.rochester.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TASC.2019.2912166

for the sense amplifier. In Subsection II-E, several connection topologies for the proposed amplifier are discussed.

A. Cryogenic Spin-Based Devices

Magnetic memory is currently widely considered as a replacement for several layers of conventional CMOS memory hierarchy, such as SRAM and DRAM. Two prospective types of magnetic memory that operate within a cryogenic environment are cryogenic orthogonal spin transfer (COST) [7] and cryogenic spin hall effect (CSHE) [8] devices.

COST devices utilize a spin-valve structure with a polarizer for fast and low energy switching of the magnetization of the free layer. The major advantage of COST devices, as compared to CSHE, is the low impedance of the resulting magnetic memory element, resulting in enhanced compatibility with SFQ logic. COST devices currently exhibit a low magnetoresistance (MR), on the order of 10%. In this paper, a two terminal COST device with low MR is considered as a memory element.

B. Nanocryotron

A cryotron is a superconducting switch, first proposed in 1956 [9]. It is a four terminal device, in which current is passed through a coil wrapped around a wire which disrupts the superconductivity by exceeding the critical magnetic field of the wire. The nanocryotron, proposed in 2014 [10], is a three terminal electrothermal device consisting of a superconductive channel and a weak link (choke). When a current pulse is applied to the gate, connected to the weak link, a localized hotspot causes the channel to become resistive, diverting the bias current into the load. In this sense, an nTron device is similar to a superconducting nanowire single photon detector (SNSPD) [11], in which incident photons create localized hotspots, and current diverted into a load produces a voltage. The output waveform and relaxation time of an nTron, similar to an SNSPD, are characterized by an L/R time constant [12].

The current diverted into the load can be used to switch or read a spin-based memory cell. For readout, the nTron output current waveform is converted into a binary SFQ signal, later processed by SFQ logic.

C. Memory Cell Readout

For the purpose of the readout circuit, the memory cell is composed of a driver device and a spin-based memory element, such as an MTJ or spin valve device (see Subsection II-A). The driver device considered here is the nTron. The memory element is modeled as a variable resistive load of 5 or 5.5 ohms (corresponding to a magnetoresistance of 10%). Although the COST device exhibits a nonlinear dV/dI dependence on the current flowing through the device [7], it is negligible due to the magnitude of the currents used for readout ($\sim 45\ \mu$A). The memory cell is schematically shown in Figure 1. The read enable pulse V_{read} switches the driver (nTron), diverting the bias current I_{bias} into the load (spin valve), exhibiting a resistance R_{load}.

The nTron device is switched on (to a resistive state) by an SFQ pulse (the read enable signal V_{read}). A resistive-inductive current divider is formed between the nTron device and the spin valve memory cell R_{load}. The current I_{out} that flows through the memory cell biases the sense junction J_2 within the sense amplifier. The magnitude and shape of the output current waveform are dependent on the resistance R_{load}, and therefore the logic state of the memory cell.

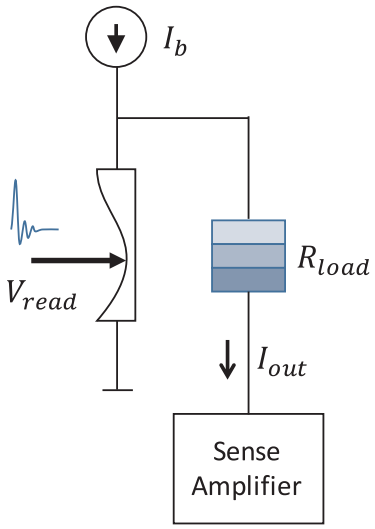

Fig. 1. Memory cell readout circuit. V_{read} is the read enable SFQ pulse, I_b is the bias current for the readout circuit, R_{load} is a spin valve element exhibiting a variable resistance, and I_{out} is the output current of the readout circuit.

D. Synchronous DC/SFQ Converter as Memory Sense Amplifier

Due to natural quantization of magnetic flux, SFQ technology provides numerous benefits for efficient and fast analog-to-digital conversion [13] Conventional SFQ analog-to-digital flash converters capable of resolving small differences in the nTron output current caused by a small MR require significant area for the resistive ladder and inductive quantizer. In addition, these converters typically require higher current than provided by an nTron device of reasonable size. A sense amplifier suitable for analog-to-digital conversion within the memory array, requiring significantly smaller area, is therefore presented in this subsection.

The proposed sense amplifier is based on a well known timed DC/SFQ converter, first described in [14]. The clocked DC-to-SFQ converter is schematically shown in Figure 2.

The converter consists of two JJs – a sense junction J_2 and an escape junction J_1. The incoming SFQ clock pulses are either transmitted by switching J_2 or blocked by switching J_1, depending upon the bias current of the sense junction. This bias current (I_{in} in Figure 2, and I_{out} in Figure 1) is the input of the converter. The two states of the memory cell produce two different resistances (R_{load}); therefore, two distinct L/R time constants and two different current waveforms at the input of the converter. The output of this sense amplifier is therefore in the form of a specific number of SFQ pulses which corresponds to the logic state of the memory cell.

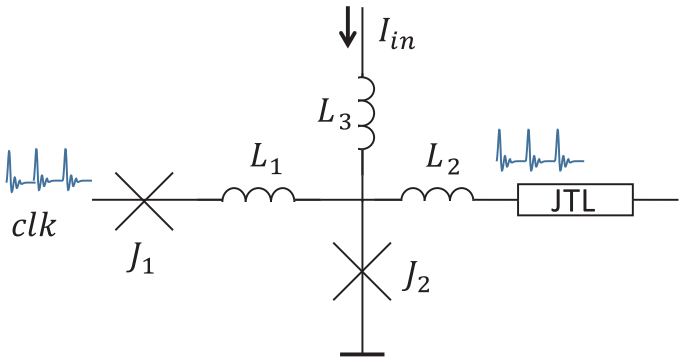

Fig. 2. Clocked DC-to-SFQ converter. J_1 and J_2 make up the decision making pair of Josephson junctions. The SFQ clock signal passes through the circuit and is modulated by the input current I_{in}, which functions as a bias current for J_2.

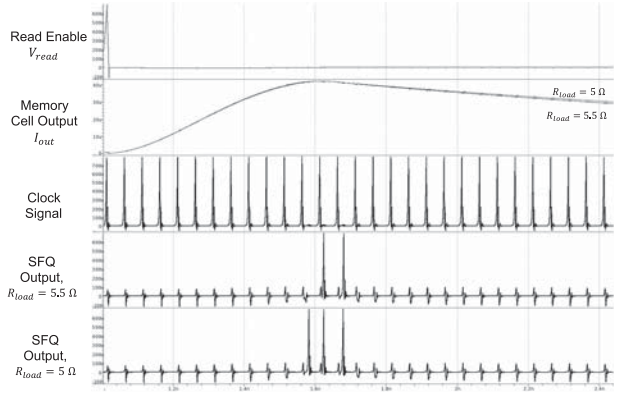

Fig. 3. Low MR waveforms. The clock frequency is 20 GHz. R_{load} is 5 Ω to 5.5 Ω. The bias current is 74 μA. The sense amplifier output is two to three SFQ pulses.

As the state of the memory cell is distinguished by the number of SFQ pulses, this output needs to be converted into standard RSFQ convention (logic one is the presence of an SFQ pulse, logic zero is the absence of an SFQ pulse). This conversion can be achieved by a counter attached to the output of the readout circuit. The counter introduces a significant overhead; however, only one counter per memory column is necessary. For prospective devices with improved MR, the number of generated SFQ pulses and therefore the size of the output counters can be decreased.

The operation of the sense amplifier for those devices with low MR can be enhanced by increasing the frequency of the input SFQ clock signal. This method enhances the resolution and speed of the amplifier, but requires larger output counters to discriminate between the two memory states.

The circuit described here is broadly used as a sensor circuit, including the previously mentioned hybrid Josephson-CMOS memory [15]. A few important distinctions exist with the previous work. This circuit is typically used to discriminate between two distinctly different current levels with a square shaped input waveform. Sensing is therefore reliable and binary (the input current is either ”on” or ”off”). The proposed topology utilizes the exponential L/R decay of the input current to produce a different number of SFQ pulses. This approach therefore exploits the shape of the nTron output waveform while enabling the use of a well known, compact, and robust readout circuit.

E. Sense Amplifier Topologies

Several possible methods exist to connect the clocked DC/SFQ converter to the memory readout circuit. These methods are described in the following subsections.

1) Direct Connection: The output of the nTron-COST device is directly connected to the input terminal of the SFQ-to-DC converter without any additional bias. In this way, the overhead of the additional bias lines is avoided. The sense junction (J_2 in Figure 2) is, however, only biased by the input current. This method requires higher nTron output current, resulting in a significantly larger nTron device and bias current.

2) Additional Current Bias: An additional current source is connected to the input of the sense amplifier. This approach enables a smaller nTron for the readout circuit.

3) Additional Flux Bias: Additional flux is inductively coupled into the SQUID loop within the sense amplifier ($J_1 - J_2$ in Figure 2). In this way, the benefits of additional bias current are combined with a more compact layout and lower energy dissipation.

III. Simulation Results

The proposed readout scheme is simulated in WRSpice [16] for the low MR (10%) and high MR (100%) cases and two different SFQ clock frequencies, 20 GHz and 50 GHz. All simulations in this section use the topology described in Subsection II-E1.

The circuit simulations utilize an RCSJ model of a Josephson junction with the fabrication process parameters for the MIT LL SFQ5ee process, and an unpublished compact model of the nanocryotron, which includes a nonlinear kinetic inductance and hotspot formation and relaxation [17], [18]. A compact model for a spin valve is not used since these devices are currently under development. Reliable switching of the MR states is assumed, and the spin valve element is modeled as two different resistances.

The component parameters for the simulations discussed in this section are chosen somewhat arbitrarily. The specific parameters should be obtained as a result of optimization for a particular spin valve resistance and MR. The critical current of J_1 and J_2 is 125 μA. J_1 is critically damped ($\beta = 1$), while J_2 is slightly underdamped ($\beta \approx 3$). The connecting inductors L_1 and L_2 between the junctions are 2 pH. The current input is connected through L_3, a 1 pH inductor. The nTron driver of the memory cell has a 12 nm gate, a 2 μm source/drain, and a 1.08 μm channel. The bias current of the nTron is varied, and is mentioned in the caption for Figures 3 to 5.

The simulations are initiated with a read enable pulse applied to the gate of the nTron. This pulse switches the nTron, diverting the bias current into the memory element R_{load}. For different R_{load}, different output waveforms are produced. The bias current applied to J_2 within the sense amplifier is therefore also

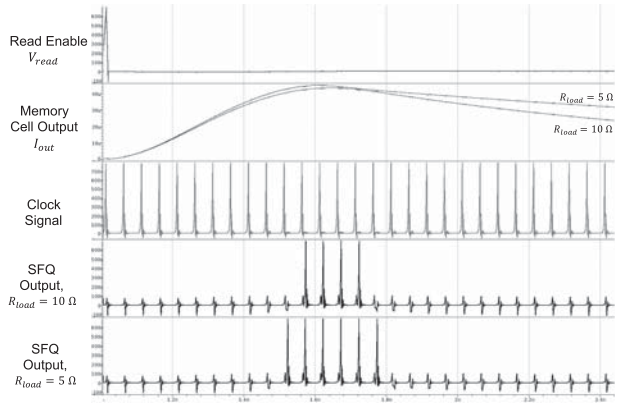

Fig. 4. High MR waveforms. The clock frequency is 20 GHz. R_{load} is 5 Ω to 10 Ω. The bias current is 76.6 μA. The sense amplifier output is four to six SFQ pulses.

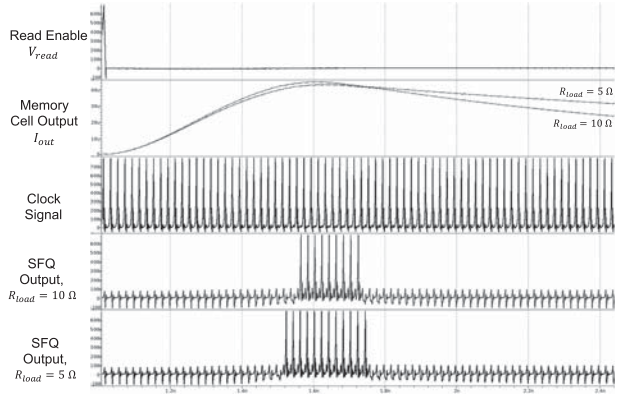

Fig. 5. High MR and high frequency waveforms. The clock frequency is 50 GHz. R_{load} is 5 Ω to 10 Ω. The bias current is 76.6 μA. The sense amplifier output is nine to twelve SFQ pulses.

different. This condition produces a varying number of clock signals passed to the output of the sense amplifier, corresponding to the state of the memory element.

Waveforms for the low MR case are shown in Figure 3. The resistance R_{load} of the memory cell is varied between 5 and 5.5 ohms, corresponding to 10% MR. The sense amplifier generates two or three SFQ pulses depending upon the state.

A larger output difference and greater robustness of operation are achieved for a memory element with a higher MR. Waveforms for the high MR case are shown in Figure 4. The resistance of the memory cell is varied between 5 and 10 ohms, corresponding to 100% MR. The sense amplifier produces four or six SFQ pulses.

In these simulations, the clock frequency is set to 20 Ghz. The waveforms for the high MR case operating at a higher clock frequency (50 Ghz) are shown in Figure 5. The sense amplifier produces nine or twelve SFQ pulses depending upon the state. The synchronous DC-to-SFQ converter therefore greatly benefits from the higher clock frequency.

IV. Conclusions

A sense amplifier to read memory cells composed of MTJs and nTrons is presented here. Guidelines for the sense amplifier are described, and simulation results for several MR values are shown. The sense amplifier is based on a clocked DC-to-SFQ converter, which exploits the properties of the nTron output current. Enhanced speed and resolution for spin-based memory cells with a low MR of 10% make a clocked DC-to-SFQ converter a flexible and low area solution for reading out magnetic memory. A high MR combined with a high clock frequency results in robust discrimination of the memory states.

Acknowledgment

The authors would like to thank M. Kazemi for helpful discussions and A. Wagner and S. Whiteley for the compact models used in the circuit simulations. The content of the information does not necessarily reflect the position or the policy of the Government, and no official endorsement should be inferred.

References

[1] M. A. Manheimer, "Cryogenic computing complexity program: Phase 1 introduction," *IEEE Trans. Appl. Supercond.*, vol. 25, no. 3, Jun. 2015, Art. no. 1301704.

[2] S. Nagasawa, K. Hinode, T. Satoh, Y. Kitagawa, and M. Hidaka, "Design of All-DC-Powered high-speed single flux quantum random access memory based on a pipeline structure for memory cell arrays," *Supercond. Sci. Technol.*, vol. 19, no. 5, pp. S325–S330, Mar. 2006.

[3] S. V. Polonsky, A. F. Kirichenko, V. K. Semenov, and K. K. Likharev, "Rapid single flux quantum random access memory," *IEEE Trans. Appl. Supercond.*, vol. 5, no. 2, pp. 3000–3005, Jun. 1995.

[4] H. Suzuki, T. Imamura, and S. Hasuo, "Applications of synchronized switching in series-parallel-connected Josephson junctions," *IEEE Trans. Electron Devices*, vol. 37, no. 11, pp. 2399–2405, Nov. 1990.

[5] T. V. Duzer *et al.*, "64-kb hybrid Josephson-CMOS 4 Kelvin RAM with 400 ps access time and 12 mW read power," *IEEE Trans. Appl. Supercond.*, vol. 23, no. 3, Jun. 2013, Art. no. 1700504.

[6] I. I. Soloviev, N. V. Klenov, S. V. Bakurskiy, M. Y. Kupriyanov, A. L. Gudkov, and A. S. Sidorenko, "Beyond Moore's technologies: Operation principles of a superconductor alternative," *Beilstein J. Nanotechnol.*, vol. 8, pp. 2689–2710, Nov. 2017.

[7] L. Ye *et al.*, "Spin-transfer switching of orthogonal spin-valve devices at cryogenic temperatures," *J. Appl. Phys.*, vol. 115, no. 17, Feb. 2014, Art. no. 17C725.

[8] L. Liu, C.-F. Pai, Y. Li, H. W. Tseng, D. C. Ralph, and R. A. Buhrman, "Spin-Torque switching with the giant spin hall effect of tantalum," *Science*, vol. 336, no. 6081, pp. 555–558, May 2012.

[9] D. A. Buck, "The Cryotron—A superconductive computer component," *Proc. IRE*, vol. 44, no. 4, pp. 482–493, Apr. 1956.

[10] A. N. McCaughan and K. K. Berggren, "A Superconducting-Nanowire three-terminal electrothermal device," *Nano Lett.*, vol. 14, no. 10, pp. 5748–5753, Sep. 2014.

[11] G. N. Gol'tsman *et al.*, "Picosecond superconducting single-photon optical detector," *Appl. Phys. Lett.*, vol. 79, no. 6, pp. 705–707, Aug. 2001.

[12] A. J. Kerman *et al.*, "Kinetic-Inductance-Limited reset time of superconducting nanowire photon counters," *Appl. Phys. Lett.*, vol. 88, no. 11, Mar. 2006, Art. no. 111116.

[13] O. A. Mukhanov, D. Gupta, A. M. Kadin, and V. K. Semenov, "Superconductor analog-to-digital converters," *Proc. IEEE*, vol. 92, no. 10, pp. 1564–1584, Oct. 2004.

[14] K. K. Likharev and V. K. Semenov, "RSFQ Logic/Memory family: A new Josephson-junction technology for sub-terahertz-clock-frequency digital systems," *IEEE Trans. Appl. Supercond.*, vol. 1, no. 1, pp. 3–28, Mar. 1991.

[15] Q. Liu *et al.*, "Simulation and measurements on a 64-kbit hybrid Josephson-CMOS memory," *IEEE Trans. Appl. Supercond.*, vol. 15, no. 2, pp. 415–418, Jun. 2005.

[16] S. R. Whiteley, "Josephson junctions in SPICE3," *IEEE Trans. Magn.*, vol. 27, no. 2, pp. 2902–2905, Mar. 1991.

[17] J. K. W. Yang, A. J. Kerman, E. A. Dauler, V. Anant, K. M. Rosfjord, and K. K. Berggren, "Modeling the electrical and thermal response of superconducting nanowire single-photon detectors," *IEEE Trans. Appl. Supercond.*, vol. 17, no. 2, pp. 581–585, Jun. 2007.

[18] J. R. Clem and V. G. Kogan, "Kinetic impedance and depairing in thin and narrow superconducting films," *Phys. Rev. B*, vol. 86, Nov. 2012, Art. no. 174521.