Flux Mitigation in Wide Superconductive Striplines

Tahereh Jabbari, *Student Member, IEEE*, and Eby G. Friedman, *Fellow, IEEE*

***Abstract*—The increasing complexity of modern superconductive circuits, and single flux quantum (SFQ) circuits in particular has made the issue of flux trapping of growing importance. The use of wide superconductive striplines for signal routing has exacerbated this issue. Trapping residual magnetic fields in these striplines degrades performance while reducing margins, damaging the operability of superconductive circuits. In this article, an area efficient topology for striplines is introduced to manage flux trapping in large scale SFQ circuits. This topology is composed of narrow parallel lines in series with small resistors. The proposed topology decreases the length of the striplines by exploiting the mutual inductance between the narrow parallel lines. The topology requires significantly less area while preventing flux trapping within wide superconductive striplines. The narrow parallel line topology also reduces coupling capacitance between striplines. The proposed approach is compatible with automated routing of large scale SFQ integrated circuits.**

***Index Terms*—Automated layout and routing, electronic design automation (EDA), single flux quantum (SFQ), superconductive integrated circuits.**

I. Introduction

RECENT advances in fabrication technology and electronic design automation have enabled the increasing integration of rapid single flux quantum (RSFQ) circuits [1], [2]. A significant issue in large scale superconductive integrated circuits is the sensitivity of SFQ circuits to magnetic fields [3]–[9]. Residual magnetic fields in very large scale integration (VLSI) complexity RSFQ circuits increase the probability of trapped fluxons within the ground planes, Josephson junctions (JJs), superconductive loops, and striplines [7], [10]. Flux mitigation is, therefore, necessary within large scale RSFQ circuits and, in particular, the striplines, to support the development of advanced superconductive systems.

The fluxons trapped within the wide striplines near the logic cells degrade circuit operation while lowering the critical current and decreasing the bias margins of the JJs. The trapped magnetic field also couples trapped fluxons into nearby inductances, interconnects, and bias lines.

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The authors are with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY 14627 USA (e-mail: tjabbari@ece.rochester.edu; friedman@ece.rochester.edu).

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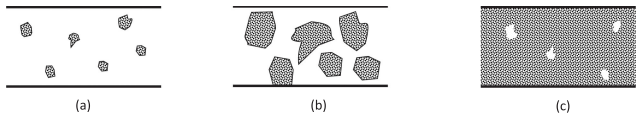

Fig. 1. Flux trapping process in a cryogenic thin film. (a) Superconductive regions at the critical temperature. (b) Growing superconductive regions above the critical current. (c) Four normal regions surrounded by merged superconductive regions below the critical temperature.

Moats within superconductive ground planes have been used to mitigate the effects of flux trapping within SFQ circuits [3], [5]. These moats are widely used in ground planes to prevent undesired magnetic flux in unwanted areas, preventing degradation in performance and more circuit malfunctions. The location of the moats is important to minimize coupling between the inductances and moats [3]–[5], [11]. The moats within the striplines degrade the stripline characteristics; therefore, moats are not used for striplines. A novel approach is, therefore, required to eliminate flux trapping within wide superconductive striplines while not increasing the area of the striplines.

In this article, a topology is proposed to manage flux trapping within wide striplines. The principles of flux trapping, minimum energy, and external magnetic thresholds are briefly reviewed in Section II. Different types of trapped flux in SFQ cells are also described. A configuration for wide superconductive striplines to eliminate flux trapping is proposed in Section III. This new stripline configuration is evaluated in Section IV. Finally, this article is concluded by Section V.

II. Background

Flux trapping within superconductive thin films was discovered in 1982 [12]. During the cooling process, quantized flux is trapped within a superconductive film at temperatures below the critical temperature, T_C. The flux trapping process is illustrated in Fig. 1. As the temperature approaches the critical temperature, superconductive regions appear within the film [see Fig. 1(a)]. These superconductive regions grow larger as the temperature cools [see Fig. 1(b)]. After merging of the superconductive regions, some normal regions will be surrounded by superconductive regions [see Fig. 1(c)]. If the magnetic field within these normal regions exceeds $1/2\Phi_0$, a vortex will be trapped within these regions [4], [5], [12], [13].

The critical magnetic field to produce a vortex within a superconductive film is B_C. Vortices are excluded from the film when the applied magnetic field B_a is below B_C. A trapped vortex within a superconductive film is described by the Gibbs free energy [3], [13]. The minimum energy to trap a vortex is

the pairing energy

$$E_{\text{pair}} = \frac{\Phi_0}{4\pi\mu_0\Lambda} \tag{1}$$

where Λ is the Pearl length $\Lambda = 2\lambda^2/d$ (λ is the London penetration depth and d is the thickness of a stripline), $\Phi_0 \approx 2.07 \times 10^{-7}$ is the superconductive flux quantum, and $\mu_0 \approx 4\pi \times 10^{-7}$ H/m is the magnetic permeability of free space [13]. The Gibbs free energy exhibits a local minimum and maximum at the center of a superconductive stripline. The difference between the Gibbs free energy of the local minimum and maximum in the center of the stripline is E_B. The vortex trapping process occurs when E_B equals E_{pair}, which occurs at $B_K = 1.65\ \Phi_0/\text{W}^2$ [4], [13].

For an applied magnetic field B_a above the critical magnetic field of stripline B_K, the number of trapped vortices n is,

$$n = \frac{B_a - B_K}{\Phi_0}\ . \tag{2}$$

As long as $B_a < B_K$, no flux is trapped within the striplines. Therefore, the maximum width of the striplines based on an applied magnetic field B_a is

$$W = \sqrt{\frac{1.65\Phi_0}{B_a}}\ . \tag{3}$$

This expression determines the maximum width W_{max} of a stripline without trapped fluxons. For narrower lines, B_K is significantly larger. The probability of trapping flux is, therefore, almost zero for $\text{W} \ll W_{\text{max}}$.

Another important type of trapped flux in SFQ cells is produced by a residual magnetic field caused by bias currents. Due to this magnetic field, flux quanta are trapped within the inductance of the superconductive loops. Some SFQ cells with a large storage loop are particularly sensitive to flux trapping, such as a C-element and D flip flop (DFF). If flux is trapped in the inductors within these cells, the cell may not operate correctly. A C-element is commonly used in synchronization and handshaking [14]. Flux trapping in a C-element can cause skews within the synchronization circuitry.

III. Model for Wide Striplines

An important issue in SFQ digital circuits is the sensitivity of the cell margins to trapped magnetic flux inside and near the logic elements. A residual magnetic field degrades the performance of the JJs, producing noise and lowering margins. The purpose of this article is to introduce a methodology to mitigate the effects of flux trapping on striplines and JJs. The proposed strategy is described in Section III-A. A different approach is described in Section III-B to eliminate residual currents in superconductive loops. A combination of these techniques is described in Section III-C to mitigate flux trapping in striplines while simultaneously eliminating residual currents in SFQ circuits.

A. Multiple Narrow Parallel Lines

A novel stripline topology is described in this section to mitigate flux trapping in striplines, inductances, and interconnects.

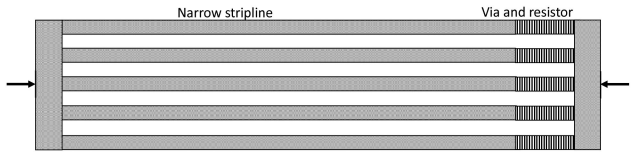

Fig. 2. Configuration of the stripline composed of multiple narrow parallel lines.

Fig. 3. Current distribution within a stripline with the six parallel line topology.

The topology of the proposed stripline is shown in Fig. 2. The stripline is placed between two ground planes to shield the signal routing [15], [16]. Multiple narrow parallel lines are used rather than a single wide line. The narrow parallel lines are connected with perpendicular lines at the ends of the narrow lines. The preferable width of the narrow lines and the spacing between these lines are technology dependent. The stripline width is set by (3), where $W \ll W_{\text{max}}$ and the maximum magnetic field B_a. A thinner stripline width lowers the likelihood of flux being trapped within the stripline.

The current distribution within the superconductive stripline is nonuniform [17]. The current density of a stripline with six narrow lines is shown in Fig. 3. The current flows equally through all of the narrow parallel lines. More current flows along the edges of the narrow lines as compared to the center of the lines. The proposed topology exhibits a higher effective inductance as compared to a wide line due to the mutual inductance between the narrow parallel lines.

Narrow parallel lines also enhance the layout of SFQ cells. In superconductive circuits, a wide line is used rather than a single narrow line between two JJs far from each other. An example of an inductor with the same length and width is depicted in Fig. 4. The length $L = l_1 + l_2 + l_3$ and width w of both inductive striplines are, respectively, 28 and 1.7 μm. The configuration of the parallel lines is composed of two 0.5 μm parallel lines with 0.7 μm spacing. Here, the MIT Lincoln Laboratory SFQ5ee fabrication process [15] is assumed, where the striplines are placed in layer M5. The inductance of the wide stripline and two narrow striplines is, respectively, 5.8 and 7.9 pH. The narrow parallel line configuration achieves the target length while preventing flux trapping in wide lines.

B. Small Resistor

To manage the residual currents within a superconductive loop, a small resistor is placed in series with the loop inductance. A circuit model of this structure is shown in Fig. 5. The inductor

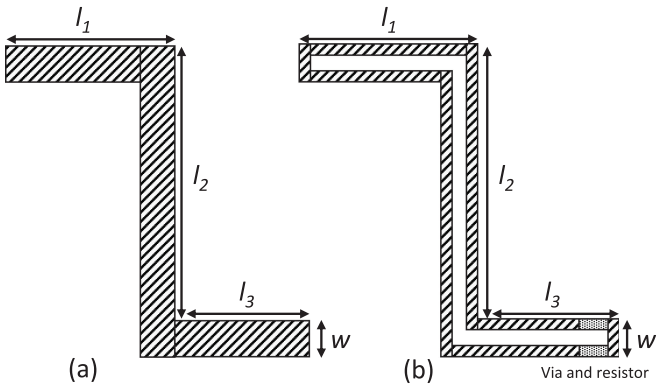

Fig. 4. Configuration of the stripline. (a) Wide line and (b) two narrow parallel lines. $L = l_1 + l_2 + l_3 = 28$ μm and $w = 1.7$ μm, MIT Lincoln Laboratory SFQ5ee fabrication process [7], [15]

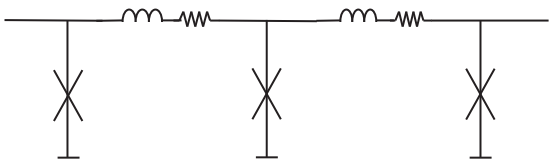

Fig. 5. Circuit model of the flux trapping mitigation circuit with a small resistor in series with an inductor.

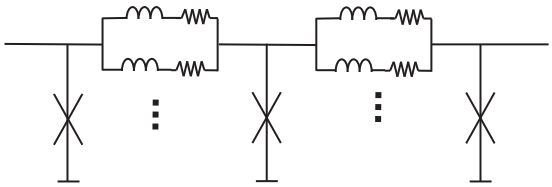

Fig. 6. Circuit model of the flux trapping mitigation circuit with multiple narrow parallel lines in series with small resistors.

in series with the small resistor releases any unwanted flux quanta from the superconductive loops, allowing the magnetic flux to decay [15]. The decay time τ is L/R, where L and R are, respectively, the loop inductance and the small series resistor. Two constraints exist for this decay time. The decay time should be longer than the clock period $1/f_{\text{clk}}$ and sufficiently short to prevent the storage loops from resetting.

C. Multiple Narrow Parallel Lines in Series With Small Resistors

To minimize the occurrence of flux trapping in JJs and wide inductors, a narrow parallel line topology can be combined with a small resistor in series with a loop inductance. The topology of this structure is shown in Fig. 6. To prevent flux trapping in superconductive loops composed of narrow lines, each narrow line is connected to a single resistive layer. The small resistors also produce parasitic inductances within the narrow lines. The individual resistors increase the number of vias within complex SFQ circuits. The narrow parallel line topology releases any unwanted flux quanta from the superconductive loops and from the JJs within the logic cells. The narrow parallel lines prevent flux from being trapped, while the small resistors break the superconductive loops, allowing the magnetic flux to gradually decay.

An important issue in the proposed approach is the dissipation of the stored flux within the storage loop. Due to the resistor, the stored flux decays over time. This feature disturbs the operation of the superconductive storage loops at ultralow frequencies. The proposed topology can be utilized in storage loops when data do not need to be stored.

TABLE I
COMPARISON OF STRIPLINE CHARACTERISTICS WITH DIFFERENT NARROW PARALLEL LINE STRUCTURES, 10 KA/CM^2 PROCESS TECHNOLOGY [15]

Stripline	Length = 80 μm		Length = 500 μm	
	Width (μm)	Impedance (Ω)	Width (μm)	Impedance (Ω)
Wide stripline	5.2	7.5	5.2	7.3
Two parallel striplines	5.1	7.276	5.1	7.275
Four parallel striplines	5.1	7.275	5.1	7.275
Six parallel striplines	5.5	6.835	5.5	6.83

IV. CHARACTERIZATION OF NARROW PARALLEL STRIPLINES

The parallel narrow line configuration is characterized in this section. This structure is evaluated with striplines and the inductive loop within a DFF. Characterization of the passive transmission lines (PTLs) striplines is described in Section IV-A, and evaluation of the inductive loop within a DFF cell is described in Section IV-B .

A. Narrow Parallel Lines for Signal Routing

The narrow parallel PTL line topology has been characterized in Sonnet. An $RLGC$ model is used to compare the characteristics of a wide stripline with multiple narrow parallel striplines. In this article, the dimensions of the striplines, minimum feature size of the striplines, and space between the parallel narrow lines are based on the MIT Lincoln Laboratory SFQ5ee fabrication process [7], [15]. The passive striplines are within the M2 layer and are 5.2 μm wide (10 kA/cm^2 process technology [16]). Four configurations with the same width are considered. The configurations are composed of a single 5.2 μm wide line, two 2.3 μm wide parallel lines with 0.6 μm spacing, four 1 μm wide parallel lines with 0.5 μm spacing, and six 0.5 μm wide parallel lines with 0.5 μm spacing. A comparison of the impedance of these different configurations is listed in Table I. The length of the PTL striplines is 80 and 500 μm. The multiple narrow parallel line topology exhibits the same output impedance characteristics as the wide lines; no changes are therefore required for the driver and receiver within the PTL. Operation of the receiver connected to a stripline with four narrow lines is shown in Fig. 7. The circuit operates correctly when connected to the multiple narrow line topology. In the routing layer, a single narrow stripline produces a high impedance, which requires a different receiver and driver circuit.

The bias current margins of the receiver and the driver [8] connected to a 500 μm stripline with four narrow parallel lines

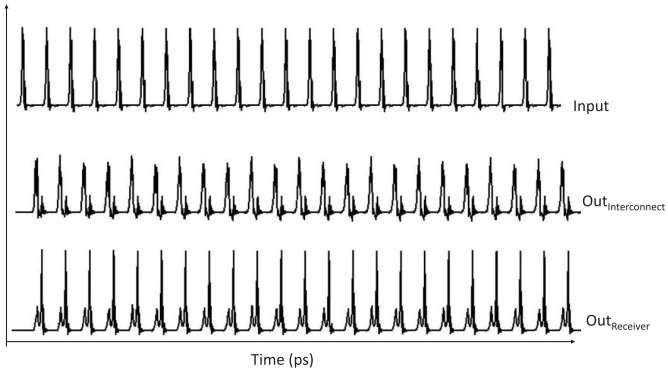

Fig. 7. Operation of the receiver connected to the stripline with four narrow parallel lines.

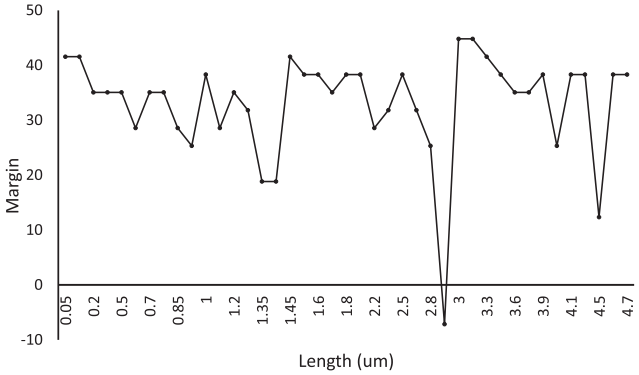

Fig. 9. Resonance effects in a stripline with four narrow parallel lines at 20 GHz, 10 kA/cm^2 technology.

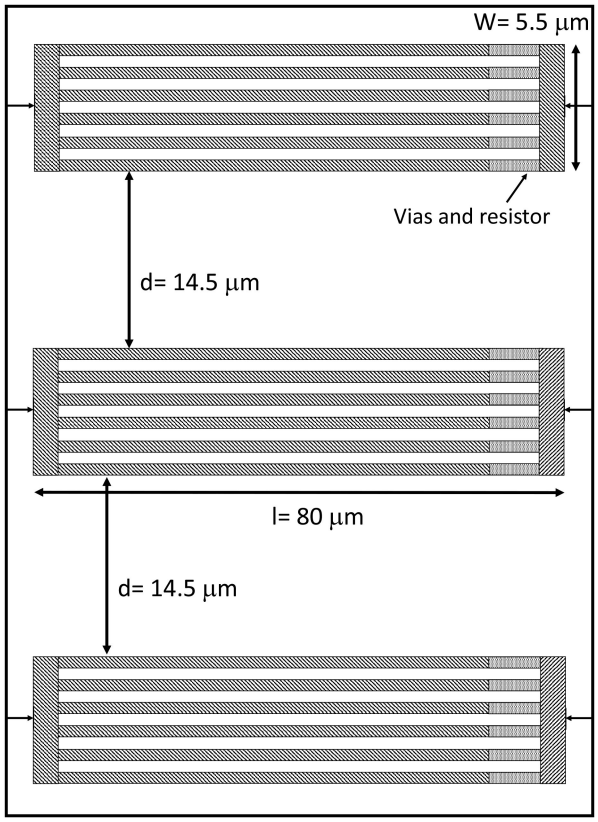

Fig. 8. Configuration of the stripline topology with six parallel lines.

are, respectively, (-40%, $+30\%$) and ($\pm 50\%$). The margins of the critical current for the JJ within the receiver and the driver are approximately, respectively, (-25%, $+35\%$) and (-32%, $+68\%$). The margins of the inductor within the receiver are approximately -75% and $+30\%$.

The coupling capacitance between three interconnects is evaluated in Sonnet based on a π model at 20 GHz. One, two, four, and six parallel line topologies for the interconnect are considered. The configuration of the stripline with six parallel lines is shown in Fig. 8. The width of a wide stripline and a stripline with six narrow parallel lines is, respectively, 5.2 and 5.5 μm. The width of the narrow lines and the space between the narrow lines is 0.5 μm. The length of the lines is 80 μm. The space between two striplines is 14.5 μm. The coupling capacitance between two wide striplines is 0.9 pF. The coupling capacitance between two striplines with six narrow parallel lines is 0.2 pF. The narrow parallel line configuration exhibits a much smaller coupling capacitance with the nearby striplines as compared to the wide interconnect stripline. The proposed approach, therefore, supports routing of long robust superconductive striplines.

The bias margin of the receiver connected to a stripline with the four narrow parallel line topology is shown in Fig. 9. At a specific frequency, the bias margin is determined for different stripline lengths. The dependence of the bias margin on the stripline length is depicted in Fig. 9. The resonance length of a stripline depends upon the frequency of the SFQ signal [9], which peaks at the lowest margins (see Fig. 9). The resonance lengths degrade the operation of the receiver. The resonance behavior of the single wide stripline [9] and the stripline with four narrow parallel lines at 20 GHz occurs at 2.9 mm. The multiple narrow parallel line topology exhibits the same set of resonance lengths as a single wide stripline. The forbidden set of resonance lengths of a wide PTL is therefore applicable for the proposed configuration [9].

B. Multiple Narrow Parallel Lines in Series With Small Resistors Within DFF

A long and wide inductor within the storage loop traps significantly more fluxons. In the layout of a standard XOR and DFF, the length of the inductor is 50 μm with a width of 2 μm and 40 μm with a width of 1 μm [16]. Using narrow parallel inductors enhances the layout of the SFQ cells, requiring less area while preventing flux from being trapped within the inductors.

The topology composed of a narrow parallel line in series with small resistors is also evaluated. The inductance of the storage loop is composed of two narrow parallel inductances, i.e., L1 and L2, in series with two small resistors. The small resistors in series with the narrow parallel lines allow the trapped magnetic flux to decay. The resistive range of the small resistors for a DFF operating at 20 GHz is $0 \ll R \ll 200\,\text{m}\Omega$. Large resistors degrade the operation of the cell. Small resistors of $\approx 40\ \text{m}\Omega$ do not significantly degrade the operation of the DFF while effectively removing residual currents within the storage loop.

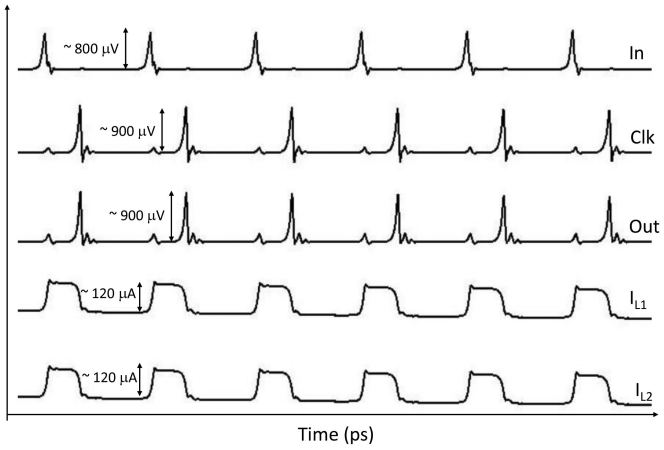

Fig. 10. Operation of the DFF with two narrow lines in series with a resistor. In, Clk, and Out are, respectively, the input, clock pulse, and output of the DFF cell. I_{L1} and I_{L2} are the loop currents within the parallel inductances.

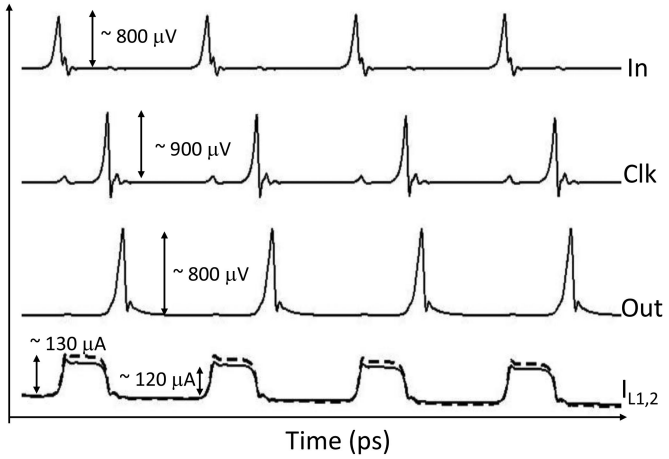

Fig. 11. DFF operation with two different narrow lines. In, Clk, and Out are, respectively, the input, clock pulse, and output of the DFF cell. The solid line is the current in the larger inductance ($L_1 = 19$ pH), and the dashed line is the current in the smaller inductance ($L_2 = 16$ pH).

Operation of a DFF cell with two parallel inductances and resistors is shown in Fig. 10. A small parasitic inductance in series with each small resistor is included. The circuit correctly operates at both low and high operating frequencies although a small degradation in the performance of the storage loop is exhibited due to the transition time of the loop current (see I_{L1} and I_{L2} in Fig. 10). The margins of the loop inductances are +95% and −60%. The margins of the bias current are +37% and −60%. The margins of the JJs are greater than ±30%. Flux trapping in the loop inductors is prevented by the multiple narrow lines. The small resistors remove any residual current within the JJs and break any undesired superconductive loops while exhibiting wide margins.

Process variations are a challenging issue in large scale integrated circuits. Due to resolution limitations and variations in the photolithography process, nonuniform shapes often occur in striplines, changing the inductance. The effects of process variations in multiple narrow parallel lines are evaluated in the storage loop within a DFF circuit. The loop inductance of the DFF is 8.5 pH [18]. This inductance is modeled with two different narrow parallel lines, L_1 and L_2, respectively, as 19 and 16 pH. The operation of the DFF is shown in Fig. 11. The circuit operates correctly when considering the effects of process variations. These variations slightly affect the resistive range of the small resistors, decay time, and current within the storage loops. The current within the storage loops is dependent upon the inductance that stores the flux quantum. A narrow line with a larger inductance passes a lower current (see the solid line in Fig. 11). The difference between the currents is approximately 10 μA (see $I_{L1,2}$ in Fig. 11). A small difference between the inductances produces a small difference in the currents that store the flux quantum. Minimal process variations [19], [20], therefore, negligibly affect the current within the storage loops. The proposed flux mitigation approach, therefore, supports robust routing of superconductive striplines while requiring less area and producing less coupling noise.

V. Conclusion

Flux trapping within superconductive striplines is a significant issue in the routing of large scale RSFQ circuits. The trapped fluxons degrade the performance and margins of these circuits. A multiple narrow parallel line topology is proposed to prevent flux trapping in striplines while simultaneously eliminating residual currents in SFQ circuits. The maximum width of the narrow parallel striplines is set by the applied magnetic field B_a and critical magnetic field B_K within the stripline. The proposed flux mitigation topology requires less physical area and produces less capacitive coupling noise in VLSI complexity RSFQ circuits. Design guidelines and tradeoffs are also presented for the multiple narrow parallel line topology. These guidelines are compatible with automated routing tools.

Acknowledgment

The content of the information does not necessarily reflect the position or the policy of the U.S. Government, and no official endorsement should be inferred.

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Tahereh Jabbari (Student Member, IEEE) received the B.Sc. and M.Sc. degrees from the Sharif University of Technology, Tehran, Iran, in 2012 and 2015, respectively, and the M.Sc. degrees, in 2019, from the University of Rochester, Rochester, NY, USA, where she is currently completing the Ph.D. degree, all in electrical engineering.

From 2015 to 2017, she was a Researcher in Superconductive Digital Electronics with the Superconductor Electronics Research Laboratory, Sharif University of Technology. Her research interests include superconducting digital electronics, electronic design automation techniques and algorithms, global signaling, synchronous and asynchronous clocking of very large scale integration single flux quantum circuits, security analysis of superconductive electronics, microwave behavior of superconductive striplines, noise coupling and flux trapping issues in superconductive circuits, adiabatic quantum flux parametron (AQFP) and directly coupled quantum flux parametron (DQFP) interface circuits, bistable Josephson junctions, and all-Josephson junction superconductive circuits.

Eby G. Friedman (Fellow, IEEE) received the B.S. degree from Lafayette College, Easton, PA, USA, in 1979, and the M.S. and Ph.D. degrees from the University of California Irvine, Irvine, CA, USA, in 1981 and 1989, respectively, all in electrical engineering.

He was with Hughes Aircraft Company, from 1979 to 1991, where he became a Manager of the Department of Signal Processing Design and Test, where he was responsible for the design and test of high-performance digital and analog integrated circuits (ICs). Since 1991, he has been with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY, USA, where he is currently a Distinguished Professor and the Director of the High Performance Very Large Scale Integration/IC Design and Analysis Laboratory. He is also a Visiting Professor with the Technion—Israel Institute of Technology, Haifa, Israel. He is the author of almost 600 papers and book chapters, inventor of 24 patents, and the author or editor of 19 books in the fields of high speed and low power CMOS design techniques, 3-D design methodologies, high speed interconnect, and the theory and application of synchronous clock and power distribution networks. His current research interests include high performance synchronous digital and mixed-signal microelectronic design and analysis with application to high speed portable processors, low-power wireless communications, and server farms.

Dr. Friedman is a recipient of the IEEE Circuits and Systems Mac Van Valkenburg Award, the IEEE Circuits and Systems Charles A. Desoer Technical Achievement Award, the University of Rochester Graduate Teaching Award, and the College of Engineering Teaching Excellence Award. He is a Member of the Editorial Board of *Journal of Low Power Electronics* and *Journal of Low Power Electronics and Applications*, and a Member of the Technical Program Committee of numerous conferences. He was the Editor-in-Chief and the Chair of the Steering Committee of IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, Editor-in-Chief of the *Microelectronics Journal*, Regional Editor for *Journal of Circuits, Systems and Computers*, a Member of the Editorial Board of the PROCEEDINGS OF THE IEEE, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: ANALOG AND DIGITAL SIGNAL PROCESSING, *Analog Integrated Circuits and Signal Processing*, IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS, and *Journal of Signal Processing Systems*, a Member of the Circuits and Systems Society Board of Governors, and the Program and Technical Chair of several IEEE conferences. He is a Senior Fulbright Fellow and an Honorary Chair Professor with National Sun Yat-sen University.