All-JJ Logic Based on Bistable JJs

Tahereh Jabbari, Mark Bocko, and Eby G. Friedman

(Invited Paper)

***Abstract*—The all-JJ logic family is a promising area and power efficient, scalable single flux quantum (SFQ) technology for application to exascale supercomputers. All-JJ superconductive logic is based on a superconductor-ferromagnet-superconductor (SFS) bistable JJ, enabling nanometer feature sizes in VLSI complexity superconductive systems. In this paper, a mechanical analogy is proposed to describe the dynamic behavior of these bistable JJs. Novel all-JJ logic gates, such as TFF, DFF, OR, AND, and NOT gates, are presented here. All-JJ circuits are composed of bistable JJs, standard JJs, and bias currents, not requiring large inductors within the storage loops. All-JJ logic cells exhibit less delay and power than standard SFQ cells with the same critical current density. All-JJ systems can operate at high frequencies due to the small capacitance of the SFS JJ. A complex all-JJ circuit from the suite of ISCAS'85 benchmark circuits is also characterized. This complex all-JJ circuit exhibits less delay and power as compared to standard SFQ logic. The bias current in a conventional benchmark circuit and all-JJ benchmark circuit is, respectively, 22 mA and 13 mA. The delay of each cell within the conventional benchmark circuit and all-JJ benchmark circuit is, respectively, approximately 20 and 8 ps. A parasitic inductance in series with the JJs disturbs the current distribution within the all-JJ circuits while degrading the margins. To suppress the effects of this parasitic inductance on SFS JJs, small linear inductors are added to manage the current distribution and improve the parameter margins.**

***Index Terms*—Single flux quantum, superconductive integrated circuits, bistable Josephson junctions, all-JJ circuits.**

I. Introduction

SINGLE flux quantum (SFQ) logic based on Josephson junctions (JJ) is a promising ultra-low power and ultra-high speed circuit technology for beyond CMOS exascale supercomputing [1], [2], [3], [4]. Superconductive IC technology has been demonstrated to operate at frequencies approaching 80 GHz for an RSFQ arithmetic logic unit with an 8 b data path suitable for high performance computing applications [5], [6]. These features make superconductive logic a promising candidate for scalable computing systems.

The integration density of superconductive circuits is far lower than current CMOS technology. Due to the complexity of the clock distribution and bias networks in SFQ cells, scaling superconductive systems is a challenging issue. Shift registers with a circuit density of 7.4×10^6 JJs/cm^2 and 1.3×10^7 JJs/cm^2 have recently been fabricated for, respectively, the 250 and 150 nm MIT Lincoln Laboratory (LL) process [7]. Recent advances in the fabrication of VLSI complexity SFQ systems require an increasing number of inductors. The large inductors in the SFQ cells occupy a significant area and are difficult to scale, while producing inductive noise coupling, flux trapping [8], [9], [10], [11], and longer delay. Scaling superconductive systems to a higher density therefore requires novel approaches. A new inductor-less superconductive logic family [12] based on a ferromagnetic JJ enables nanometer feature sizes for VLSI superconductive systems.

Recent research in superconductive technology has included the development of ferromagnetic JJs with a pure second harmonic in the current-phase relationship and double well energy-phase relationship [13], [14]. These JJs are known as bistable JJs due to the double well energy-phase relation [12]. In bistable SFS Josephson junctions, the amplitude of the second harmonic B is greater than half of the amplitude of the first harmonic A, $|B| > A/2$. If B is negative, the energy minima symmetrically occur at $\pm\phi$, where ϕ is an arbitrary phase and $0 < |\phi| \leq \pi/2$. If the amplitude of the second harmonic is positive, the energy minima occur at $\phi = 0$ and $\pm\pi$ [15], [16], [17]. Note that 0-π junctions with only a second harmonic are called $2\phi-$JJ [12], [13]. Superconductive circuits based on ferromagnetic bistable $2\phi-$JJs are known as all-JJ logic circuits.

The all-JJ logic family enables the development of scalable superconductive circuits [12], [18]. This logic family requires no large inductances – for example, greater than 8 pH – within the storage loop of the logic cells. A standard SFQ storage loop includes two standard JJs and a large inductance whereas in an SFS logic family, the storage loop is replaced with two bistable JJs [12], [18]. A 2ϕ bistable JJ requires only half of an SFQ pulse to switch the phase. These structures therefore dissipate less power while enabling nanometer feature sizes in superconductive systems. To enable large scale all-JJ systems, novel logic cells based on a 2ϕ bistable JJ are required.

In this paper, the dynamic behavior of a bistable JJ is described in Section II. Novel all-JJ logic cells are presented in Section III. The effects of parasitic and linear inductors on the operation of

Manuscript received 7 December 2022; revised 15 February 2023; accepted 12 March 2023. Date of publication 23 March 2023; date of current version 21 April 2023. This work was supported in part by the National Science Foundation under Grant 2124453 and in part by the Department of Defense Agency Intelligence Advanced Research Projects Activity through the U.S. Army Research Office under Grant W911NF-17-9-0001. *(Corresponding author: Tahereh Jabbari.)*

The authors are with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY 14627 USA (e-mail: tjabbari@ur.rochester.edu; mark.bocko@rochester.edu; friedman@ece.rochester.edu).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TASC.2023.3260774.

Digital Object Identifier 10.1109/TASC.2023.3260774

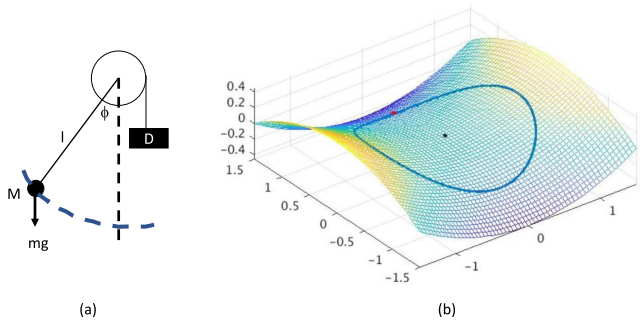

Fig. 1. Mechanical analogy of a JJ, (a) pendulum system illustrating the dynamic behavior of a standard JJ, and (b) hyperbolic paraboloid system illustrating the dynamic behavior of a bistable JJ.

all-JJ circuits are described in Section IV. The paper is concluded in Section V.

II. Dynamic Behavior of Josephson Junctions

The dynamic behavior of a standard JJ based on a pendulum system is described in Section II-A. The dynamic behavior of a bistable $2\phi-$JJ based on a hyperbolic paraboloid system is described in Section II-B.

A. Standard Josephson Junction

A circuit model of a standard Josephson junction, where a Josephson junction, resistor, and capacitor are connected in parallel, is a resistively and capacitively shunted junction (RCSJ) [3], [12], [18], [19]. The current passing through a standard JJ is the sum of individual current components,

$$i = I_c sin(\phi) + \frac{1}{R}.\frac{\hbar}{2e}\frac{d\phi}{dt} + c\frac{\hbar}{2e}\frac{d^2\phi}{dt^2} \quad , \tag{1}$$

where I_c is the critical current, ϕ is the phase across the junction, $\hbar$ is the reduced Plank's constant, and R and c are, respectively, the shunt resistor and capacitance in the RCSJ model.

An alternative analogy for describing the dynamic behavior of a JJ is a pendulum system. Expression (1) a describes the dynamic behavior of a pendulum with mass M and length l, as shown in Fig. 1(a), deflected by an angle ϕ from an equilibrium state [19], [20]. A torque D applied to a pendulum corresponds to the applied bias current of a JJ, determining the initial state of the pendulum. An additional applied torque current rotates the pendulum, changing the angle ϕ. Damping the pendulum corresponds to the junction conductance $1/R$, while the moment of inertia corresponds to the junction capacitance. The angle ϕ from an equilibrium state and angular velocity correspond, respectively, to the phase difference within the JJ and voltage $V = \hbar/2e\, \mathrm{d}\phi/dt$. This mechanical analogy can be used to illustrate the dynamic behavior of a JJ. A fast kick of the pendulum rotates the pendulum, affecting a 2π change in phase from the initial equilibrium state to the next state, producing a voltage pulse.

Another mechanical analogy to describe the dynamic behavior of a Josephson junction is the "tilted washboard model" with the potential energy of a particle with a specific mass M and damping $\eta = \Phi_0/\mu_v$, where μ_v and Φ_0 are, respectively, the mobility and a single flux quantum [20]. In this analogy, the particle moves down a slope with a sinusoidally modulated height, another representation of a pendulum system. M is proportional to the junction capacitance C, and damping on a tilted washboard potential is proportional to the junction conductance $1/R$. The angle ϕ is folded horizontally, and the slope is proportional to the applied torque. If the current is larger than the critical current, the particle moves down the slope and reaches an equilibrium state, switching the phase of the junction by 2π.

B. Bistable Josephson Junction

The dynamic behavior of a $2\phi-$JJ as well as a standard JJ is described by the well known RCSJ model. The current passing through a bistable SFS JJ with a second harmonic is

$$i = I_{c1} sin(\phi) + I_{c2} sin(2\phi) + \frac{1}{R}.\frac{\hbar}{2e}\frac{d\phi}{dt} + c\frac{\hbar}{2e}\frac{d^2\phi}{dt^2} \quad . \tag{2}$$

If (2) is divided by $c\frac{\hbar}{2e}$, the current of a bistable JJ is

$$i = Asin(\phi) + Bsin(2\phi) + \alpha\dot{\phi} + \ddot{\phi} \quad , \tag{3}$$

where A and B are, respectively, the amplitude of the first and second harmonics in the CPR which are normalized to the critical current of junction I_c. In $2\phi-$JJs, A is negligible ($A \approx 0$), and α is the damping coefficient of the JJ and is ω_p/ω_c, where ω_p and ω_c are, respectively, the plasma frequency and Josephson junction characteristic frequency [12], [13], [21]. Both ω_p and ω_c depend upon the fabrication process, thickness of the ferromagnetic layer, and type of barrier within the junction. In this paper, the damping coefficient α of the bistable JJ is approximately one.

A mechanical analogy for describing the dynamic behavior of a bistable JJ is proposed here as a hyperbolic paraboloid system, as depicted in Fig. 1(b). This analogy can be used to illustrate phase switching and the equilibrium states of a bistable JJ, characterizing the dynamic behavior of all-JJ circuits. The potential function U(ϕ) for a mass moving along a circular path with radius r on the surface is

$$U(\phi) = r^2 cos(2\phi). \tag{4}$$

The potential energy of a mass traveling in a circle on a surface is proportional to the height of the surface, which is proportional to cos(2ϕ). The particle motion, adapted from [20], is

$$mr^2\frac{d^2\phi}{dt^2} = -mg\frac{\partial U(\phi)}{\partial\phi} - \eta\frac{d\phi}{dt} \quad . \tag{5}$$

An expression for the motion of the particle is suggested by substituting the potential energy into (5), yielding

$$\frac{d^2\phi}{dt^2} = gsin(2\phi) - \frac{\eta}{mr^2}\frac{d\phi}{dt} \quad . \tag{6}$$

Force $F = ma$ on the particle is proportional to the gradient of the potential energy which is represented by the sin(2ϕ) term. Two stable equilibrium states exist for a bistable JJ in the hyperbolic paraboloid system similar to the phase-current relationship of a JJ [12]. The phase difference between the two equilibrium states is π. A bistable JJ requires less bias current to move down the slope to achieve an equilibrium state. Based on the proposed mechanical analogy for a bistable JJ, a 2ϕ

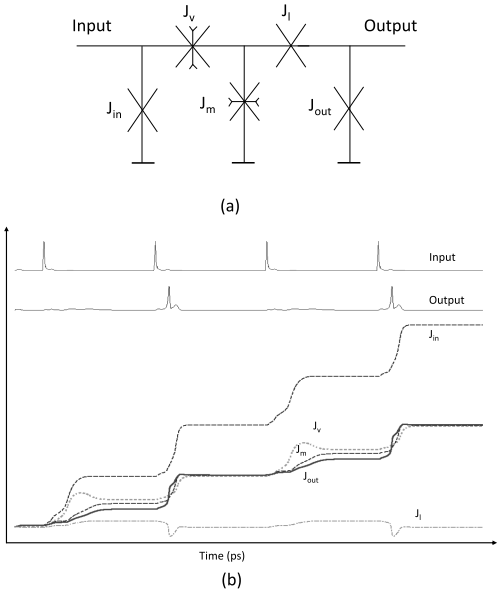

Fig. 2. All-JJ TFF, (a) circuit, and (b) operation; $J_{in} = 280\ \mu$A, $J_v = 150\ \mu$A, $J_m = 150\ \mu$A, $J_l = 350\ \mu$A, and $J_{out} = 150\ \mu$ A.

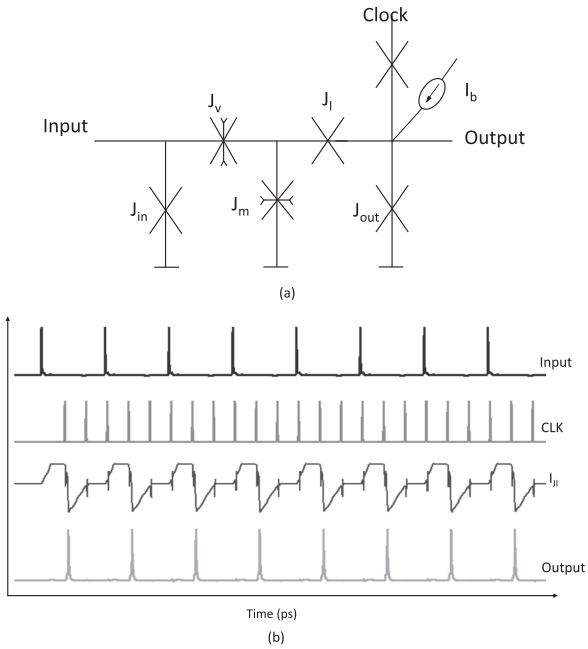

Fig. 3. All-JJ DFF, (a) circuit, and (b) operation; $J_{in} = 250\ \mu$A, $J_v = 200\ \mu$A, $J_m = 150\ \mu$A, $J_l = 450\ \mu$A, $J_{out} = 150\ \mu$A, and $I_b = 50\ \mu$A.

JJ switches when a π phase difference occurs across the JJ, producing a half flux quantum (HFQ) pulse. The HFQ pulse is half of an SFQ pulse, rotating the particle and switching the angle ϕ of the JJ by π rather than 2π. 2ϕ JJs therefore require only half an SFQ pulse to phase switch, enabling power efficient superconductive logic.

III. All-JJ Logic Cells

Several novel all-JJ logic cells are described in this section. The large inductor within the storage loop of a standard SFQ logic cell is replaced with two bistable JJs. The phase within each superconductive loop including the bistable JJs is 2πn, producing a circulating current to achieve the 2πn phase within the loop. The proposed gates are compared to equivalent standard SFQ logic elements in terms of delay and power. The proposed all-JJ logic circuits and a complex benchmark circuit are described in the following subsections.

A. Flip Flops

Standard SFQ flip flops are composed of a superconductive storage loop with a large inductor. These gates are typically clocked, where a logic one (zero) is represented as the presence (absence) of an SFQ pulse within the storage loop during each clock period. In all-JJ circuits, the large inductor within the storage loop is replaced with two bistable JJs. The operation of commonly used all-JJ flip flops, such as a D flip flop (DFF) and T flip flop (TFF), is described in this subsection.

1) TFF: A T flip flop is the basic storage loop operating as a frequency divider. The circuit diagram of an all-JJ TFF is depicted in Fig. 2(a). The TFF is adopted from [12]. The input loop is composed of a single standard JJ and two $2\phi-$JJs, J_v and J_m. The output loop operates as a Josephson transmission line, producing an SFQ pulse. The all-JJ TFF is composed of both bistable JJs and standard JJs. The operation of the all-JJ TFF is shown in Fig. 2(b) and is based on the phase difference of the JJs, requiring no bias current. A 2π phase change across a standard junction is equally distributed between the bistable $2\phi-$JJs, producing an HFQ pulse across the junction while changing the phase by π across each $2\phi-$JJ. After two input pulses, the $2\phi-$JJs provide a sufficient drop in phase across the standard JJs, J_l and J_{out}, moving down the slope to achieve an equilibrium state (see Fig. 1(b)), producing an SFQ pulse.

The bias margins and performance of the all-JJ TFF are further evaluated within a chain of all-JJ TFFs when used as a digital frequency divider. Significant distortion occurs within the TFF chain, causing the circuit to not function properly. Since no bias currents exist within the circuit, the SFQ pulse disappears after the third stage of the all-JJ TFF. A small bias current is added to eliminate reflections and amplify the SFQ pulse. Based on the proposed mechanical analogy for a bistable JJ, the small bias current moves the bistable JJ down the slope to achieve an equilibrium state (see Fig. 1(b)). This bias current enhances the operation of the TFF gates in complex systems while slightly improving the circuit margins.

2) DFF: A D flip flop with a destructive readout is one of the primary superconductive gates with a clock signal. The circuit diagram of an all-JJ DFF is depicted in Fig. 3(a). The DFF is adopted from [12]. All-JJ circuits are composed of bistable JJs, standard JJs, and bias currents. The bias current in the all-JJ DFF cell is 50 μA, significantly smaller than an SFQ DFF. The switching speed, critical currents, and damping coefficient of the bistable junctions determine the behavior of the all-JJ DFF cell. The parameters of the circuit are adjusted to operate at a frequency in the range between 1 GHz to 10 GHz based on the applied input and clock patterns. The operation of the all-JJ

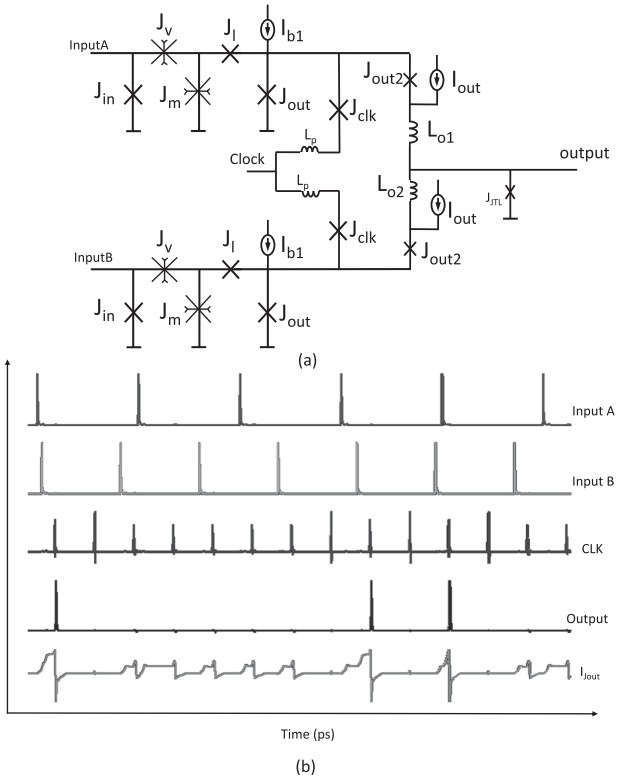

Fig. 4. All-JJ AND, (a) circuit, and (b) operation; $J_{in} = 250\ \mu$A, $J_v = 250\ \mu$A, $J_m = 120\ \mu$A, $J_l = 450\ \mu$A, $J_{out} = 270\ \mu$A, $II_{b1} = 180\ \mu$A, $L_p = 2$ pH, $J_{clk} = 150\ \mu$A, $L_{out} = 2$ pH, $I_{out} = 120\ \mu$A, $J_{out2} = 176\ \mu$A, and $J_{JTL} = 470\ \mu$A.

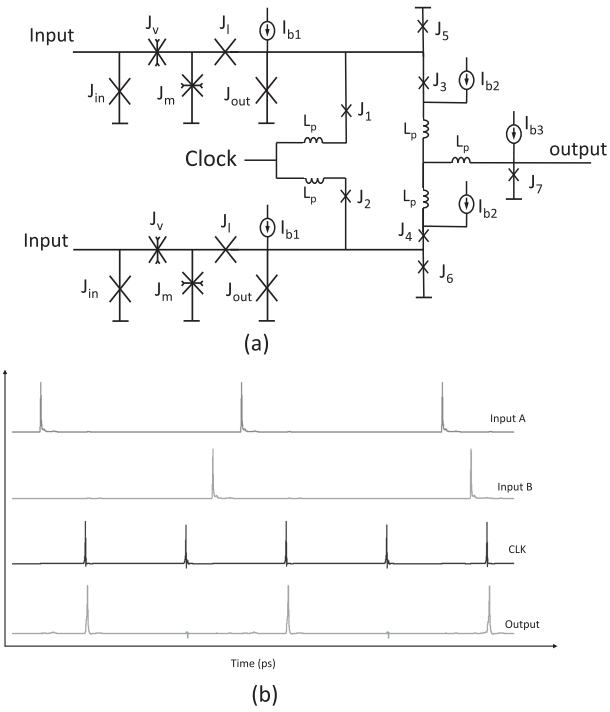

Fig. 5. All-JJ OR gate, (a) circuit and (b) operation; J $J_{in} = 250\ \mu$A, $J_v = 250\ \mu$A, $J_m = 150\ \mu$A, $J_l = 450\ \mu$A, $J_{out} = 270\ \mu$ A, II $_{b1} = 100\ \mu$A, $L_p = 2$ pH, $J_{1,2} = 120\ \mu$A, $J_{3,4} = 176\ \mu$A, $J_{5,6} = 180\ \mu$A, $I_{b2} = 200\ \mu$A, $I_{b3} = 40\ \mu$A, and $J_7 = 250\ \mu$ A.

DFF is shown in Fig. 3(b). Most of the bias current flows through J_{out}. Based on the proposed mechanical analogy for a bistable JJ, the first SFQ input pulse changes the phase across J_{out} to an unstable equilibrium state, defining the state as a "1" (see Fig. 1). To read the state of the DFF, a clock pulse is applied. This pulse switches both J_l and J_{out}. These JJs move down the slope to achieve an equilibrium state, producing an SFQ pulse, as shown in Fig. 3(b). The clock pulse in state "0" is removed by slightly changing the phase across J_{out}.

B. OR and AND Gate

An all-JJ AND gate and OR gate are shown, respectively, in Figs. 4(a) and 5(a). The all-JJ OR gate and all-JJ AND gate are composed of all-JJ DFFs to store an SFQ pulse when one and two inputs arrive. The large inductor within the storage loops in conventional OR and AND gates is replaced with bistable JJs. A primary challenge in the all-JJ OR and AND gates is pulse reflections at the clock ports. Small inductors in the all-JJ OR cell are placed at the clock input to eliminate these pulse reflections in the clock ports. Additional small inductors, L_1 and L_2, are placed within the all-JJ AND gate to manage the distribution of the reflected current at the input and clock ports, as shown in Fig. 4(a). The operation of the all-JJ AND gate and OR gate is shown, respectively, in Figs. 4(b) and 5(b). Due to the large critical current of J_{out}, the junction only switches when two pulses arrive. Inductances L_1 and L_2 within the all-JJ AND gate manage the current flow through J_{out} to ensure correct operation.

TABLE I
COMPARISON BETWEEN ALL-JJ AND STANDARD SFQ CELLS

	SFQ TFF	SFQ OR	SFQ TFF	SFQ OR	All-JJ TFF	All-JJ OR
Critical current density	10 kA/cm²	10 kA/cm²	1 kA/cm²	1 kA/cm²	1 kA/cm²	1 kA/cm²
Delay	5 ps	5 ps	10 ps	22 ps	6 ps	8 ps
Bias current	250 μA	650 μA	250 μA	610 μA	90 μA	350 μA
Loop inductance length	40 μm	80 μm	60 μm	120 μm	—	—

The all-JJ OR cell and all-JJ TFF are compared here to conventional SFQ circuits. The size of the inductor within the storage loop is listed in Table I. The all-JJ logic cells are smaller than standard SFQ logic cells with standard JJs – a storage loop is no longer required to store the SFQ pulse since the state of the cells is stored within the bistable JJs. The parameters of the all-JJ OR gate and all-JJ AND gate are adjusted to reduce the bias current. The bias current in the all-JJ OR/AND cells and conventional OR/AND cells is, respectively, 350 μA and 650 μA. The bistable JJs within the all-JJ gates require less bias current as compared to standard JJs to achieve an equilibrium state. The all-JJ OR gate and all-JJ AND gate therefore require smaller bias current than conventional OR/AND cells. The 2ϕ–JJ logic cells exhibit a significantly smaller delay than standard cells composed of standard JJs and inductors with the same critical current density. The delay of the all-JJ OR/AND cells and conventional OR/AND cells is, respectively, 22 and

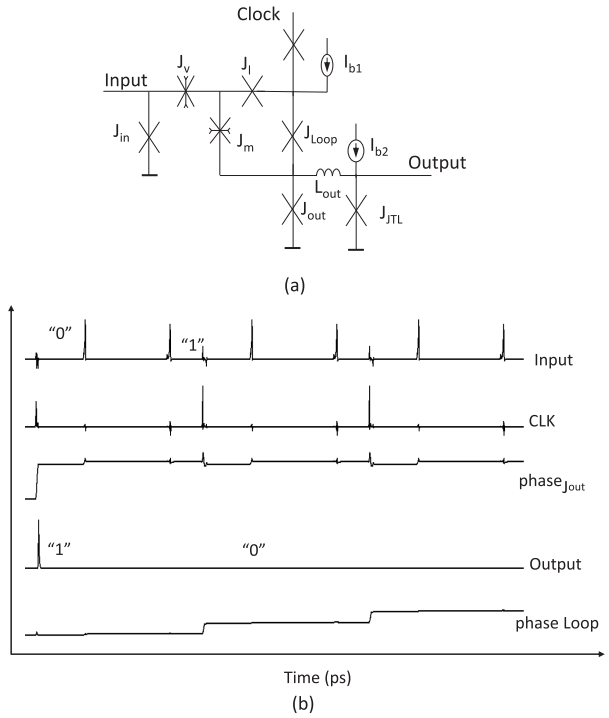

Fig. 6. All-JJ NOT gate, (a) circuit, and (b) operation; $J_{in} = 300\ \mu$A, $J_v = 170\ \mu$A, $J_m = 40\ \mu$A, $J_l = 200\ \mu$A, $J_{Loop} = 250\ \mu$A, $J_{out} = 200\ \mu$A, $J_{JTL} = 250\ \mu$A, $I_{b1} = 140\ \mu$A, $L_{out} = 4$ pH, and $I_{b2} = 145\ \mu$ A.

8 ps. The margins of the bias currents, I_{b1}, I_{b2}, and I_{b3}, of the OR gate are, respectively, ($\pm$10%), ($\pm$10%) and ($\pm$75%). The margins of the bias currents, I_{b1} and I_{out}, of the AND gate are, respectively, ($-$22%, +39%) and ($-$38%, +83%).

C. NOT

Data can be effectively inverted in all-JJ logic unlike in SFQ logic. The circuit diagram of an all $-$ JJ NOT gate is depicted in Fig. 6(a). The NOT gate is adopted from [12]. The NOT cell is enhanced by including a single stage JTL, bias current, and inductor, allowing the circuit to operate at a frequency in the range of 1 GHz to 25 GHz. The proposed inverter utilizes a linear inductor to manage the current distribution between the JJs while enhancing the margins. The proposed all-JJ inverter stores the input data in the storage loop, $J_{in}-J_v-J_m-J_{out}$, functioning similar to an all-JJ DFF. The clock pulse inverts the data during each clock period. The operation of the all-JJ inverter is shown in Fig. 6(b). In state "0," a clock pulse switches J_{out}, producing an SFQ pulse at the output. In state "1," J_{Loop} is switched by a clock pulse due to the phase difference across J_{Loop}.

D. c17 Circuit

A complex c17 circuit from the suite of ISCAS'85 benchmark circuits [22] is used here to compare the performance characteristics of all-JJ circuits with standard SFQ circuits. The circuit diagram of the c17 circuit is shown in Fig. 7. The c17 circuit includes six NAND gates. A single stage JTL is included at the input and output of each cell. The truth table expressions for

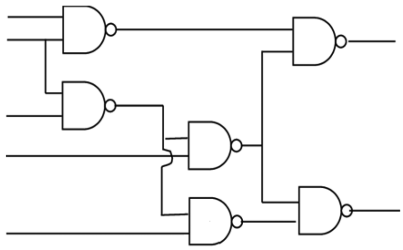

Fig. 7. c17 circuit from suite of ISCAS'85 benchmark circuits.

TABLE II
COMPARISON BETWEEN ALL-JJ AND STANDARD SFQ IN C17 BENCHMARK CIRCUIT

	SFQ c17	**all-JJ c17**
Critical current density	1 kA/cm^2	1 kA/cm^2
Delay (AND)	22 ps	8 ps
Delay (NOT)	20 ps	7 ps
Bias current	22 mA	13 mA
Loop inductance length	0.8 to 1 mm	–

the c17 circuit with five inputs and two outputs demonstrates the logical operation of the cell; $out_1 = (ab) + (\bar{b}d) + (\bar{c}d)$ and $out_2 = (\bar{b}d) + (\bar{c}d) + (\bar{b}e) + (\bar{c}e)$. The all-JJ circuit operates correctly for all combinations of inputs. A comparison between an all-JJ and standard SFQ c17 circuit is listed in Table II. By removing the storage loop inductors within the all-JJ logic cells, the all-JJ complex circuit is much smaller than the standard JJ circuit (with inductors). The bias current in the all-JJ version of the c17 circuit and conventional c17 circuit is, respectively, 13 mA and 22 mA. For the same critical current density, 1 kA/cm^2, the $2\phi-$ JJ logic cells exhibit a significantly smaller delay than standard SFQ cells composed of standard JJs and inductors. The delay of the NOT and AND cells within the conventional c17 circuit and all-JJ c17 circuit is, respectively, 20 and 22 ps and 7 and 8 ps.

IV. INDUCTANCE IN ALL-JJ CIRCUITS

Two sources of inductance exist in superconductive circuits; linear inductors and parasitic inductances, as depicted in Fig. 8, an example of a superconductive layout [23]. Inductive striplines are the primary type of connection between JJs in superconductive systems, affecting the distribution of current [8], [24], [25]. Vias connect the metal layers. These vias produce a parasitic inductance. These sources of inductance can also occur within all-JJ circuits, changing the performance characteristics such as the margins. The effects of the parasitic inductance are discussed in Section IV-A. To enhance the performance of all-JJ circuits, the effects of a linear inductance are described in Section IV-B.

A. Parasitic Inductances

Significant issues in large scale superconductive integrated circuits exist, such as limited metal resources and process variations [7], [26]. The connections between the metal layers in

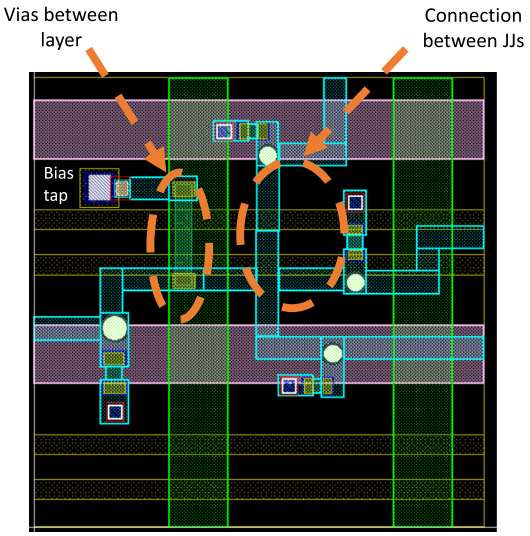

Fig. 8. Two sources of inductance within the layout of a superconductive circuit.

complex SFQ ICs produce a parasitic inductance. Due to resolution limitations and variations in the photolithography process, nonuniform shapes often occur in the striplines, producing an additional parasitic inductance while affecting the stripline characteristics. The parasitic inductance in series with the JJs disturbs the current distribution within all-JJ circuits while affecting the margins of the bistable JJs.

The operation of an all-JJ NOT gate is described for a range of parasitic inductances. A small inductance is placed in series with each Josephson junction to evaluate the effects of the parasitic inductance. This gate operates correctly with small margins for a parasitic inductance ranging from 0.01 to 0.1 pH. For a large parasitic inductance, ranging from 0.1 to 0.5 pH, the current distribution and operation of the all-JJ NOT gate are disturbed.

B. Linear Inductance

The connections between the JJs within all-JJ circuits can be modeled as a small parasitic linear inductor, disturbing the current distribution within these circuits. Undesired small inductors degrade performance while reducing margins, damaging the operation of superconductive systems.

To manage the current distribution and improve margins, linear inductances are placed within the all-JJ cells. The linear inductance within an all-JJ NOT gate simultaneously prevents reflected pulses at the input, suppressing the effects of the parasitic inductance on the SFS JJs by managing the current distribution within the circuit. A circuit diagram of an enhanced all-JJ NOT cell is shown in Fig. 9. This cell operates correctly for a parasitic inductance ranging from 0.5 to 1.5 pH and for a linear inductance L_L ranging from 2 to 4 pH. Parameter margins with these inductors are greater than $\pm 20\%$. The margins of the bias currents, I_{b1} and I_{b2}, of the NOT gate are, respectively, $(-18\%, +22\%)$ and $(-21\%, +24\%)$. These results indicate the importance of accurately extracting the linear and parasitic inductors.

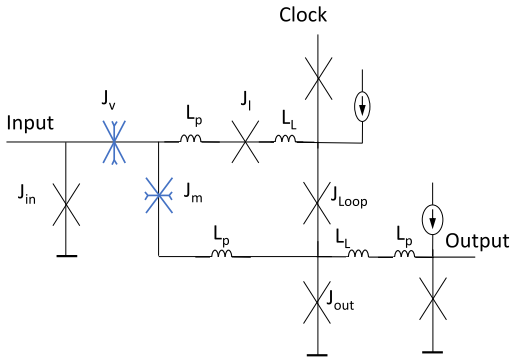

Fig. 9. Enhanced all-JJ NOT gate with two linear inductors and a parasitic inductance in series with the JJs.

V. Conclusion

All-JJ superconductive logic based on a bistable JJ enables nanometer feature sizes in VLSI complexity superconductive systems. All-JJ circuits do not require a large inductor within the storage loop. In this paper, a mechanical analogy is presented to describe the phase switching and dynamic behavior of a bistable JJ. Novel all-JJ logic gates, such as flip flops, OR, AND, and NOT gates, are presented. A complex all-JJ circuit, from the suite of ISCAS'85 benchmark circuits, is also characterized. All-JJ circuits exhibit approximately 13 ps less delay and 9 mA less bias current than standard SFQ cells (for the 10 kA/cm^2 MIT LL SFQ5ee fabrication process). The effects of the parasitic inductance and linear inductors on the operation of an all-JJ NOT cell are considered. Small linear inductors placed within the logic cells to manage the current distribution suppress the effects of the parasitic inductance, improving the parameter margins of the all-JJ circuits.

Acknowledgment

The content of the information does not necessarily reflect the position or the policy of the U.S. Government, and no official endorsement should be inferred.

References

[1] K. K. Likharev and V. K. Semenov, "RSFQ logic/memory family: A new Josephson-junction technology for sub-terahertz-clock-frequency digital systems," *IEEE Trans. Appl. Supercond.*, vol. 1, no. 1, pp. 3–28, Mar. 1991.

[2] S. V. Polonsky et al., "New RSFQ circuits (Josephson junction digital devices)," *IEEE Trans. Appl. Supercond.*, vol. 3, no. 1, pp. 2566–2577, Mar. 1993.

[3] G. Krylov and E. G. Friedman, *Single Flux Quantum Integrated Circuit Design*. Berlin, Germany: Springer, 2022.

[4] T. Jabbari and E. G. Friedman, "Global interconnects in VLSI complexity single flux quantum systems," in *Proc. Workshop Syst.-Level Interconnect: Problems Pathfinding Workshop*, 2020, pp. 1–7.

[5] Y. Ando, R. Sato, M. Tanaka, K. Takagi, N. Takagi, and A. Fujimaki, "Design and demonstration of an 8-Bit bit-serial RSFQ microprocessor: CORE E4," *IEEE Trans. Appl. Supercond.*, vol. 26, no. 5, Aug. 2016, Art. no. 1301205.

[6] T. V. Filippov et al., "20 GHz operation of an asynchronous wave-pipelined RSFQ arithmetic-logic unit," *Phys. Procedia*, vol. 36, pp. 59–65, Sep. 2012.

[7] S. K. Tolpygo, E. B. Golden, T. J. Weir, and V. Bolkhovsky, "Inductance of superconductor integrated circuit features with sizes down to 120 nm," *Supercond. Sci. Technol.*, vol. 34, no. 8, pp. 1–24, Jun. 2021.

[8] T. Jabbari and E. G. Friedman, "Flux mitigation in wide superconductive striplines," *IEEE Trans. Appl. Supercond.*, vol. 32, no. 3, Feb. 2022, Art. no. 3800306.
[9] T. Jabbari, G. Krylov, S. Whiteley, E. Mlinar, J. Kawa, and E. G. Friedman, "Interconnect routing for large scale RSFQ circuits," *IEEE Trans. Appl. Supercond.*, vol. 29, no. 5, Aug. 2019, Art. no. 1102805.
[10] T. Jabbari and E. G. Friedman, "Surface inductance of superconductive striplines," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 69, no. 6, pp. 2952–2956, Jun. 2022.
[11] T. Jabbari and E. G. Friedman, "Inductive and capacitive coupling noise in superconductive VLSI circuits," *IEEE Trans. Appl. Supercond.*, under review.
[12] I. I. Soloviev et al., "Superconducting circuits without inductors based on bistable Josephson junctions," *Phys. Rev. Appl.*, vol. 16, no. 014052, pp. 1–11, Jul. 2021.
[13] M. J. A. Stoutimore et al., "Second-harmonic current-phase relation in Josephson junctions with ferromagnetic barriers," *Phys. Rev. Lett.*, vol. 121, Oct. 2018, Art. no. 177702.
[14] A. Pal, Z. H. Barber, J. W. A. Robinson, and M. G. Blamire, "Pure second harmonic current-phase relation in spin-filter Josephson junctions," *Nature Commun.*, vol. 5, no. 3340, pp. 1–5, Feb. 2014.
[15] M. Weides et al., "0-π Josephson tunnel junctions with ferromagnetic barrier," *Phys. Rev. Lett.*, vol. 97, no. 24, Dec. 2006, Art. no. 247001.
[16] N. Pompeo et al., "Thermodynamic nature of the $0-\pi$ quantum transition in superconductor/ferromagnet/superconductor trilayers," *Phys. Rev. B*, vol. 90, Aug. 2014, Art. no. 064510.
[17] E. C. Gingrich et al., "Controllable 0-π Josephson junctions containing a ferromagnetic spin valve," *Nature Phys.*, vol. 12, pp. 564–567, Jun. 2016.
[18] I. Salameh, E. G. Friedman, and S. Kvatinsky, "Superconductive logic using 2ϕ–Josephson junctions with half flux quantum pulses," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 69, no. 5, pp. 2533–2537, May 2022.
[19] T. V. Duzer and C. W. Turner, *Principles of Superconductive Devices and Circuits*, 2nd ed., Englewood Cliffs, NJ, USA: Prentice-Hall, 1981.
[20] A. M. Kadin, *Introduction to Superconducting Circuits*. Hoboken, NJ, USA: Wiley, 1999.
[21] A. S. Vasenko, A. A. Golubov, M. Y. Kupriyanov, and M. Weides, "Properties of tunnel Josephson junctions with a ferromagnetic interlayer," *Phys. Rev. B*, vol. 77, Apr. 2008, Art. no. 134507.
[22] ISCAS85 benchmark circuits, Feb. 2022. [Online]. Available: https://www.filebox.ece.vt.edu/mhsiao/iscas85.html
[23] T. Jabbari, G. Krylov, J. Kawa, and E. G. Friedman, "Splitter trees in SFQ circuits," *IEEE Trans. Appl. Supercond.*, vol. 31, no. 5, Aug. 2021, Art. no. 1302606.
[24] T. Jabbari, G. Krylov, S. Whiteley, J. Kawa, and E. G. Friedman, "Repeater insertion in SFQ interconnect," *IEEE Trans. Appl. Supercond.*, vol. 30, no. 8, Dec. 2020, Art. no. 5400508.
[25] T. Jabbari and E. G. Friedman, "Stripline topology for flux mitigation," *IEEE Trans. Appl. Supercond.*, vol. 33, no. 5, Aug. 2023, Art. no. 1500604.
[26] S. S. Meher, C. Kanungo, A. Shukla, and A. Inamdar, "Parametric approach for routing power nets and passive transmission lines as part of digital cells," *IEEE Trans. Appl. Supercond.*, vol. 29, no. 5, Aug. 2019, Art. no. 1101307.