SFQ/DQFP Interface Circuits

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***Abstract*—The increasing complexity of hybrid superconductive computing systems has made interface circuits between logic families an issue of growing importance. In this paper, interface circuits between single flux quantum (SFQ) and directly coupled quantum flux parametron (DQFP) logic families to achieve high speed, low power hybrid superconductive computing systems are presented. In the proposed DQFP-to-SFQ interface, margins greater than ±20% for the critical current of the JJs, bias currents, and inductances are exhibited. The margins of the excitation current of the DQFP buffer are −38% and +35% with the frequency of the excitation current in the range of 2 GHz to 10 GHz. In the proposed SFQ-to-DQFP interface, the margins are greater than −33% and +25%. The margins of the excitation current of the DQFP buffer are −50% and +20% for frequencies ranging from 2 GHz to 10 GHz. Since no transformers are required, the physical area of the adiabatic portion of the interface circuits is significantly less than existing interface circuits. The SFQ-to-DQFP interface circuit operates at frequencies approaching 20 GHz. These interface circuits therefore exhibit high parameter margins and operating frequencies while requiring significantly less area as compared to existing interface circuits. The proposed interface circuits support the use of both ultra-low power and high speed logic families in complex hybrid superconductive systems.**

***Index Terms*—Adiabatic quantum flux parametron, directly coupled quantum flux parametron, single flux quantum, superconductive integrated circuits.**

I. Introduction

SUPERCONDUCTIVE electronics is a highly promising, albeit cryogenic, beyond CMOS technology for prospective exascale computing systems, which enable ultra-low power and ultra-high speed integrated circuits [1], [2], [3], [4], [5]. Superconductive single flux quantum (SFQ) technology exhibits switching delays on the order of a few picoseconds and switching energies of approximately 10^{-19} Joules [2], [6], [7]. Superconductive SFQ technology has been demonstrated to operate at frequencies approaching 80 GHz for an RSFQ arithmetic logic unit with an 8 bit datapath [8]. Adiabatic superconductive circuits, such as adiabatic quantum flux parametron (AQFP) [9], [10], [11], [12], [13], [14], [15] and directly coupled quantum flux parametron (DQFP) [16], [17], [18], are highly energy efficient logic families. The dynamic power consumption of AQFP circuits is reduced by adiabatic operation to a switching energy of $0.03 \times I_c\Phi_0$, where I_c and Φ_0 are, respectively, the critical current of a Josephson junction (JJ) and a single flux quantum. AQFP circuits dissipate two to three orders of magnitude lower power than SFQ circuits. AQFP circuits however typically operate at much lower frequencies than SFQ circuits.

A hybrid computing system, composed of both SFQ and AQFP logic families, provides both ultra-high speed and extremely low power operation. Interface circuits are therefore required to transfer data between the SFQ and AQFP circuitry. A standard AQFP-to-SFQ interface includes eleven Josephson junctions (JJs) and two transformers, requiring significant bias current and physical area [19], [20]. These standard AQFP/SFQ interface circuits also exhibit narrow parameter margins and operate at low frequencies. To achieve high speed, hybrid computing systems, enhanced AQFP/SFQ interface circuits are desirable to transfer data between the AQFP and SFQ circuitry. These circuits should require low area, exhibit effective parameter margins, and operate at high frequencies.

In this paper, interface circuits between adiabatic logic circuits and SFQ logic circuits are proposed. Directly coupled quantum flux parametron logic is reviewed in Section II. A novel DQFP-to-SFQ interface requiring less area and improved parameter margins is described in Section III. A novel SFQ-to-DQFP interface is proposed in Section IV. The effects of the circuit parameters on the performance of the DQFP-to-SFQ and SFQ-to-DQFP interfaces are also described, respectively, in Sections III and IV. The paper is concluded in Section V.

II. DQFP Logic

Directly coupled quantum flux parametron (DQFP) logic is power and area efficient. DQFP logic operates adiabatically, similar to AQFP logic [9], [16], [17], [21]. Due to adiabatic switching, DQFP dissipates bit energy per switching similar to AQFP [17]. An AQFP buffer gate is shown in Fig. 1(a). Standard AQFP logic uses signal transformers to propagate and invert the output current, requiring significant area [9], [10], [11], [21]. A DQFP buffer gate is shown in Fig. 1(b). Unlike AQFP, however, DQFP logic inverts and transfers the output current without requiring signal transformers, thereby requiring significantly less area [16], [17], [18]. The DQFP buffer is composed of two RF superconductive quantum interference device (SQUID) loops with a shared inductance L_q [9], as shown in Fig. 1(b). Characterization of the JJs within the DQFP buffer is based on the 10 kA/cm^2 MIT Lincoln Laboratory SFQ5ee fabrication process [22]. The JJs are not damped with resistors to achieve extremely low energy consumption [14]. When the AC excitation current I_x increases, either J1 or J2 switches,

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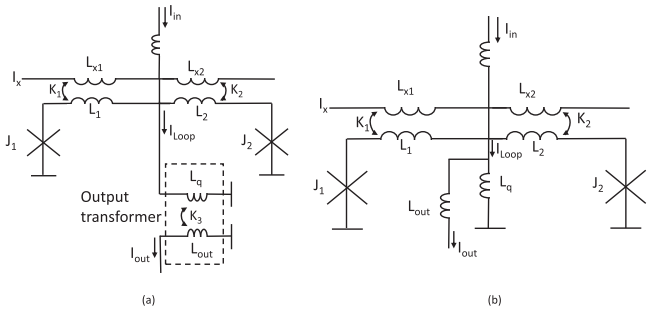

Fig. 1. Buffer logic circuit, (a) AQFP, and (b) DQFP. $L_{x1,2} = 2.1$ pH, $L_{1,2} = 1.3$ pH, $K_{1,2} = 0.35$, J1 = J2 = 200 μA, $L_q = 10.2$ pH, $K_3 = 0.6$, $L_{out_{AQFP}} = 10$ pH, and $L_{out_{DQFP}} = 1.5$ pH.

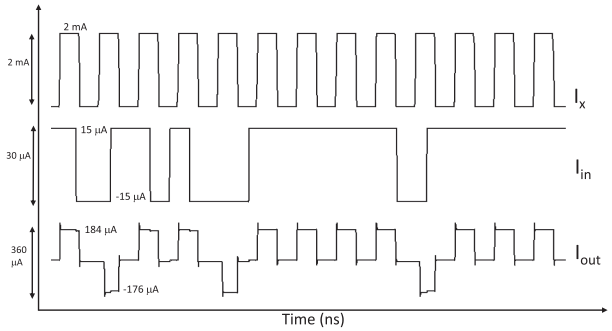

Fig. 2. Operation of DQFP buffer with large JJs. I_x, $I_{\rm in}$, and $I_{\rm out}$ are, respectively, the AC excitation current, input current, and DC output current. The output current $I_{\rm out}$ of the DQFP buffer is $\sim$180 μA.

producing current through L_q and $L_{\rm out}$ depending upon the direction of the input current $I_{\rm in}$. A current I_{Loop} is produced within the loop, setting the state of the buffer. The DQFP buffer is area efficient. Unlike an AQFP buffer, $I_{\rm out}$ can be directly transferred to the next stage without a transformer. The state of the buffer is set by the direction of the loop current I_{Loop}, as with AQFP logic.

The output of the DQFP buffer is shown in Fig. 2. The frequency of the excitation current is 2.5 GHz. The output pulse $I_{\rm out}$ is a DC current directly connected to the next stage of either a DQFP or AQFP circuit. The magnitude of the output current is dependent upon the output inductor $L_{\rm out}$, JJs, and inductor L_q within the SQUID loops. The JJs within the DQFP buffer are typically large to produce a high DC output current within the AQFP/DQFP-to-SFQ interface. The operation of the DQFP buffer with these large JJs ($I_c = 200$ μA) is shown in Fig. 2 when connected to the DQFP buffer at the input and output ports. The output current $I_{\rm out}$ of the DQFP buffer is $\sim$180 μA.

III. DQFP-to-SFQ Interface

An AQFP-to-SFQ interface circuit [19], [20] transfers data from an adiabatic circuit to an SFQ circuit in a hybrid superconductive digital system. Standard interfaces [19], [20], [23] exhibit small parameter margins, particularly for the JJs within the SFQ portion of the interface, while requiring significant area for the transformer within the AQFP buffer. In the proposed

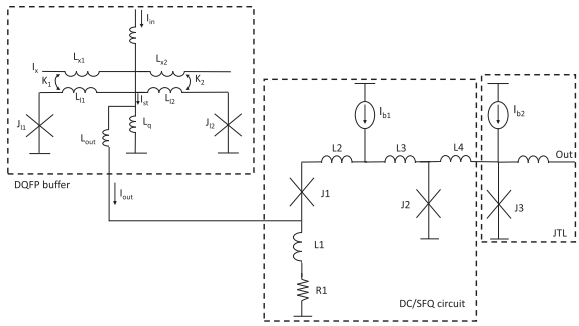

Fig. 3. Proposed DQFP-to-SFQ interface. $L_{x1,2} = 2.1$ pH, $L_{1,2} = 1.3$ pH, $K_{1,2} = 0.35$, J1 = J2 = 200 μA, $L_q = 10.4$ pH, $L_{out_{DQFP}} = 1.5$ pH, J1 = 158 μA, J2 = 80 μA, J3 = 250 μA, L1 = 5.7 pH, L2 = 0.5 pH, L3 = 1 pH, L4 = 10 pH, L5 = 2 pH, $R_1 = 1$ mΩ $I_{b1} = 115$ μA, and $I_{b2} = 220$ μA.

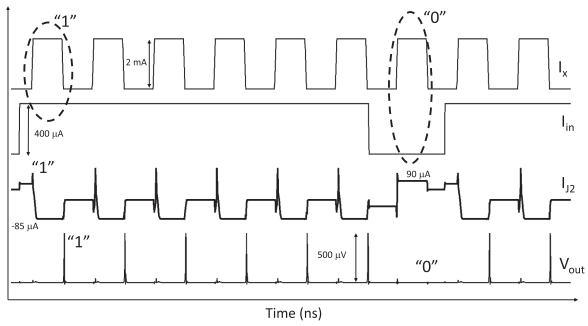

Fig. 4. Waveform characteristics of DQFP-to-SFQ interface. I_x and $I_{\rm in}$ are, respectively, the AC excitation current and input current of the DQFP buffer. I_{J2} is the DC current through junction J_2. In logic state "1" of the DQFP buffer, junction J_2 switches, producing an SFQ pulse. $V_{\rm out}$ is the SFQ output pulse of the DQFP-to-SFQ interface.

DQFP-to-SFQ interface, the AQFP buffer is replaced with a DQFP buffer. The DQFP buffer transfers output current without requiring transformers, reducing the area of the adiabatic portion of the circuit. The interface also exhibits wider parameter margins.

The proposed DQFP-to-SFQ interface is shown in Fig. 3. The interface is composed of a DQFP buffer and a DC-to-SFQ interface. Three JJs are used in the SFQ portion of the DQFP-to SFQ interface, requiring no signal transformers between the DQFP buffer and the SFQ portion. The output of the DQFP buffer is a DC current. To produce an SFQ pulse, a DC-to-SFQ converter is directly connected to the output of the DQFP buffer. The output of the DQFP-to-SFQ interface is shown in Fig. 4. The frequency of the excitation current is 2.5 GHz. In state "1," where the current at the input of the DC-to-SFQ circuit increases, the DC current through junction J_2 exceeds the critical current, switching the junction. Junction J_3 operates as a single stage Josephson transmission line (JTL) [7] at the output of the DQFP-to-SFQ interface.

The magnitude of the output current of the DQFP buffer $I_{\rm out}$ affects the performance of the interface. A standard DC-to-SFQ interface operates with a large DC input current [24], [25]. The output DC current of the DQFP and AQFP buffer is dependent upon the size of the JJs. Large JJs with a critical current of 200 μA

are used within standard AQFP-to-SFQ interfaces [20]. For the DQFP buffer to provide greater DC output current, larger JJs are also used within the DQFP buffer (see Section II). The DC-to-SFQ interface within the proposed DQFP-to-SFQ interface targets an input current ranging from 60 μA to 160 μA.

The DC-to-SFQ converter at the output of the DQFP-to-SFQ interface produces a small offset current within the loops of the DQFP buffer due to the two bias currents, I_{b1} and I_{b2}. This offset current disturbs the operation of the DQFP buffer. To manage this offset current, inductors L_1, L_2, and L_3 are designed to minimize the offset current ($L_2 \gg L_3$ and $L_{\text{out}} \gg L_1$). A large L_2 directs bias current I_{b_1} to flow through L_3 and J_2. The current through L_2 flows through small inductor L_1 rather than L_{out}, reducing the offset current. Increasing the input current I_{in} by connecting to the DQFP buffer with large JJs (see Section II) lowers the offset current within the loops of the DQFP buffer.

For small inductance L_4, the input DC current is divided between junctions J_2 and J_3, reducing the negative margin of the input DC current. A large inductance L_4 passes the input DC current through junction J_2 while increasing the overall delay of the DC-to-SFQ converter. The output delay of the SFQ part is 8.5 ps. A tradeoff therefore exists between the negative margin of the input DC current and the signal delay.

The DQFP-to-SFQ interface achieves wider margins as compared to a standard AQFP-to-SFQ interface. The standard AQFP-to-SFQ interface exhibits less than $\pm 10\%$ parameter margins for those JJs in the SFQ portion of the circuit [20], [23]. The distribution of bias currents in the SFQ portion and the offset current within the DQFP buffer significantly suppress the parameter margins. The effects of these currents on the margins within the proposed DQFP-to-SFQ interface can be improved to at least $\pm 20\%$ by adjusting L_1, L_2, L_3, and L_4. The margins of the excitation current of the DQFP buffer are -38% and +35% with the frequency of the excitation current in the range of 2 GHz to 10 GHz. The margins of J_1 and J_2 are, respectively, $\pm 20\%$ and (-40% and +62%). The margins of the bias current I_{b1} are -35% and +20%. The margins of the input inductor L_1 are -26% and +40%. The margins of inductors L_2 to L_4 are -90%, +100%.

IV. SFQ-to-DQFP Interface Circuit

An SFQ-to-DQFP interface transfers data from an SFQ circuit to an adiabatic circuit. A standard SFQ-to-AQFP interface [19] is composed of two parts, an SFQ part and an AQFP part. These two parts are connected by a transformer [19] which requires significant area. The standard interface also exhibits narrow margins for the JJs within the SFQ part and a low operating frequency [19], [23]. An SFQ-to-DQFP interface with wider parameter margins and higher operating frequencies is proposed here. In this interface, the AQFP buffer is replaced with a DQFP buffer, and no transformers are necessary.

The proposed SFQ-to-DQFP interface is composed of an SFQ-to-DC converter [24] and DQFP buffer, as shown in Fig. 5. The SFQ-to-DC converter is at the input of the interface and produces a DC output voltage. The output characteristics of the SFQ-to-DC converter are composed of a series of SFQ pulses. The output of the SFQ-to-DC converter is directly connected to the DQFP buffer (see Fig. 5).

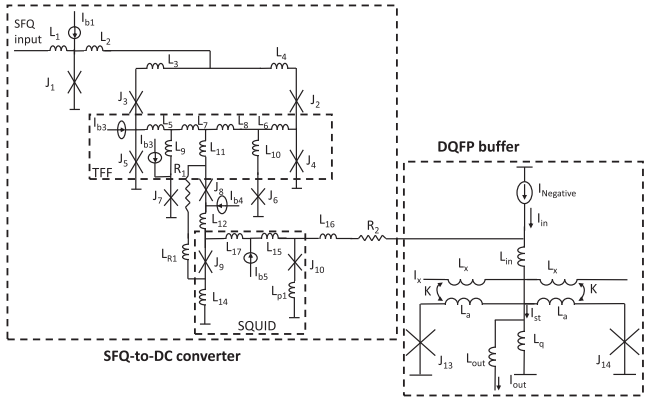

Fig. 5. Proposed SFQ-to-DQFP interface. L $_x$ = 2.1 pH, L_a = 1.46 pH, $K_{1,2} = 0.35$, J1 = J2 = 200 μA, L $_q$ = 12.4 pH, $L_{out_{DQFP}}$ = 2 pH, $L_{in_{DQFP}}$ = 15.3 pH, R2 = 1.5 ω, and $I_{Negative} = -20$ μA.

The SFQ-to-DC interface includes a T flip flop (TFF) at the input and a SQUID loop at the output (see Fig. 5). The incoming pulse stores a flux quantum inside the TFF. Due to the stored flux quantum and current within the TFF, the JJs within the SQUID, J_9 and J_{10} are biased above the critical current to produce a series of SFQ voltage pulses. The average of these pulses is a DC voltage. The next incoming SFQ pulse releases the stored flux within the TFF. The JJs within the SQUID are biased below the critical current. The circuit produces zero voltage (the absence of an SFQ pulse) at the output.

To produce both logic states within the DQFP buffer of the SFQ-to-DQFP interface, a bidirectional DC current at the input of the DQFP buffer is required. The SFQ portion of the SFQ-to-DQFP interface, the SFQ-to-DC converter, provides a positive DC current to produce logical state "1" within the DQFP buffer. An additional negative DC current $I_{Negative}$ is added at the input of the DQFP buffer to produce logical state "0" within the DQFP buffer. Both states of the DQFP buffer are synchronized by the excitation current I_x.

The output of the SFQ-to-DQFP interface is shown in Fig. 6. The frequency of the excitation current is 2.5 GHz. To provide a small DC current at the output of the DQFP buffer, small JJs with a critical current of 50 μA are used within the DQFP buffer. With these small JJs, the peak-to-peak magnitude of the output current $I_{out-DQFP}$ of the SFQ-to-DQFP interface is approximately 100 μA.

The SFQ-to-DC converter within the interface produces an offset current as well as fluctuations within the inductive loops of the DQFP buffer. These fluctuations occur due to the series of SFQ pulses at the output of the SFQ-to-DC converter. To manage the offset current and fluctuations, a resistor is placed in series with the output inductance of the SFQ-to-DC circuit.

The effects of the resistor on the performance of the SFQ-to-DQFP interface are shown in Fig. 7(a) and (b). The slow decay time – the time to achieve sufficient negative current – of the current due to the small resistor (see Fig. 7(a)) produces incorrect

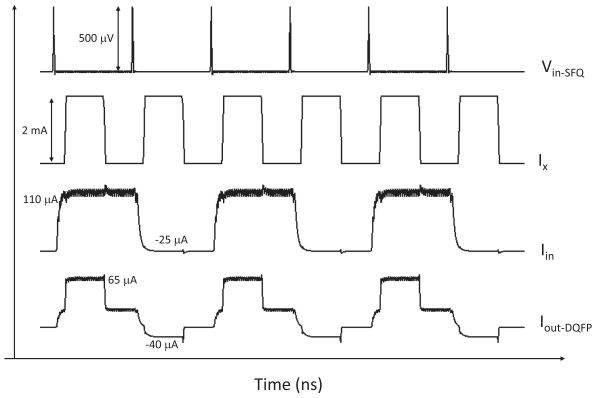

Fig. 6. Operation of SFQ-to-DQFP interface. V_{in-SFQ} is the input of the SFQ-to-DQFP interface. I_x and $I_{in-DQFP}$ are, respectively, the AC excitation current and input current of the DQFP buffer. $I_{out-DQFP}$ is the DC output current of the SFQ-to-DQFP interface.

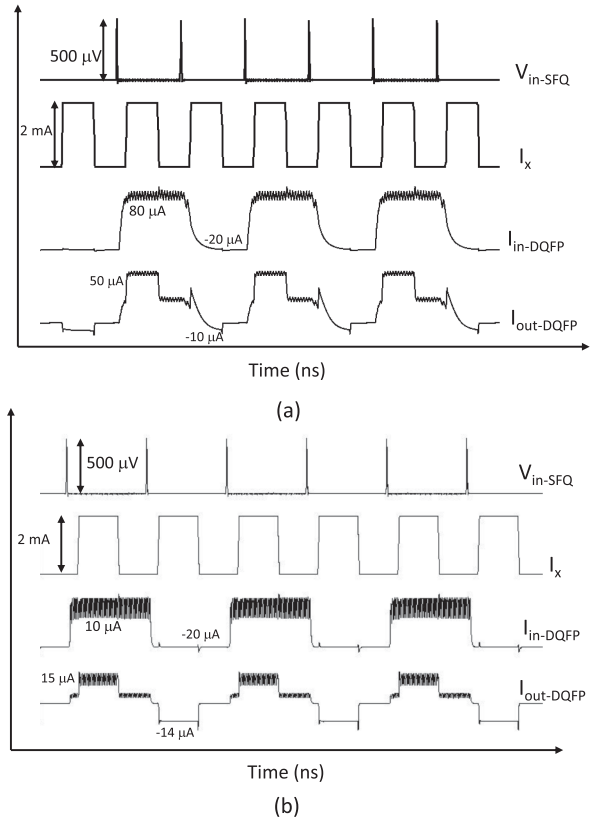

Fig. 7. Effects of the resistor within the SFQ-to-DQFP interface, (a) small resistor, and (b) large resistor. V_{in-SFQ} is the input of the SFQ-to-DQFP interface. I_x and $I_{in-DQFP}$ are, respectively, the AC excitation current and input current of the DQFP buffer. I_{out} is the DC output current of the SFQ-to-DQFP interface. The small resistor lowers the signal fluctuations while increasing the decay time.

operation within the SFQ-to-DQFP interface when operating at high frequencies while decreasing the signal fluctuations in the input signal of the DQFP buffer. A large resistor decays the signal more quickly while increasing the fluctuations at the input of the DQFP buffer (see Fig. 7(b)). A tradeoff therefore exists between the decay time and the signal fluctuations.

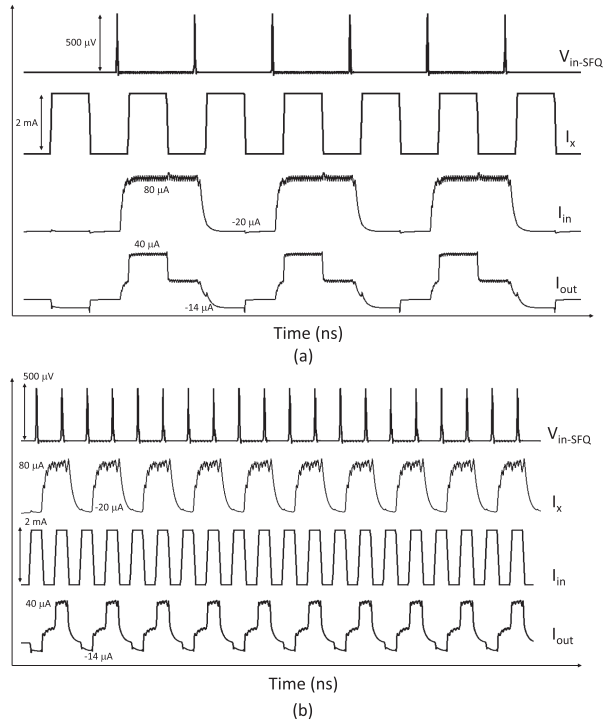

Fig. 8. Operation of the proposed SFQ-to-DQFP interface, (a) 2 GHz, and (b) 10 GHz. V_{in-SFQ} is the input SFQ pulse of the SFQ-to-DQFP interface. I_x and I_{in} are, respectively, the AC excitation current and input current of the DQFP buffer. I_{out} is the DC output current of the SFQ-to-DQFP interface.

The operating frequency of the SFQ-to-DQFP interface is also impacted by the resistor. A large resistor produces a shorter decay time while increasing fluctuations in the signal (see Fig. 7(b)). Due to the short decay time, the SFQ-to-DQFP interface with a large resistor can operate at a higher frequency, up to 20 GHz.

The resistor at the input of the DQFP buffer significantly affects the parameter margins. A small resistor improves the margins of all of the parameters. A 1 Ω resistor effectively removes any offset currents and fluctuations within the DQFP buffer while not significantly degrading the operation of the interface. The waveform characteristics of the proposed SFQ-to-DQFP interface at 2 GHz and 10 GHz are, respectively, illustrated in Fig. 8(a) and (b). In the proposed SFQ-to-DQFP interface, the margins of all of the parameters including the bias currents, inductors, and JJs are greater than −33% and +25%. The margins of the excitation current of the DQFP buffer are −50% and +20% from 2 GHz to 10 GHz. Future research to enhance the interface and verify the advantages in terms of the area, margins, and operating frequency include parameter optimization, physical design, and post-layout parameter extraction.

V. Conclusion

Superconductive digital circuits utilizing different logic families require an interface. Interfaces between superconductive adiabatic logic and SFQ logic are presented in this paper. The interfaces exhibit small area, wide margins, and high operating frequencies as compared to standard SFQ/AQFP interfaces.

A DQFP buffer is used rather than an AQFP buffer, significantly reducing area. In the DQFP-to-SFQ interface, the parameter margins are greater than $\pm 20\%$. The margins in the SFQ-to-DQFP interface are greater than -33% and $+25\%$. The SFQ-to-DQFP interface operates at frequencies approaching 20 GHz. Tradeoffs for the proposed interfaces among the delay, parameter margins, decay time, and signal fluctuations are also discussed.

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