Inductive and Capacitive Coupling Noise in Superconductive VLSI Circuits

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***Abstract*—The increasing complexity of modern superconductive circuits, and single flux quantum (SFQ) circuits in particular, has made the issue of coupling noise of growing importance. Limited metal resources within superconductive circuits have exacerbated this issue. In this article, the different sources of coupling noise within SFQ circuits are described. Coupling noise among inductors, routing striplines, and bias microstriplines within SFQ circuits degrade performance while decreasing margins. In this article, inductive and capacitive coupling between the different layers are characterized. Inductive coupling models between different layers in the MIT LL SFQ5ee process match experimental data within 3%. The dependence of inductive coupling on the thickness of the oxide and metal layer is also discussed. An understanding of inductive and capacitive coupling can determine the minimum physical distance between lines. In addition, tradeoffs exist among inductive coupling, capacitive coupling, layout complexity, and the vias between ground layers. The different coupling sources are characterized, and guidelines are provided to enhance the automated routing process.**

***Index Terms*—Automated layout, coupling noise, electronic design automation (EDA), superconductive integrated circuits.**

I. Introduction

RECENT advances in fabrication technology and electronic design automation (EDA) have enabled a fully planarized, eight niobium (Nb) layer process for superconductive circuits with Nb/Al-AlO_x/Nb Josephson junctions (JJs) with a 10-kA/cm^2 (100 μ A/μm^2) critical current density. The fabrication process supports the increasing integration of rapid single flux quantum (RSFQ) circuits exceeding 4.2×10^6 Josephson junctions (JJs) per cm^2 with a minimum feature size of 150 nm [1], [2], [3]. Recent complementary research in superconductive technology has developed SFQ-based EDA tools to enable the automated design of complex RSFQ circuits [4], [5], [6], [7], [8], [9], [10], [11], [12]. Smaller feature sizes enhance circuit densities but limited metal resources introduce design challenges. Closely spaced striplines in very large scale integration (VLSI) complexity RSFQ circuits increase coupling noise between the lines. Characterization of inductive and capacitive coupling between different layers is therefore desirable to support the development of advanced superconductive systems.

One of the primary requirements for SFQ-based automated routing is accurate impedance characterization of the striplines and microstriplines [2], [13]. The parasitic coupling between superconductive microstriplines for certain geometries is negligible due to the ground layer structure [14], [15]. The coupling noise plays a significant role in the line impedance and resonance behavior of striplines within large scale integrated SFQ systems [6], [16], [17], [18]. As metal resources are limited, striplines are often asymmetric with two signal lines between two ground planes, increasing the coupling noise between the lines. This structure produces different line characteristics, as described by the self- and mutual inductance and capacitance. Inductive and capacitive coupling in superconductive circuits is dependent upon the structure of the lines, vertical distance to the ground layers, separation between lines in the same and different layers, thickness of the line, and overlap between lines within different layers. Due to the imperfect nature of fabrication processes, nonuniform thickness of the striplines and dielectric oxides can occur [1], [3]. This feature also changes the characteristics of the lines, such as the self- and mutual inductance and capacitance. The thickness of the striplines and dielectric oxides also affects the inductive and capacitive coupling in superconductive circuits. Specialized guidelines are therefore required to support accurate inductive and capacitive coupling analysis for fabrication processes to determine the minimum physical space between lines in VLSI complexity SFQ circuits.

In this article, inductive and capacitive coupling between different lines in superconductive systems is described. The rest of this article is organized as follows. The sources of coupling noise are discussed in Section II. Inductive coupling is presented in Section III. Capacitive coupling between striplines is presented in Section IV. The effects of capacitive coupling noise on the operation and resonance behavior of an SFQ circuit are discussed in Section V. Guidelines and tradeoffs are also provided in Sections III–V. Finally, Section VI concludes this article.

II. Coupling Noise in Superconductive ICs

Multiple sources of inductive and capacitive coupling noise exist in superconductive ICs in the eight layer niobium MIT Lincoln Laboratory SFQ5ee technology. For example, inductive and capacitive coupling occurs between the microstriplines and

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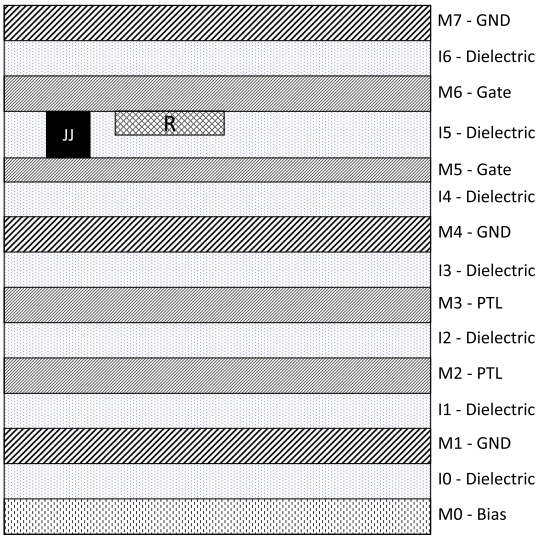

Fig. 1. MIT LL SFQ5ee technology [2], [19].

striplines. This noise degrades the performance of large scale systems while decreasing margins. Noise coupling between two superconductive lines has yet to be fully evaluated for multi-layered Nb ICs. In this section, noise between different lines is discussed. A superconductive IC with eight Nb layers in the MIT LL SFQ5ee process [2], [18], [19], [20] is schematically shown in Fig. 1. Metal resources are severely limited in this modern superconductive technology, as depicted in this figure. The routing lines and inductors are striplines. The striplines are placed between two ground planes, which act as nearby return paths for the magnetic currents. The stripline is separated from the lower and upper ground planes by a dielectric layer. The inductors and routing striplines are placed, respectively, in the M5 and M6 layers and M2 and M3 layers. The width of a passive transmission line (PTL) is 5.2 μm. SFQ signals propagating through the striplines can couple to other lines, producing noise. The bias lines placed in the M0 layer are microstriplines. A microstripline is also separated from the upper ground plane and the M1 layer by a dielectric layer. The width of the bias lines in the MIT Lincoln Laboratory SFQ5ee process is 1.8 μm [19]. Bias lines carrying high current can also affect the operation of the PTL. Characterizing local coupling noise between the PTL lines and bias lines is therefore necessary.

One of the primary issues in SFQ-based automated routing algorithms is the magnitude of the inductive and capacitive coupling noise between lines [8]. Electromagnetic simulators, such as Sonnet [21], can be used to provide an accurate estimate of the impedance and noise characteristics. These characteristics depend upon certain material parameters, such as the surface inductance L_s of the superconductive material. The surface inductance of a stripline is analytically described in [22]. Expressions for the surface inductance of a stripline provide an accurate estimate of the self- and mutual inductance and capacitance between superconductive lines [22]. The mutual inductance of several structures at different distances from the stripline to the ground layers, evaluated in Sonnet, is listed in Table I. These results match experimental data within 3%, less than the standard deviation of the experimental data [23]. The mutual inductance of these striplines, evaluated by a commercial 3-D inductance extractor (FastHenry) [8], is also listed in Table I. These results match experimental data within 7% [8]. The noise characteristics of striplines based on expressions for the surface inductance therefore provide an accurate estimate of the mutual inductance between striplines [22]. Estimates of the self- and mutual inductance can be used as guidelines for automated routing tools and for the placement of standard cells within VLSI complexity SFQ circuits.

TABLE I
MUTUAL INDUCTANCE OF DIFFERENT STRIPLINE STRUCTURES

Coupled striplines	Mutual inductance, pH, experimental [?]	Experimental standard deviation %	Mutual inductance, pH, Sonnet	Error %	Mutual inductance, pH, FastHenry [?]	Error %
M4-M5-M7, M4-M6-M7	1.95	1.43	1.97	+1.09	1.89	-3.2
M3-M4-M7, M3-M5-M7	2.75	2.89	2.82	+2.67	2.94	+6.9
M2-M3-M7, M2-M4-M7	3.04	2.04	3.09	+1.60	3.13	+3.0
M1-M2-M7, M1-M3-M7	3.27	0.90	3.256	+0.42	3.30	+0.9
M0-M1-M7, M0-M2-M7	3.37	1.12	3.354	+0.47	3.58	+6.2

III. INDUCTIVE COUPLING BETWEEN DIFFERENT LAYERS

Inductive coupling between lines in different layers degrades the performance of superconductive circuits while reducing margins. Inductive coupling between different layers is evaluated in Sonnet based on a π model. Different line structures exhibit different inductive coupling noise characteristics. In this section, the effects of inductive coupling noise are characterized to determine the minimum space between the routing and bias lines, enhancing the robustness of the routing structures used within VLSI complexity SFQ circuits. In Section III-A, inductive coupling in PTL interconnect lines is described. The dependence of the inductive coupling on the length of the PTL, thickness of the inductors in the logic gates, width of the ground layers, and number of vias between ground layers is described in Section III-A. Inductive coupling between the PTL lines and bias lines and between the PTL lines and inductors within the logic cells is also discussed in Section III-B. The dependence of inductive coupling on the thickness of the inductors in logic gates is also described in this section. In Section III-C, the noise characteristics of the bias lines due to coupling to the PTLs and logic inductors are described, and design tradeoffs to enhance the bias networks are presented.

A. Same Layer and Adjacent Layer Coupling

Different parameters of a layout can affect the coupling characteristics of a PTL. These parameters are the separation between PTLs, length of PTLs, thickness of the striplines, width of the ground layers, and number of connecting vias between the ground layers. The dependence of the PTL coupling characteristics on these parameters is described in this section.

Inductive coupling between PTL striplines in the same layer and adjacent layers is shown in Fig. 2(a). PTLs in the M2 and

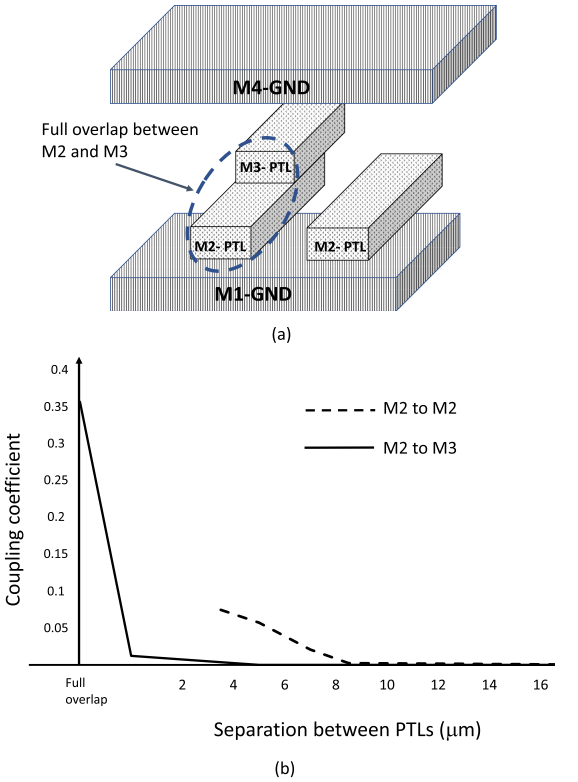

Fig. 2. Coupling coefficient between the same layer and adjacent layers. (a) Stripline structure with full overlap between M2 and M3 PTL. (b) Dependence of coupling noise on physical separation.

M3 layers behave as parallel striplines. The width and thickness of the PTLs in the M2 and M3 layers are, respectively, 5.2 μm and 200 nm (see Section II). The length of the PTLs is 100 μm. The ground layers are placed in M1, M4, and M7. The multiple ground planes are connected with stitching vias—vias connecting the ground layers—[18], [19], [20]. The dependence of the coupling coefficient K on the separation between PTLs in the same layer and adjacent layers is illustrated in Fig. 2(b). A large separation between the lines lowers the coupling coefficient. Two PTL lines in the M2 layer exhibit larger inductive coupling than two PTL lines in an adjacent layer. The distance between the M2 and M3 layers to the ground layers and the distribution of the return path in the ground layers affect the coupling coefficient by approximately an order of magnitude (see Fig. 2). The return path is partially distributed among three different ground layers. Most of the return current flows in the ground plane closest to the stripline. Note that the ground layers are connected with stitching vias. The ground layers will therefore be shared among the current return paths of the different striplines. PTLs in adjacent layers with a vertical overlap between striplines [as shown in Fig. 2(a)] exhibit higher coupling depending upon the area of the overlap. When a stripline in the M3 layer is entirely above a stripline in the M2 layer [see Fig. 2(a)], full overlap is realized, producing significant coupling between these lines [see Fig. 2(b)].

The width of the ground layers in M1 and M4 can also affect the inductive coupling between PTLs in the M2 and

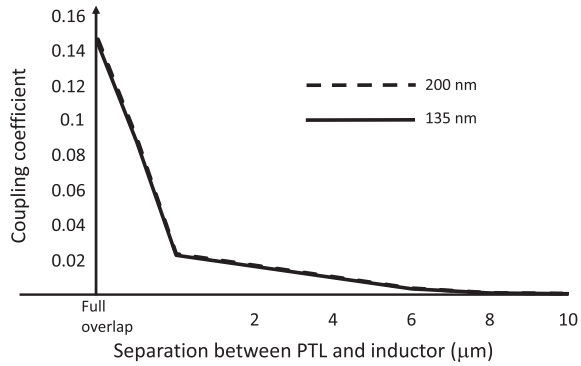

Fig. 3. Coupling coefficient between M3 PTL and M5 inductors.

M3 layers. Note that wide ground layers slightly improve the inductive coupling coefficient between lines. The wide ground layer covers the entire layout. The dimensions of the ground are approximately 0.5×0.5 mm. The coupling coefficient decreases by -0.7% in the full overlap case [see Fig. 2(a)]. Wide ground layers are therefore more desirable from a noise perspective than multiple small ground layers in a multilayer process.

B. PTL Coupling to Bias Lines and Inductors

Different line structures produce different inductive coupling characteristics. Inductive coupling from a PTL to the bias lines and inductors is discussed here. In this section, the effects of the thickness of the inductors on the inductive noise between PTLs and the effects of the vertical distance between lines on the inductive coupling are described.

The standard thickness of a PTL within the M3 layer and inductor in the M5 layers are, respectively, 200 and 135 nm (for the MIT LL SFQ5ee process [19]). The dependence of coupling noise between the PTL and the inductors due to the physical separation between lines is shown in Fig. 3. The width of the PTL and inductor is, respectively, 1.8 and 2 μm. The bias line and inductor are in parallel over a length of 20 μm. The coupling coefficient of the thicker inductor is slightly larger than a standard inductor. The effects of the line thickness on the inductance are analytically modeled in [22]. The thicker lines produce a lower self-inductance. The mutual inductance between the L_1 and L_2 inductors is $M = K\sqrt{L_1 L_2}$, where K is the coupling coefficient. Increasing the thickness of the Nb striplines therefore slightly lowers the mutual coupling between layers.

Coupling from a PTL to those layers separated by the M1 and M4 ground planes is shown in Fig. 4. The PTL, inductor, and bias lines are placed, respectively, in the M3, M5, and M0 layers. The lines are placed in parallel to evaluate the worst case inductive coupling. The coupling coefficient of the PTL to the inductor is higher than to a bias line in the full overlap case [see Fig. 4(a)] and nonoverlap cases, as shown in Fig. 4(b). The larger thickness of the dielectric between the layers produces less coupling between the PTL and M5 than between the PTL and M0.

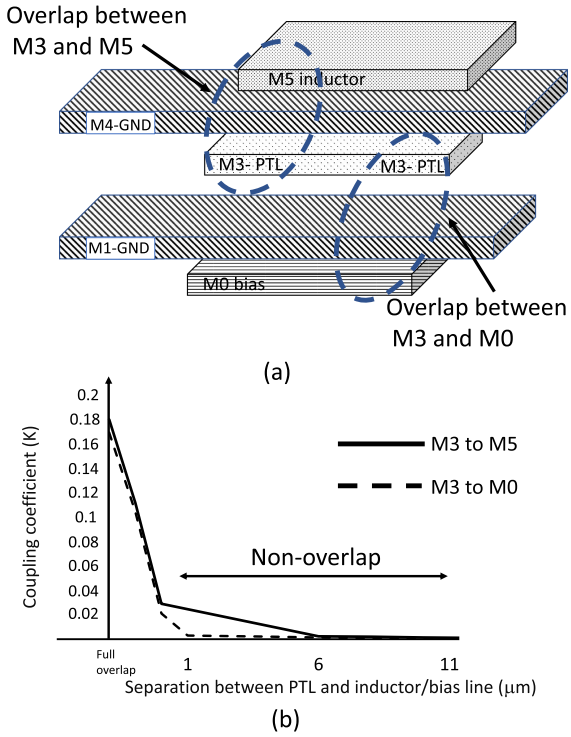

Fig. 4. PTL coupling to M0 bias line and M5 inductor. (a) Line structure with overlap between lines. (b) Dependence of coupling noise on physical separation.

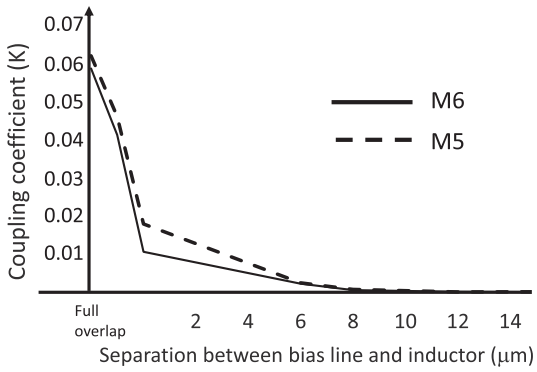

Fig. 5. Coupling coefficient between bias line and inductor in M5 and M6.

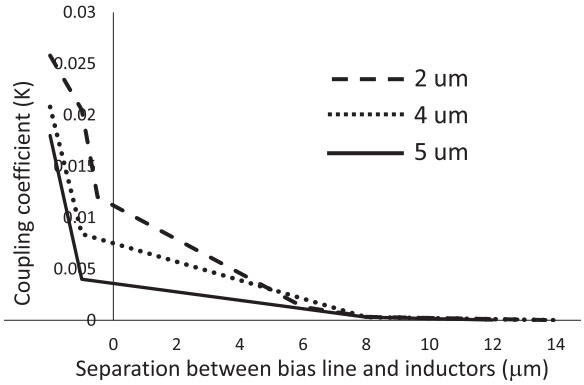

Fig. 6. Coupling coefficient between the M0 bias line and M6 inductor for different line widths.

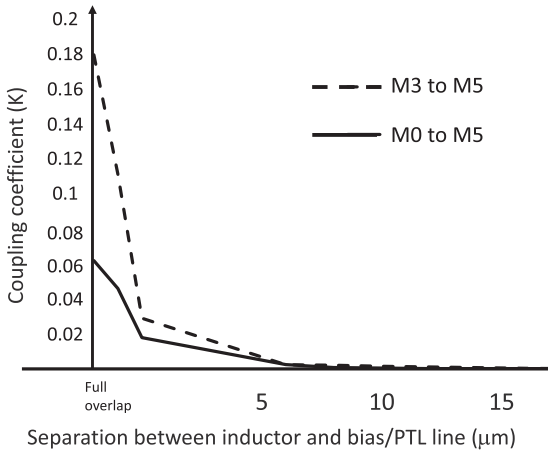

Fig. 7. Coupling coefficient of PTL and bias to an inductor.

C. Coupling Between Bias Lines and Inductors

The bias lines carry high current which affects the operation of the PTLs and logic gates. Narrower bias lines enhance circuit densities, preventing any overlap between the bias lines and inductors while producing less inductive coupling. Characterization of the local coupling noise among the bias lines, PTL lines, and inductors can be used to provide design guidelines for enhancing the robustness of automated routing tools in VLSI complexity SFQ circuits. The parameters affecting the inductive coupling characteristics are the vertical distance to the inductors, width of the inductors, and number of ground layers. The dependence of the bias coupling characteristics on these parameters is described in this section.

The dependence of the coupling coefficient between the bias lines and inductors in M5 and M6 (through two ground planes) on the physical separation is shown in Fig. 5. The bias line and the inductor are in parallel over a length of 80 μm. The width of the bias line is 1.8 μm. The inductors directly above the bias lines exhibit significant inductive coupling noise. Note that coupling between the bias line and the inductor in M6 is slightly smaller than coupling between the bias line and the inductor in M5 due to the greater vertical distance. The coupling coefficient is slightly reduced for greater distances between layers with the same number of ground planes between layers.

Inductive coupling between the bias lines and the inductor in the M6 layer for different widths is shown in Fig. 6. The bias line and the inductor are in parallel over a length of 40 μm. The width of the bias line is 1.8 μm. The coupling coefficient of the bias line to a 2-μm wide inductor is almost two times greater than to a 5-μm wide inductor. The wider inductors exhibit a smaller coupling coefficient as compared to narrower inductors. The narrow lines however require less area, reducing the layout density of complex SFQ circuits. A tradeoff therefore exists between inductive coupling and layout density.

Inductive coupling in the M5 layer to the bias and PTL lines is compared in Fig. 7. Long straight inductors are assumed—uncommon in practical circuits—to evaluate the worst case condition. The number of ground layers between the lines affects

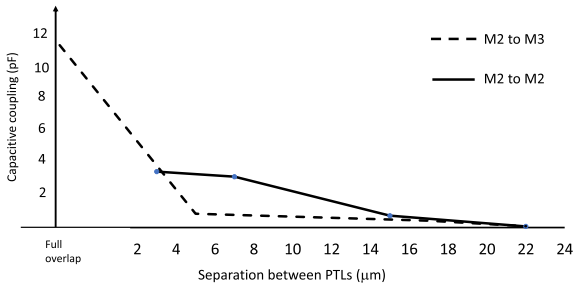

Fig. 8. Capacitive coupling coefficient between two PTLs in the same and adjacent layers.

the coupling coefficient of each structure. Coupling is less for a longer vertical distance between lines (due to a thicker dielectric). Coupling between a PTL line and an inductor is three times larger than coupling between a bias line and an inductor. Coupling between an inductor and a PTL is significant in the full overlap case. Coupling between a bias line and the M3 and M5 layers is also evaluated to determine the effects of the number of ground planes on the noise characteristics. Each ground plane between two coupled lines reduces the inductive coupling by approximately three to four times, as depicted in Fig. 7. A physical separation greater than 10 μm produces negligible inductive coupling between the M5 inductor and M0 bias/M3 PTL line.

IV. Capacitive Coupling Between Routing Layers

PTL striplines are a primary structure for signal routing in VLSI complexity SFQ circuits [5], [11]. Capacitive coupling between PTL striplines in the same and different layers degrades the delay and impedance characteristics of interconnects while also affecting the resonance behavior. Capacitive coupling between routing layers is described in this section. Simulations are performed on Sonnet, and a π model is applied. The parameters affecting the coupling capacitance, between PTL lines in the same and adjacent layers, are the physical separation between PTLs, width of the ground layers, and number of connecting vias between the ground layers. The dependence of the PTL coupling characteristics on these parameters is described in this section.

The dependence of the coupling coefficient K on the physical separation between PTLs in the same and different layers is shown in Fig. 8. The two PTL lines are parallel over a length of 80 μm. The width of the striplines is 5.2 μm. The ground layers are placed in M1, M4, and M7, as shown in Fig. 1. PTLs in adjacent layers with a full overlap exhibit significant coupling. Two PTL lines in the same M2 layer, however, exhibit larger capacitive coupling than two PTL lines in adjacent layers. The capacitive coupling between two PTL lines in the M2 layer with a separation of 3 μm is 3.54 pF, degrading the margins and operability of SFQ circuits. The large separation between the lines exponentially lowers the coupling coefficient, as shown in Fig. 8.

Capacitive coupling is also dependent on the width of the ground layers. Fabricating multiple small ground planes is extremely difficult while increasing the layout area. Capacitive coupling between two PTL lines in adjacent layers in wide and multiple small ground layers is, respectively, 18.7 and 11.5 pF. Wide ground layers significantly increase the capacitive coupling noise by approximately 40% in the full overlap case. The wide ground layers lower the inductive coupling by 7%. A tradeoff therefore exists between inductive and capacitive coupling. Wide ground layers in a multilayer process are preferable rather than multiple portions of the ground layer. A tradeoff therefore also exists between the capacitive coupling and the complexity of the fabrication process.

The dependence of the number of stitching vias—vias connecting the ground layers—on the capacitive coupling characteristics in adjacent layers is described here. For PTLs with two vias at the start and end of the lines, the capacitive coupling and capacitance-to-ground are, respectively, 0.0343 and 0.053 pF in the full PTL overlap case. The coupling capacitance and capacitance-to-ground for PTLs with five vias with a 20-μm physical space between the vias are, respectively, 0.0379 and 0.0528 pF. Increasing the number of these vias slightly increases the capacitive coupling and decreases the capacitance-to-ground. A tradeoff therefore exists between the coupling capacitance and the capacitance to ground.

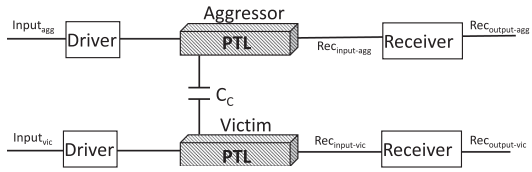

Fig. 9. Coupled aggressor and victim PTL lines.

V. Guidelines for Capacitive Coupling Noise

The interconnect characteristics [5], [11] and resonance behavior of PTL striplines [17] pose a significant challenge in the design of VLSI complexity SFQ circuits. Different circuit structures exhibit a different sensitivity to capacitive coupling noise, producing different types of errors. Capacitive coupling between PTLs in the same and adjacent layers significantly affects the PTL characteristics and operation. The effects of the coupling capacitance on the operation of the proposed receiver in [5] and the resonance behavior of PTL striplines are described, respectively, in Section V-A and V-B.

A. Effects of Capacitive Coupling Noise Between PTLs

An SFQ pulse propagates within an aggressor PTL and electromagnetically interacts with a victim PTL. The PTL lines are connected to a matched driver and receiver. A PTL driver and receiver configuration with one JJ is described in [5]. Coupled PTLs with a driver and receiver are shown in Fig. 9. Capacitive coupling occurs between lines, as shown in Fig. 8. The capacitive coupling affects the impedance characteristics of the victim PTL, producing an impedance mismatch within the transmission line, driver, and receiver. Due to this mismatch, SFQ pulses are partially reflected, disturbing the behavior of the receiver. The behavior of the PTL receiver with capacitive coupling is

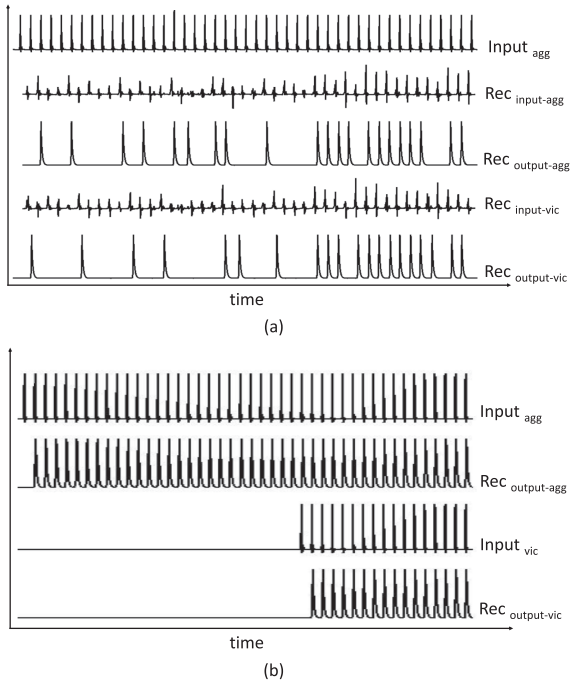

Fig. 10. Operation of PTL receivers with capacitive coupling. (a) Large coupling capacitance $C_{coupling} = 3.5$ pF. (b) Small coupling capacitance $C_{coupling} = 0.07$ pF.

illustrated in Fig. 10. Close separation between lines in the M2 layer produces a large coupling capacitance; for example, $C_{coupling} = 3.5$ pF, as shown in Fig. 8. The large capacitive coupling changes the impedance characteristics of the line and disturbs the operation of the receiver [see Fig. 10(a)]. An appropriate range of coupling capacitance is determined for the PTL receiver to operate correctly. For $C_C < 0.1$ pF, the effects of the coupling capacitance are negligible, and the receiver operates correctly [see Fig. 10(b)]. A physical space between lines greater than 10 μm produces negligible coupling capacitance between PTLs in the same layers and adjacent layers. In this case, the PTL receiver operates correctly with a few per cent degradation in margins. In a practical routing topology [19], the physical space is 20 μm, removing the effects of capacitive coupling between PTLs.

B. Resonance Characteristics of Two Coupled PTL Lines

Capacitive coupling noise also affects the resonance characteristics of PTL lines [24]. An interconnect is represented by a lossless distributed LC transmission line, where the impedance depends upon the interconnect length [25]. L and C are, respectively, the inductance and capacitance per unit length. For a lossless line, the phase velocity and resonance frequency [17] are, respectively,

$$v = \frac{1}{\sqrt{LC}} \tag{1}$$

and

$$f_r = \frac{nv}{2\,l} \tag{2}$$

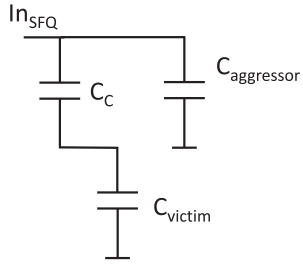

Fig. 11. Capacitance model of coupled striplines.

where l is the physical length of the PTL, and n is an integer multiplier that determines the harmonic behavior of the resonance frequency [17].

A capacitance model of a coupled stripline is shown in Fig. 11. The total capacitance of the aggressor line is

$$C_{\text{total}} = C_{\text{aggressor}} + \left(\frac{1}{\frac{1}{C_C} + \frac{1}{C_{\text{victim}}}} \right). \tag{3}$$

The coupled capacitance increases the capacitance per unit length C of the aggressor PTL. At a specific operating frequency, the resonance lengths are decreased. For example, in the worst case where $C_{\text{aggressor}} = C_C = C_{\text{victim}} = C$, the total capacitance increases by 50%, $C_{\text{total}} = 1.5\,C$. The phase velocity and resonance length decrease by 20%. Approximately 20% margins for the resonance length of all PTLs ensures that the length of each PTL stripline remains outside the resonance regions [17]. An estimate of the capacitive coupling noise can be used as a guideline for automated routing tools and for the layout of individual standard cells and interconnects. These coupling noise guidelines enable the routing of robust superconductive interconnects.

VI. Conclusion

Coupling noise in prospective large scale SFQ circuits is a significant issue in the automated routing of high speed integrated SFQ circuits. Superconductive striplines and microstriplines are primary structures in SFQ circuits. Inductive and capacitive coupling among the inductances, striplines, and bias microstriplines within superconductive circuits degrades the circuit margins of these systems. Accurate characterization of inductive and capacitive coupling is necessary to determine the minimum physical space between striplines. Inductive coupling between different layers in the MIT LL SFQ5ee process is presented here for different line structures. The mutual inductance of the striplines matches experimental data within 3%, less than a standard deviation from the experimental data presented in [23]. Capacitive coupling between routing layers in adjacent layers is also discussed. The capacitive coupling exponentially depends upon the separation between PTL lines. Design guidelines and tradeoffs are presented to reduce the effects of coupling noise on the resonance characteristics of a PTL receiver. These guidelines support automated routing tools, enabling higher performance and more robust SFQ systems.

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