Stripline Topology for Flux Mitigation

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***Abstract*—The increasing complexity of modern single flux quantum (SFQ) circuits has increased the importance of flux trapping and trapped magnetic fields within SFQ systems. This trapped flux reduces margins while damaging the operability of superconductive circuits. In this paper, an area efficient stripline topology is introduced to prevent flux from being trapped within striplines. The topology is composed of coupled narrow lines rather than wide striplines. The proposed topology uses a fingered narrow line configuration. The fingered narrow line topology enhances the scalability of SFQ systems while not requiring additional area. The proposed topology decreases the length of the striplines by exploiting the mutual inductance between narrow parallel lines. The topology requires less area while preventing flux from being trapped within wide superconductive striplines. Due to the configuration of the proposed stripline, residual current is eliminated in VLSI complexity SFQ circuits. The fingered narrow line topology also reduces coupling capacitance between striplines. The proposed topology is compatible with automated routing of large scale SFQ integrated circuits.**

***Index Terms*—Superconductive integrated circuits, single flux quantum, electronic design automation, automated layout and routing tool, flux trapping.**

I. Introduction

RECENT developments in electronic design automation have enabled the increasing integration of single flux quantum (SFQ) circuits [1], [2], [3], [4]. The sensitivity of SFQ circuits to trapped magnetic fields [5], [6], [7], is a significant issue in large scale superconductive integrated circuits. Trapped fluxons within the ground planes, Josephson junctions (JJs), superconductive loops, and striplines [6], [8] degrade the operability of superconductive circuits while decreasing margins [2], [9]. The trapped fluxons also couple into nearby interconnects, bias lines, and JJs, affecting the behavior of the lines and JJs. Flux mitigation within VLSI complexity SFQ circuits and, in particular the striplines, is therefore necessary to support the development of advanced superconductive systems.

The purpose of this paper is to introduce a topology to mitigate the effects of flux trapping within wide striplines. The principles of flux trapping are briefly reviewed in Section II. A configuration for wide superconductive striplines to eliminate flux trapping is described in section III. The proposed stripline is evaluated in Section IV. The paper is concluded in Section V.

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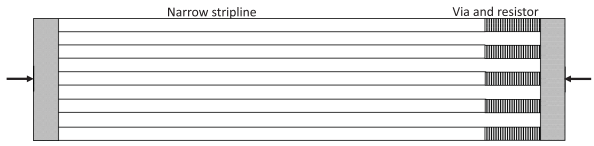

Fig. 1. Configuration of stripline composed of multiple narrow parallel lines [2].

II. Background

Flux trapping within superconductive thin films was discovered in 1982 [10]. To manage the effects of flux trapping within VLSI superconductive systems, moats within superconductive ground planes are often used [2]. These moats prevent the accumulation of undesired magnetic flux in unwanted areas, preventing degradation in circuit operability. Another primary type of flux trapping in superconductive systems is trapped fluxons within wide striplines. Placing moats within striplines is not effective due to the degradation of the stripline characteristics. The trapped fluxons within striplines near the logic cells degrade circuit operation while lowering the critical current and decreasing the bias margins of the Josephson junctions. The trapped fluxons also couple into nearby inductors, interconnects, and bias lines.

A stripline topology has recently been proposed in [2] to manage flux trapping in wide striplines – large inductors and interconnects. The stripline topology, based on narrow parallel lines, is shown in Fig. 1. The narrow parallel line topology is composed of narrow lines and small resistors (vias). Multiple narrow parallel lines are connected with perpendicular lines at the ends of the narrow lines, maintaining the same width as a wide stripline. A thinner stripline width decreases the likelihood of flux being trapped within the stripline. The small resistor within each narrow line breaks the superconductive loop within the stripline, reducing the likelihood of flux being trapped within striplines and metal layers.

The narrow parallel line topology exhibits the same output impedance characteristics as a wide line [2]; no changes are therefore required for the driver and receiver within a passive transmission line (PTL) segment. In addition, the narrow parallel line topology exhibits the same resonance characteristics as a single wide stripline. Design guidelines for wide striplines are also applicable to the narrow parallel line topology [11].

Due to the number of vias, a tradeoff exists between the scalability of SFQ circuits and the effectiveness of the parallel

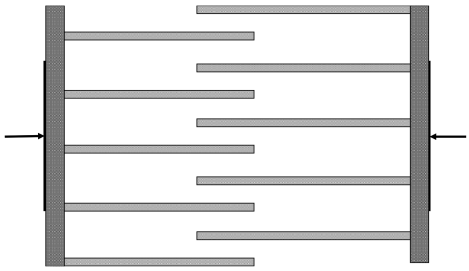

Fig. 2. Configuration of fingered stripline composed of multiple narrow coupled lines.

line topology. Using fewer vias and resistors generates holes within the stripline and a circulating current through those parallel lines without resistors, increasing the probability of flux being trapped within the narrow parallel lines.

III. Model of Wide Striplines

To enhance the scalability of SFQ systems, an approach is proposed to eliminate flux trapping within striplines while not increasing the number of vias. The proposed stripline topology is shown in Fig. 2. The fingered line topology is composed of narrow broken lines – no DC connection between the lines – which are capacitively coupled. Capacitive coupling between narrow lines passes SFQ pulses along the striplines. The proposed configuration eliminates residual current within SFQ circuits. The preferable width of the narrow lines and the space between the narrow fingered lines are technology dependent. The proposed topology significantly reduces flux trapping in striplines and metal layers. The topology exhibits a higher effective inductance as compared to a wide inductor by exploiting the mutual inductance between the coupled lines. The narrow fingered lines topology breaks the superconductive loops within the striplines while requiring less area than the narrow parallel lines topology.

A. Different Fingered Line Topologies

Different configurations of the fingered line topology are depicted in Fig. 3. These configurations are one-to-one fingered line, 3-to-2 multiple fingered line, and 3-to-3 multiple fingered line. The striplines are placed within the M2 layer (in the MIT Lincoln Laboratory SFQ5ee fabrication process). Ground planes are placed in the M1 and M4 layers. The length of all of the stripline topologies is 300 μm. The width of the lines is 5.2 μm with 0.5 μm spacing between the narrow fingered lines. The one-to-one fingered line topology is composed of two capacitively coupled broken lines. These broken lines eliminate residual currents in the superconductive loops. The coupling length, as shown in Fig. 3(a), determines the coupled capacitance between narrow lines, shifting the resonance frequency [12]. Based on the target resonance frequency, the length can be adjusted. The 3-to-2 multiple fingered line topology is composed of five broken lines; three short lines at the input and two lines at the output. The 3-to-2 fingered line topology produces multiple resonance frequencies in the S11 parameter due to the different

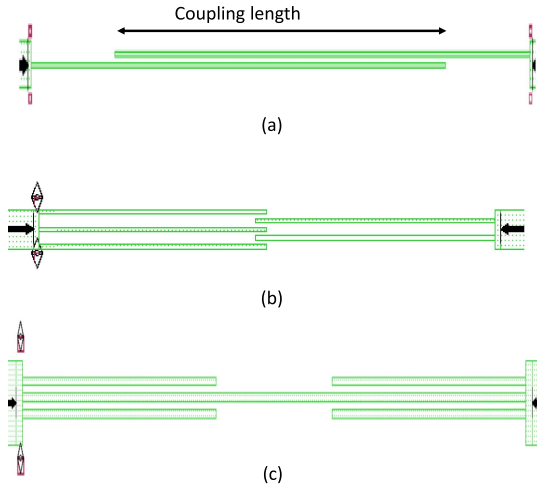

Fig. 3. Stripline with narrow fingered line topology, (a) one-to-one fingered line, (b) 3-to-2 multiple fingered lines, and (c) 3-to-3 multiple fingered lines.

coupling lengths between lines, requiring different guidelines as compared to a wide line. This topology also exhibits a small S11, reflecting most of the pulse at the input port. The 3-to-3 multiple fingered line topology is composed of multiple broken lines and one straight line. The straight line is bounded by narrow shorter lines, reducing the probability of trapping flux within the straight line. The 3-to-3 fingered line topology exhibits the same characteristics and frequency behavior as a wide stripline. This topology exhibits a smaller S11 than a wide line. S11 of the 3-to-3 fingered line is lowered by placing a load resistor at the output port of the stripline. The S11 and S21 parameters of a wide stripline, 3-to-3 fingered line topology, and one-to-one fingered line topology are illustrated in Figs. 4(a), (b), and (c). The one-to-one fingered line topology and 3-to-3 multiple fingered line topology exhibit a single resonance frequency as a wide line. A different coupling length between lines produces a different resonance frequency which is adjusted based on the operating frequency of the system. Routing guidelines for the proposed topologies are based on the resonance frequency of the striplines [12], [13]. These topologies are an effective candidate to replace wide striplines.

IV. Characterization of Narrow Striplines

PTL striplines are a primary structure for signal routing in VLSI complexity SFQ circuits [14], [15]. The proposed fingered narrow line topology is compared to the narrow parallel stripline and wide stripline topologies. The impedance characteristics of the proposed topology are described in Section IV-A. Inductive and capacitive coupling of the narrow parallel stripline and fingered stripline topologies are compared with wide striplines in Section IV-B.

A. Impedance Characteristics

The narrow parallel PTL line topology is characterized in Sonnet. The surface inductance of the striplines is based on [6]. An RLGC model is used to compare the characteristics of a

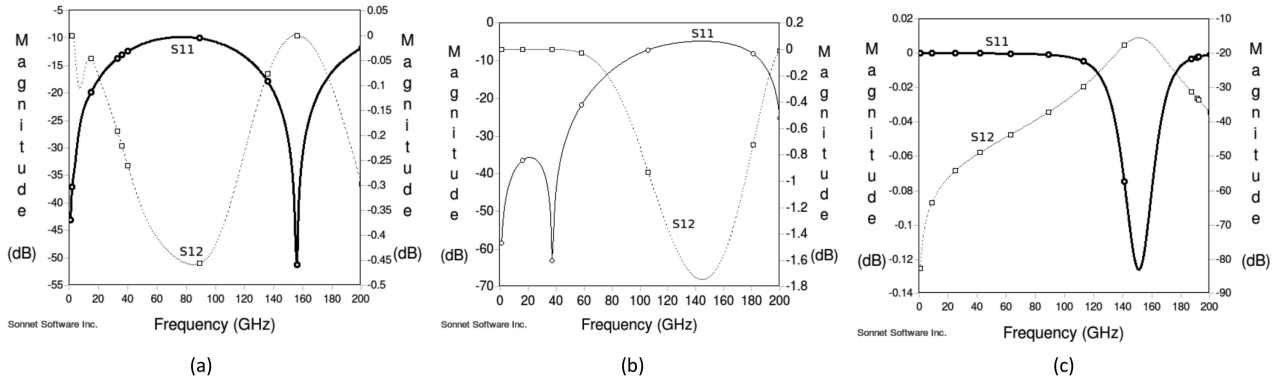

Fig. 4. S11 and S12 parameter of a stripline, (a) wide stripline, (b) 3-to-3 multiple fingered line topology, and (c) one-to-one fingered line topology.

TABLE I
COMPARISON OF IMPEDANCE CHARACTERISTICS OF STRIPLINES

	Width (μm)	**Impedance (Ω)**
Wide stripline	5.2	7.4
Narrow stripline	0.5	60
Two fingered striplines	5.2	7.27
Four fingered striplines	5.2	7.26
Six fingered striplines	5.5	6.83

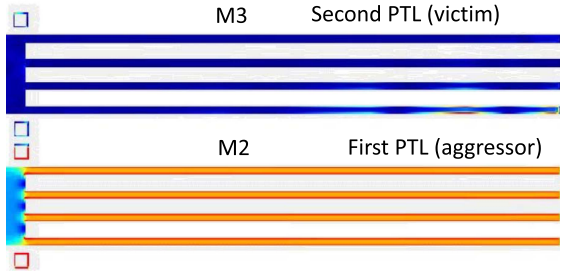

Fig. 5. Current distribution within coupled stripline with the four narrow line topology operating at around 20 GHz.

wide stripline with the fingered narrow parallel stripline. The striplines are placed within the M2 layer (in the MIT Lincoln Laboratory SFQ5ee fabrication process [16]). The ground planes are placed within the M1 and M4 layers. The width of the striplines is 5.2 μm with 80 μm length. The configuration of the striplines is composed of a single 5.2 μm wide line, one-to-one fingered line topology with two 0.5 μm wide fingered lines with 0.5 μm spacing, two-to-two fingered line topology with four 0.5 μm wide fingered lines with 0.5 μm spacing, and three-to-three fingered line topology with six 0.5 μm wide fingered lines with 0.5 μm spacing. A comparison of the impedance characteristics of these configurations is listed in Table I. The impedance characteristics of these topologies are similar to the output impedance of a wide line; a standard driver and receiver are therefore applicable for the proposed topology. Unlike the proposed topology, a single narrow stripline within a PTL segment produces a high impedance which requires a different receiver and driver circuit.

B. Inductive and Capacitive Coupling Between Striplines

Inductive and capacitive coupling between PTL striplines in the same and different layers degrades the impedance characteristics of interconnects while also affecting the resonance behavior. Inductive and capacitive coupling between adjacent layers is evaluated in Sonnet based on a π model. Different line configurations exhibit different inductive and capacitive coupling noise characteristics. In this section, the effects of inductive and capacitive coupling noise within the fingered line topology are characterized while preventing flux from being trapped within the striplines.

Inductive and capacitive coupling between adjacent layers is characterized in Sonnet based on a π model at 20 GHz, illustrating the effects of inductive coupling between narrow lines. Striplines with the four narrow parallel line topology are placed in the adjacent M2 and M3 routing layers [17]. The width of the lines is 5.2 μm. The space between two striplines is 3.5 μm. The current distribution within the aggressor and victim striplines with the four narrow parallel line topology operating at around 20 GHz is illustrated in Fig. 5. Most of the inductive coupling is applied to the last narrow line of the victim stripline near the aggressor stripline. The other narrow lines within the victim stripline compensate for the effects of inductive coupling to the victim stripline. The inductive coupling between two wide striplines is 7.7×10^{-4}. The inductive coupling between two striplines with four narrow parallel lines is 4.1×10^{-4}. The narrow parallel line configuration exhibits approximately two times less inductive coupling with the nearby striplines as compared to the wide interconnect stripline.

Inductive and capacitance coupling between different stripline configurations in the adjacent M2 and M3 layers in the SFQ5ee process is listed in Table II. The lines are placed in parallel in the full overlap case – the stripline in the M3 layer is entirely above the stripline in the M2 layer – to determine the worst case inductive and capacitive coupling. Four different configurations are considered for these striplines. These configurations are the four narrow parallel line, one-to-one fingered line, 3-to-3 fingered line, and wide stripline, as shown in

TABLE II
COMPARISON OF INDUCTIVE AND CAPACITIVE COUPLING BETWEEN DIFFERENT STRIPLINE CONFIGURATIONS

	Capacitance-to-ground (pF)	Capacitive coupling (pF)	Inductive coupling coefficient
Wide stripline	0.047	0.032	∼0.3
One-to-one fingered line topology	0.015	0.0125	∼0.6
3-to-3 fingered line topology	0.017	0.0106	∼0.2
Four narrow parallel line topology	0.03	0.015	0.185

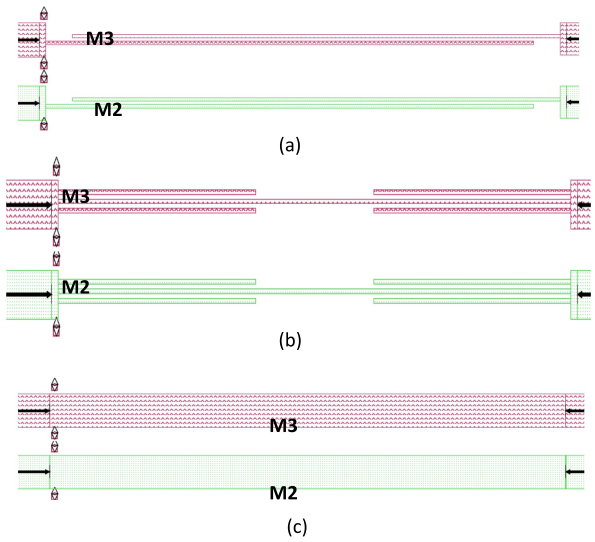

Fig. 6. Stripline configurations in the adjacent layers, (a) one-to-one fingered line topology, (b) 3-to-3 fingered line topology, and (c) wide striplines.

Figs. 5 and 6. The width of the lines at the start and end of the line is 5.2 μm. The space between two narrow lines is 0.5 μm. In the worst case, the stripline with the four narrow parallel line topology exhibits approximately two times less inductive and capacitive coupling as compared to the wide stripline. Due to less area of the proposed topologies as compared to a wide stripline, the capacitance-to-ground of the one-to-one fingered line topology and 3-to-3 fingered line topology is three times less than the capacitance of a wide stripline. The coupling capacitance of the one-to-one fingered line topology and 3-to-3 fingered line topology is, respectively, two and three times less than the coupling capacitance of a wide stripline. The inductive coupling coefficient of the 3-to-3 fingered line topology is approximately half of the inductive coupling coefficient of the wide stripline. The proposed fingered topology therefore prevents flux from being trapped within striplines, supporting robust routing of superconductive striplines while requiring less area and producing less coupling noise.

V. CONCLUSION

Flux trapping within superconductive striplines is a significant issue in VLSI complexity SFQ systems. The trapped fluxons within striplines couple to nearby JJs and interconnects, reducing margins while damaging the operability of SFQ circuits. To prevent flux trapping in striplines, a fingered line topology is proposed here, enhancing the scalability of SFQ systems. The topology simultaneously eliminates residual currents in JJs and the storage loop within SFQ circuits. The proposed fingered line topology significantly reduces the physical area of the striplines. Inductive and capacitive coupling noise between the striplines is two to three times smaller than wide striplines. The capacitance-to-ground of the proposed topologies is three times less than the capacitance of a wide stripline. The impedance characteristics of the proposed fingered line topology are similar to wide striplines. Routing guidelines for the proposed topology are compatible with automated routing tools.

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