AC Biased SFQ Clock Splitters for Current Mitigation

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***Abstract*—High current requirements in single flux quantum (SFQ) circuits pose scalability challenges, contributing to issues such as high thermal loads, static power dissipation, and increased sensitivity to flux trapping under nonideal shielding or cool down conditions. AC biasing, successfully used in other superconductive logic families, has been integrated into rapid single flux quantum (RSFQ) circuits and typically includes ac-to-dc converters, introducing area and complexity overhead. This work proposes an alternative method for applying ac biasing to existing RSFQ circuits using inductively coupled bias junctions, eliminating the need for ac-to-dc converters. This approach also combines resistive dc biasing with inductive ac biasing, reducing static power dissipation. The proposed approach targets clock splitters, which are significant contributors to on-chip current demand, achieving an average 94% reduction in splitter current and a 62% reduction in overall system current with a Josephson junction overhead of 6.5% . The technique is compatible with conventional RSFQ system architectures and logic families while significantly enhancing energy efficiency and scalability.**

***Index Terms*—AC biasing, bias current distribution, bias current reduction, clock splitters, ERSFQ, inductive coupling, RSFQ, single flux quantum, timing analysis for SFQ circuits.**

I. Introduction

SINGLE flux quantum (SFQ) technology offers fast switching speeds and low power dissipation, making the technology a strong candidate for stationary, high performance computing and signal processing applications [1]. SFQ circuits exhibit distinct characteristics, including operation at cryogenic temperatures, clocked logic gates, splitters to support multiple fanout, and strict limitations on the maximum current per integrated circuit [1], [2], [3]. Scalability remains a significant challenge, as the largest SFQ circuits currently consist of a few million Josephson junctions (JJs) [4], while advanced CMOS circuits integrate many billions of transistors [5].

In conventional RSFQ circuits, resistive dc current supplies the necessary bias current, dissipating static power. One of the primary scalability constraints in SFQ circuits is high current demand, which can reach several amperes per integrated circuit [6], [7], [8], [9], [10], [11], [12], [13]. Excessive current introduces multiple design constraints, including greater heat load, which compromises superconductive and cryogenic properties, reliability concerns, such as increasing flux trapping effect, and more stringent cooling requirements for cryogenic systems [8], [13].

As SFQ circuits scale, the number of splitters increases, particularly within the clock distribution network, leading to greater current consumption. This process of scaling exacerbates challenges related to thermal management and bias margins. To mitigate high current consumption, several techniques have been explored. Current recycling, where the ground planes are isolated to allow current to be reused between planes, has been proposed as a potential solution [14], [15], [16]. This method, however, introduces significant design and fabrication complexities. Other approaches have led to the development of alternative superconductive logic families, such as reciprocal quantum logic (RQL) [4], [17] and adiabatic quantum flux parametron (AQFP) logic [18], [19], [20]. The demonstration of RQL in shift registers and logic gates requires novel gate architectures tailored to ac biased and phase-based signaling methods [4]. While AQFP consumes significantly less power, the systems operate at much lower frequencies. Both approaches, RQL and AQFP, employ ac biasing to supply bias current. RQL also uses the ac bias to supply a synchronizing clock signal. Unlike dc biasing, which relies on resistive power distribution which dissipates significant static power, ac biasing eliminates static dissipation by using superconductive transmission lines and inductive coupling, enhancing overall system-level energy efficiency.

In an SFQ ac biased system, precise timing of the clock distribution network is critical due to the ultrafast switching characteristics and pipelined operation of the logic gates. As RSFQ circuits continue to evolve, effort has been directed toward integrating ac biasing into existing RSFQ circuits. Recent work utilizes ac-to-dc converters to supply dc bias current from sinusoidal ac waveforms [21], [22]. These approaches require multiple converters to satisfy bias current demands, degrading scalability.

A method of directly applying an ac bias to RSFQ circuits using inductive coupled junctions is proposed here. This approach eliminates the need for ac-to-dc converters, reduces static power dissipation, and lowers JJ overhead. The method is selectively applied to the clock splitters–a primary source of on-chip current demand–without modifying the logic gates or altering the

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clocking methodologies. The resulting hybrid biasing scheme maintains compatibility with standard RSFQ architectures while dissipating significantly less power and improving scalability. The tradeoff with the number of ac sources as frequency and fanouts increase is explored. The timing and current consumption characteristics in representative RSFQ circuits demonstrate the feasibility and effectiveness of the proposed approach.

The rest of this article is organized as follows. AC biasing in relevant superconductive logic families is described in Section II. AC biasing of RSFQ cells is discussed in Section III. The application of ac biasing to clock splitters is presented in Section IV. Architectural issues and related design tradeoffs are discussed in Section V. Finally, some conclusion and directions for future work are provided in Section VI.

II. AC Biasing of Superconductive Circuits

AC biasing is achieved with inductive coupling, where the bias current is inductively coupled to an ac transmission line. The bias current extracted from the ac lines depends upon the size of the inductor, coupling factor, and amplitude of the sinusoidal wave. AC biasing in RQL, AQFP, and RSFQ is described, respectively, in Sections II-A, II-B, and II-C.

A. Reciprocal Quantum Logic

RQL is a digital superconductive logic family encoding digital signals using a pair of SFQ pulses with opposite polarity [4]. An ac source is utilized in RQL to supply both current and clock and utilizes two ac power lines to generate reciprocal SFQ pulses, with power alternating between the lines in successive half cycles. These signals simultaneously provide clock synchronization, power delivery, and SFQ pulse resetting, significantly simplifying the distribution of power and eliminating static power dissipation. Crucially, RQL utilizes a four phase clocking scheme derived from these two ac bias lines, enabling sequential logic operations, controlled pulse propagation, and resetting during each clock cycle. While this circuit topology enhances power efficiency and reduces jitter, the structure also imposes stringent synchronization constraints while heightening the sensitivity to timing and fabrication variations.

B. Adiabatic Quantum Flux Parametron

In AQFP circuits, an alternating current simultaneously provides both clock and power. This dual use of ac waveforms is also seen in RQL, where the ac power lines deliver energy and timing through reciprocal operation. In contrast, ac-to-dc converters used in SFQ circuits apply an ac signal to generate a dc bias current without embedding any timing information. AQFP is characterized by extremely low energy dissipation [18], achieved primarily through ac biasing of adiabatic circuits. AQFP circuits utilize a sinusoidal ac excitation current applied through inductively coupled bias lines, allowing the circuit elements to adiabatically and gradually switch states, greatly lowering the dynamic energy [23]. Unlike conventional superconductive circuits, such as SFQ, the operation of AQFP gates is based on parametric excitation. The ac bias current gradually modulates the potential energy profile, transitioning a quantum flux with near zero energy dissipation [18]. The ac bias is delivered in multiple phases (typically two or four phases), ensuring sequential and controlled switching throughout the logic network. Despite the exceptional energy efficiency, AQFP relies on precise multiphase ac biasing, which introduces significant complexity into the clock distribution network to maintain error free operation.

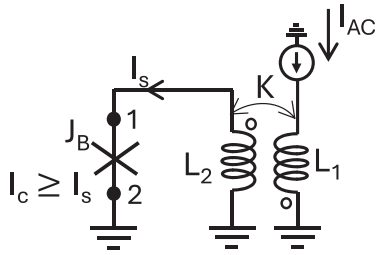

Fig. 1. AC bias with bias junction J_B.

C. Rapid Single Flux Quantum

RSFQ circuits [1] traditionally rely on resistive dc biasing, dissipating high static power. An alternative approach uses ac biasing with superconductive ac-to-dc converters and filters [21], [22]. Sinusoidal ac signals are converted to stable dc currents by JJ-based rectifiers, while filters lower any fluctuations, providing a low jitter dc bias [22]. This approach significantly reduces the static power dissipation, enhancing power efficiency and scalability. The use of ac-to-dc converters and filters, however, introduces additional design complexity.

III. AC Bias of RSFQ Circuits Using a Bias Junction

The use of a bias junction J_B to deliver an ac bias current to RSFQ circuits, along with relevant design considerations and tradeoffs, are described in this section. The operating principle of the proposed techniques is discussed in Section III-A. Some design issues are explored in Section III-B.

A. Operating Principle of AC Biased RSFQ Circuits With a Bias Junction

The primary function of the bias junction is to supply current to the SFQ gates. As illustrated in Fig. 1, the AC bias current is delivered by a bias line carrying a sinusoidal current

$$I_{\mathrm{AC}}(t) = I_0 \sin(\omega t) \tag{1}$$

where I_0 is the peak amplitude of the current, $\omega = 2\pi f$ is the angular frequency, and t is time. A mutual inductance M couples this bias line to an inductor L_2 in series with the bias junction. L_1 denotes the self-inductance of the transmission line segment coupled to the bias junction. Due to the mutual inductance, the ac bias induces a time varying magnetic flux in the grounded loop formed by the JJ and inductor L_2

$$\Phi_{\mathrm{ind}}(t) = M I_{\mathrm{AC}}(t). \tag{2}$$

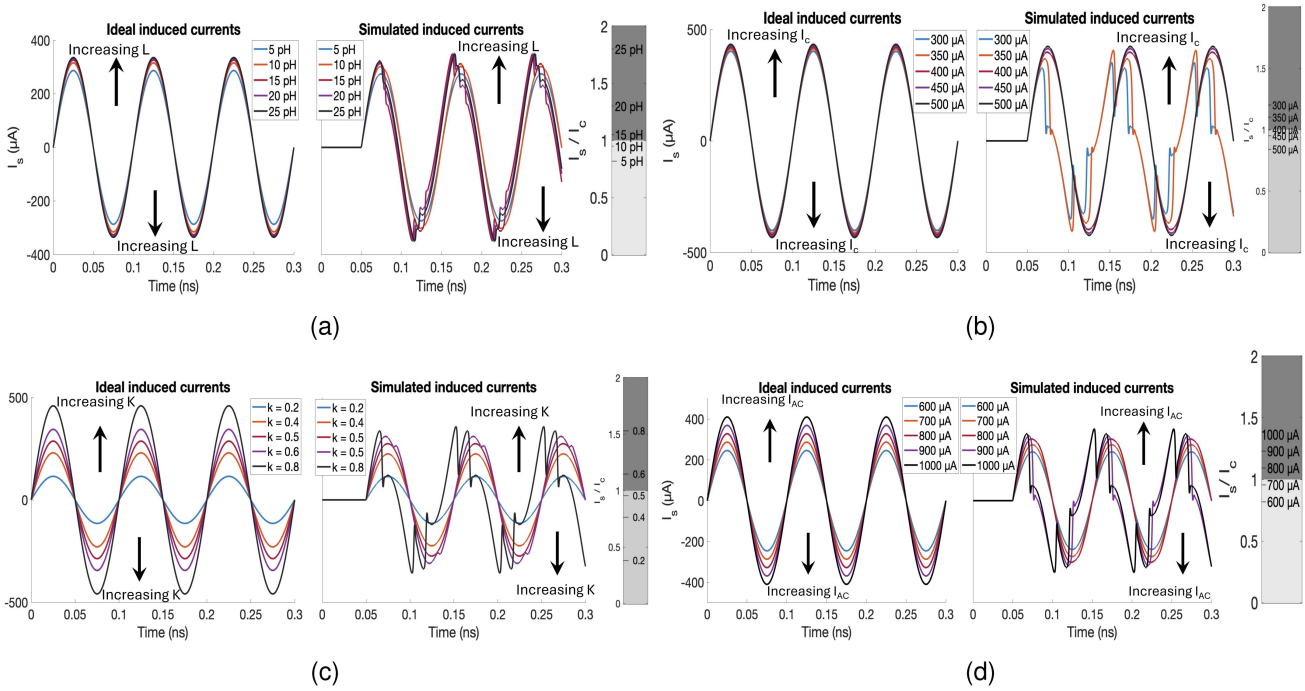

Fig. 2. Model and simulation of sinusoidal current waveform induced in the bias junction J_B, (a) inductance $L1 = L2$, (b) critical current I_c, (c) coupling factor k, and (d) peak current of transmission line I_{AC} . The fixed parameters for each subplot are listed in Table I. These waveforms operate at a frequency of 10GHz. The light gray region corresponds to the safe range $0 < I_s/I_c \leq 1$, while the dark gray region indicates distortion due to $I_s/I_c > 1$.

TABLE I
SIMULATION PARAMETERS FOR THE FOUR SUBPLOTS SHOWN IN FIG. 2

Varied parameter	L (pH)	I_c (μA)	k	I_{AC} (μA)
L	—	300	0.5	700
I_c	10	—	0.5	700
k	10	300	—	700
I_{AC}	10	300	0.5	—

Each row depicts the fixed values when the listed parameters are varied.

Applying Kirchhoff's voltage law around the loop yields a differential equation governing the phase dynamics and current response

$$L_2 \frac{dI_s}{dt} + \frac{\Phi_0}{2\pi}\frac{d\delta}{dt} = M\frac{dI_{\mathrm{AC}}}{dt} \tag{3}$$

where I_s is the induced current through the bias junction, Φ_0 is the magnetic flux quantum, and δ is the Josephson phase difference across the junction.

In the ideal case where the junction is absent, the system behaves as a linear transformer, and the induced current is

$$I_s(t) = \frac{M}{L_2} \cdot I_{\mathrm{AC}}(t). \tag{4}$$

To incorporate the effects of the Josephson inductance, which arises from the nonlinear current-phase relationship of the junction, the induced current becomes

$$I_s(t) = \frac{M}{L_2 + L_J} \cdot I_{\mathrm{AC}}(t) \tag{5}$$

where L_J is the Josephson inductance, approximated for small-signal operation as

$$L_J = \frac{\Phi_0}{2\pi I_c} \tag{6}$$

with I_c denoting the critical current of the junction and $\Phi_0 \approx 2.07 \times 10^{-15}$ Wb representing the magnetic flux quantum [2].

Substituting the expression for the mutual inductance $M = k\sqrt{L_1 L_2}$, where k is the coupling coefficient, into (5), the approximation for the induced current becomes

$$I_s(t) = \frac{k\sqrt{L_1 L_2}}{L_2 + \frac{\Phi_0}{2\pi I_c}} \cdot I_{\mathrm{AC}}(t). \tag{7}$$

The junction switches when the induced current surpasses the critical current

$$I_s(t) > I_c. \tag{8}$$

Since switching the junction affects the behavior of the coupled RSFQ circuit (see Fig. 3), switching is prevented, only occurring when the induced current is sufficiently large. To avoid unintended switching, the induced current $I_s(t)$ is maintained below the critical current I_c of the junction. This condition is expressed as

$$0 < \frac{I_s(t)}{I_c} \leq 1. \tag{9}$$

As depicted in Fig. 2, distortion occurs in the induced current signals when J_B switches. The relationship in (7) shows the dependence of $I_s(t)$ on L_1, L_2, k, and I_c, guiding the parameter selection process. The distortion effects, as depicted in Fig. 2, are determined from an analysis of the bias junction circuit with an

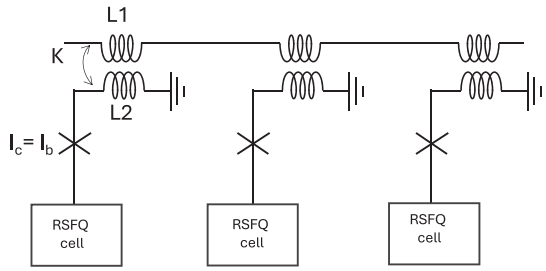

Fig. 3. AC bias of RSFQ circuits with bias junction.

ac bias, as shown in Fig. 1. The waveform represents the induced current I_s at node 2 of the Josephson junction J_B. The simulations are performed in Cadence using the WRSPICE-based JJ model from WRCAD.

As shown in Fig. 3, the bias junction is not directly grounded but is connected to the bias current injection node of the RSFQ circuits. This configuration ensures a precise supply of bias current, set by the bias junction, to the RSFQ circuits. The critical current of the bias junction is the same as the current required by the RSFQ cell connected to the junction. Since $I_c = I_B$, L_1 and L_2 are chosen to satisfy (7). The maximum and minimum bias current required by the RSFQ circuits connected to the ac transmission line determines the amplitude of I_{AC}. This range of bias current is the timing margin which refers to the window within each ac cycle during which this induced current remains above the threshold to maintain correct gate operation. Although a common I_{AC} is used for multiple RSFQ gates, the induced current at each bias point is independently regulated by the parameters k, L, and I_c, ensuring that each gate receives the required bias current to maintain correct operation without exceeding the switching threshold.

The RSFQ cells should be clocked at the frequency of the ac bias line to ensure correct operation. The total bias current supplied to the RSFQ circuits is the peak amplitude of the sinusoidal current. Therefore, the total current received by the RSFQ circuits is less than the peak current. The amplitude of the current affects the operating margin. Consider three RSFQ circuits: A Josephson transmission line (JTL) [24], a NOT gate, and a splitter, requiring, respectively, bias currents of 280 μA [25], 425 μA, and 300 μA [24].

Bias margin refers to the allowable range of I_{AC} that maintains sufficient current at the splitter input, while *timing margin* refers to the temporal window within each ac cycle during which this bias current remains above the threshold to ensure correct gate operation. These two margins jointly define the operational window. The operational bias margin to maintain correct operation is therefore determined by both the current tolerance and duration within each ac cycle in which the induced current exceeds the minimum level of current.

Using conventional dc bias currents, these circuits would collectively require a total bias current of 1.01 mA. However, when employing bias junctions connected to an ac bias transmission line, as depicted in Fig. 4(a) with the output signal of each

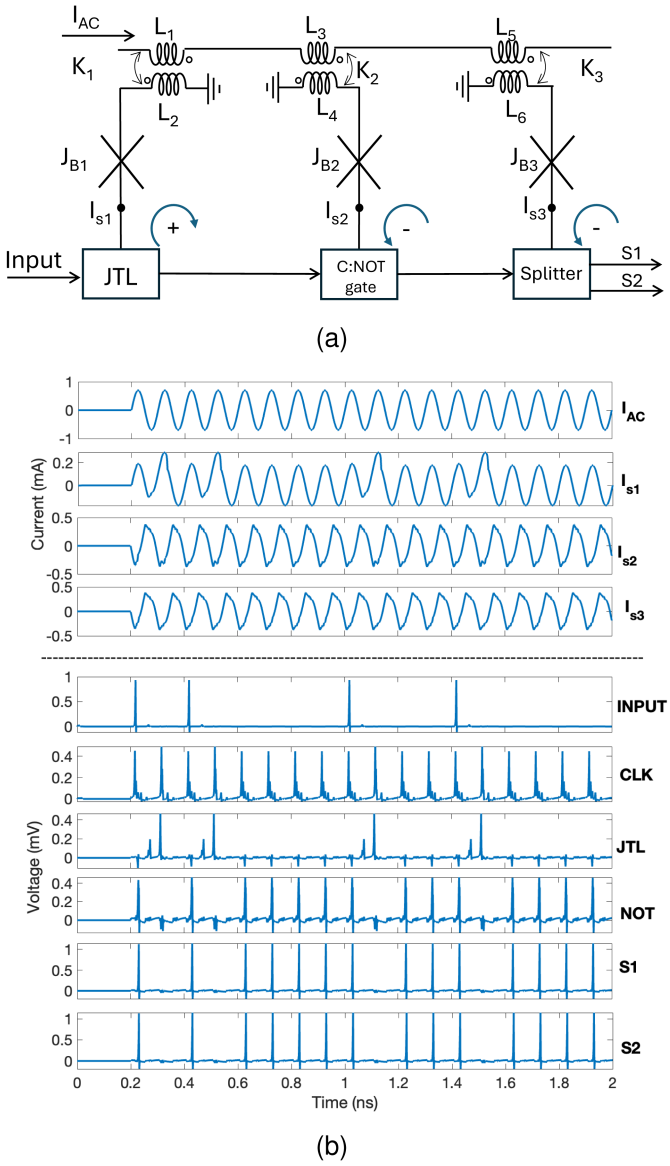

Fig. 4. AC bias of RSFQ circuits, (a) circuit diagram, and (b) I_{AC} signal, induced current I_s signals and output signals of each gate. $I_{AC} = 700$ μA at 10GHz, $L_1 = L_2 = 14$ pH, $L_3 = L_4 = L_5 = L_6 = 20$ pH, $K_1 = 0.3$, $K_2 = K_3 = 0.7$, $I_{c1} = 280$ μA, $I_{c2} = I_{c3} = 300$ μA.

circuit depicted in Fig. 4(b), the same three circuits collectively utilize a total ac current I_{AC} of 700 μA, a current reduction of approximately 30% .

B. Tradeoffs to Reduce Current

Additional delay is a primary issue with this approach as the junctions in the RSFQ circuits wait to receive sufficient current before switching. When the circuits are clocked at the same frequency, the splitters, confluence buffer, and those SFQ cells that do not require a clock can introduce a delay that affects the correct operation of the circuit. As depicted in Fig. 4(b), the ac bias introduces a delay of 93 ps in the JTL while a dc bias introduces a delay of 5 ps. Although current is saved, the added

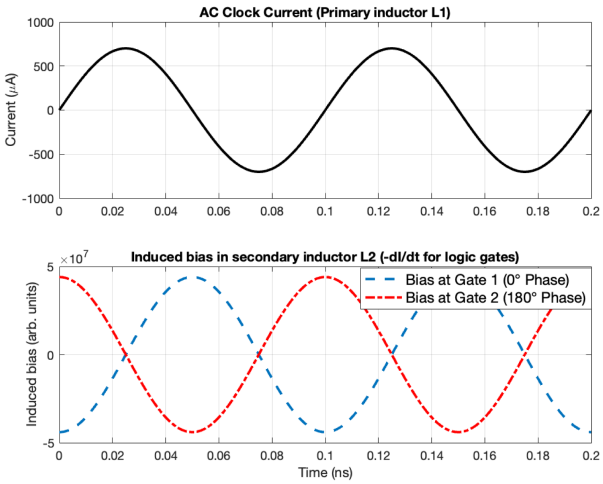

Fig. 5. Induced voltage across the secondary inductor of a clocked SFQ gate receiving an ac bias. The polarity alternates with the ac phase, motivating the alternate grounding scheme described in Section III-B.

delay and greater complexity are significant, a major drawback when applying an ac bias to RSFQ circuits.

As depicted in Fig. 4(a), clocked gates such as a NOT gate adds design complexity since the phase of the ac sinusoidal current changes whenever a gate is biased by an external clock. In a single ac transmission line with two phases, 0° and 180°, the polarity of the bias inductor alternates between logic stages to maintain a constant polarity. As illustrated in Fig. 5, although the bias current is a single sine wave, each half cycle (positive and negative) powers alternating stages within the logic pipeline. The 0° phase corresponds to the positive half cycle, and the 180° phase to the negative half cycle. Since the direction of the current in the primary transformer reverses every half cycle, the polarity of the voltage induced in the secondary inductor also reverses. If the same end of the inductor is grounded in both stages, the resulting bias current changes direction, preventing the SFQ circuit from switching effectively. By alternating the grounded terminal of the secondary inductor between pipeline stages, the direction of the induced bias current entering the SFQ gate remains the same, despite the 180° phase shift in the primary ac current. This technique ensures reliable and uniform operation across all of the clocked stages and considers the winding orientation in mutual inductance models. Alternate grounding is only required for the clocked logic gates, such as AND, OR, and XOR gates, where the switching behavior depends upon receiving the bias current with the correct polarity and timing aligned to the proper clock phase. In contrast, nonlogic cells, such as JTLs, splitters, and confluence buffers, are phase agnostic. The nonlogic cells are self-timed and operate correctly as long as sufficient bias current is received regardless of the polarity. Alternating the grounded end of the inductor is therefore unnecessary in nonlogic cells , even when connected to the same ac transmission line. Due to the increased complexity in managing the current direction and timing alignment across deep logic pipelines, this approach is not extended to clocked logic gates. The proposed ac bias method is therefore intentionally limited to the splitter networks to ensure scalability and robust operation.

When multiple RSFQ gates with different current requirements are biased by a common ac source, the fixed inductance, coupling coefficient, and waveform amplitude can cause the ac bias current for certain gates to exceed the required current. This excess current may couple into adjacent cells through a parasitic mutual inductance, leaking current and producing unintended switching activity. These effects manifest as voltage perturbations in the output of the JTL waveform, as depicted in Fig. 4(b). The leakage currents reflect the challenge of using a shared ac bias for cells with nonuniform current demand. To avoid these limitations, the proposed method selectively applies an ac biasing to the clock splitter circuits, where the bias requirements are well understood with a similar bias margin and intercell interference is minimal.

IV. AC Biasing of Clock Splitters

The advantages of ac power comes with tradeoffs in longer delay and added circuit complexity. To address the issue of high bias current, applying ac biased junctions to only the clock signal splitters is proposed. The splitters within the clock network are a major source of bias current. This approach shifts the delay of the RSFQ logic gates to the clock distribution network, where the delay characteristics can be managed by the ac biased clock topology. The complexity of the clocked gates (alternating phase) is also lessened while significantly reducing the bias current and maintaining compatibility with existing RSFQ logic families. The timing characteristics of the clock splitters incorporating bias junctions is presented in Section IV-A, while the use of ac biased splitters in benchmark circuits is explored in Section IV-A.

A. Timing Characteristics of AC Bias Propagation in SFQ Clock Trees

As discussed in Section III-B, the sinusoidal nature of the ac bias introduces delay. AC biased splitters are placed within the clock distribution network where the clock pulse arrival time is known. The delay of the clock network can be managed while reducing the required current. This effect is achieved by combining the dc bias for the logic gates with the ac bias for the clock splitters. The ac bias current and the clock signal are synchronized to the same frequency, ensuring that the clock pulses arrive within the timing margin $Rang$, as illustrated in Fig. 6. An ac biased splitter is illustrated in Fig. 7, where each splitter utilizes a bias junction with a critical current of $I_c = 300\ \mu$A, inductance $L_1 = L_2 = 20$ pH, and operates at a clock frequency of 10 GHz. With a dc bias, the delay per splitter stage is approximately 1.8 ps, assuming the 10 KA/cm^2 MIT Lincoln Laboratory SFQ5ee fabrication process [26]. Unlike dc biased circuits, ac biased SFQ clock networks rely on a time varying bias current distributed through a hierarchical tree of splitters.

The current delivered to a clock splitter is described by (7) provided the bias range to prevent switching of J_B, determined by (9), is satisfied. The resulting time margin Δt_{op}, the intervals during which the current remains above I_c of J_B,

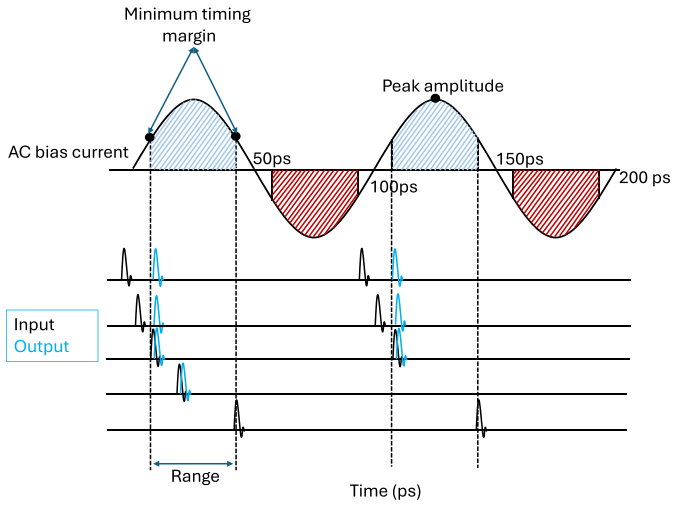

Fig. 6. Timing margin, range, and delay introduced by the ac bias splitters.

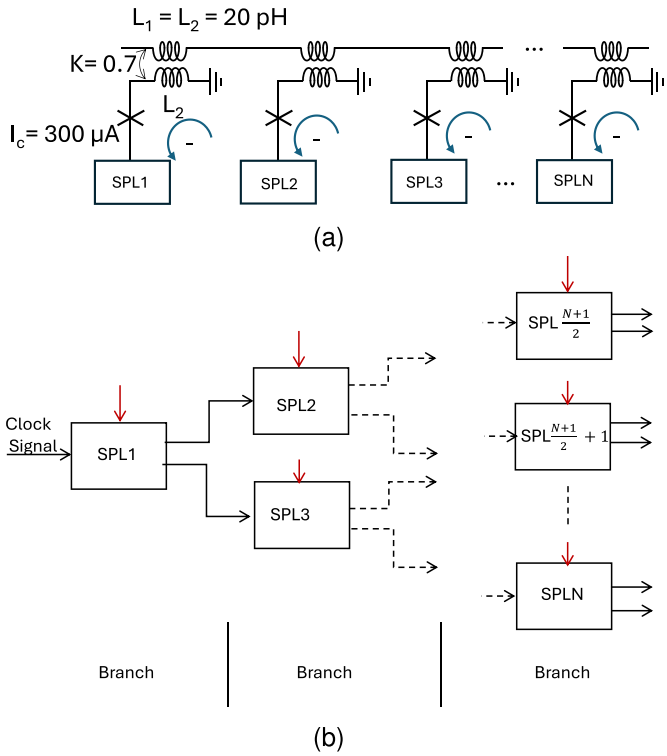

Fig. 7. AC bias of clock splitters with bias junction, (a) ac transmission line, and (b) splitter tree to optimize delay

is

$$\Delta t_{\text{op}} = \frac{1}{\omega}\left[\arcsin\left(\frac{I_c}{\alpha I_{\text{AC}}}\right) - \arcsin\left(\frac{0.01 I_c}{\alpha I_{\text{AC}}}\right)\right] \tag{10}$$

where the effective coupling factor α accounts for the Josephson inductance which is

$$\alpha = \frac{k\sqrt{L_1 L_2}}{L_2 + \frac{\Phi_0}{2\pi I_c}}. \tag{11}$$

A derivation of the timing margin expression is provided in the Appendix. To ensure the presence of a timing margin of induced current, the minimum ac peak amplitude to guarantee correct operation is

$$I_{\text{AC}}^{\min} = \frac{I_c}{\alpha} = \frac{I_c\left(L_2 + \frac{\Phi_0}{2\pi I_c}\right)}{k\sqrt{L_1 L_2}}. \tag{12}$$

While $I_{\text{AC}}^{\min}$ is the theoretical threshold required to achieve the maximum bias margin, this value often corresponds to a high ac current that offers little practical benefit over significantly lower amplitudes. To describe the maximum achievable timing window, consider the case where the induced current covers the range from $0.01 I_c$ to I_c during a sinusoidal cycle. The corresponding timing margin is

$$\Delta t_{\max} = \frac{1}{\omega}\left[\arcsin(1) - \arcsin(0.01)\right]. \tag{13}$$

In many practical scenarios, significantly lower ac amplitudes, however, result in timing margins that are nearly indistinguishable from $\Delta t_{\max}$ due to the flatness of the arcsin function near the upper bound. To reduce power consumption while preserving timing robustness, a practical ac amplitude $I_{\text{AC}}^{\text{practical}}$ is the smallest ac current that produces a timing margin within a small tolerance δ of $\Delta t_{\max}$

$$I_{\text{AC}}^{\text{practical}} = \min\left\{ I_{\text{AC}} \,\middle|\, \Delta t_{\text{op}} \geq \Delta t_{\max} - \delta \right\}. \tag{14}$$

In a binary clock tree, each splitter branch [27] exhibits a propagation delay d_{branch} of 1.8 ps [26]. The number of branches that can be supported within the available timing margin is

$$N_{\text{branch}} = \left\lfloor \frac{\Delta t_{\text{op}}}{d_{\text{branch}}} \right\rfloor \tag{15}$$

resulting in a target fanout

$$\text{Fanout} = 2^{N_{\text{branch}}}. \tag{16}$$

To drive a target fanout requiring Fanout $-$ 1 splitters, the number of necessary ac bias sources is

$$\text{Number of AC sources} = \left\lceil \frac{N_{\text{branch}} \cdot d_{\text{branch}}}{\Delta t_{\text{op}}} \right\rceil. \tag{17}$$

The timing characteristics for different clock networks across a range of frequencies, from 5 to 40 GHz, are listed in Table II. The minimum ac current, maximum timing margin, total delay, and corresponding number of bias sources needed to support the fanout of an SFQ clock tree at different operating frequencies are listed in the table.

B. AC Bias Source Insertion and Phase Alignment Between Sources in Clock Splitter Tree

The maximum timing margin $\Delta t_{\max}$ decreases with increasing frequency due to the smaller time margin of the ac current bias. For example, $\Delta t_{\max}$ drops from 46.8 ps at 5 GHz to 5.8 ps at 40 GHz. This reduction limits the number of branches that can be supported by a single ac source. Despite this constraint, as depicted in Fig. 8, high fanouts can be achieved by inserting additional ac bias sources within the tree. For example, a 25 branch

TABLE II
TIMING CHARACTERISTICS OF AC BIASED SPLITTER TREE FOR DIFFERENT FANOUTS AND FREQUENCIES

Branches	Fanout	Total delay (ps))	Frequency (GHz))	$I_{\mathrm{AC}}^{\min}$ (mA)	Maximum timing margin $\Delta t_{\max}$(ps)	Number of bias sources
1	2	1.8	5	0.4	46.8	1
			10	0.4	23.4	1
			20	0.4	11.7	1
			40	0.4	5.8	1
5	32	9.0	5	0.4	46.8	1
			10	0.4	23.4	1
			20	0.4	11.7	1
			40	0.8	5.8	2
9	512	16.2	5	0.4	46.8	1
			10	0.4	23.4	1
			20	0.8	11.7	2
			40	1.2	5.8	3
10	1,024	18.0	5	0.4	46.8	1
			10	0.4	23.4	1
			20	0.8	11.7	2
			40	1.6	5.8	4
15	32,768	27.0	5	0.4	46.8	1
			10	0.8	23.4	2
			20	1.2	11.7	3
			40	2.0	5.8	5
20	1,048,576	36.0	5	0.4	46.8	1
			10	0.8	23.4	2
			20	1.6	11.7	4
			40	2.8	5.8	7
25	33,554,432	45.0	5	0.4	46.8	1
			10	0.8	23.4	2
			20	1.6	11.7	4
			40	3.2	5.8	8

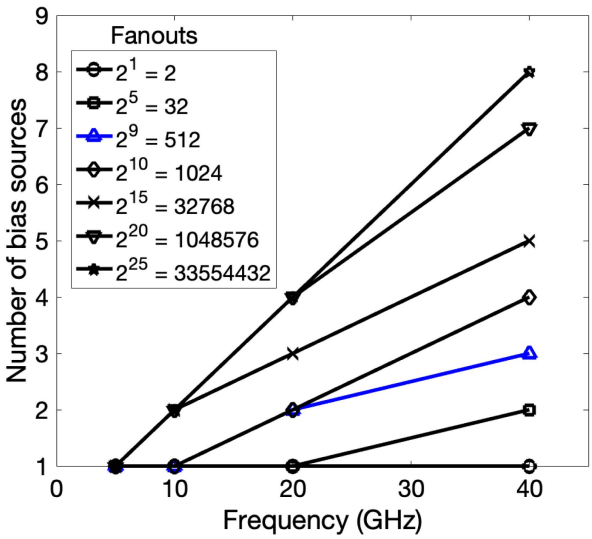

Fig. 8. Number of bias sources as a function of fanout and frequency.

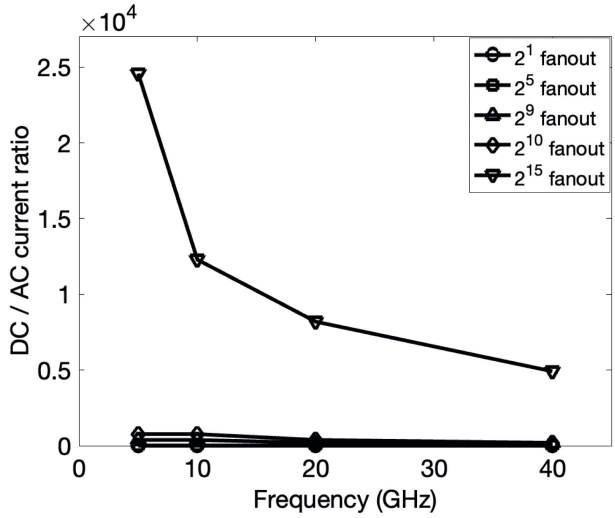

Fig. 9. DC/AC current ratio of clock splitter tree as a function of frequency and fanout. Note that the dc current is constant with frequency while the ac current varies with frequency.

splitter tree with a fanout of more than 33 million can operate at 20 GHz with four bias sources and at 40 GHz with eight bias sources, as listed in Table II. These additional sources restore the timing margin lost to delay accumulation through each branch. Additional ac bias sources are introduced with controlled phase shifts, as depicted in Fig. 10(a), to ensure the second bias source begins to supply current before the previous source drops below the safe operating margin. The second ac source is phase shifted to ensure that the current exceeds the minimum acceptable value $0.01I_c$ precisely when the timing margin of the first source ends.

Phase Shift Condition

To maintain uninterrupted biasing

$$I_s(t = \Delta t_{\mathrm{op}}) = 0.01I_c. \tag{18}$$

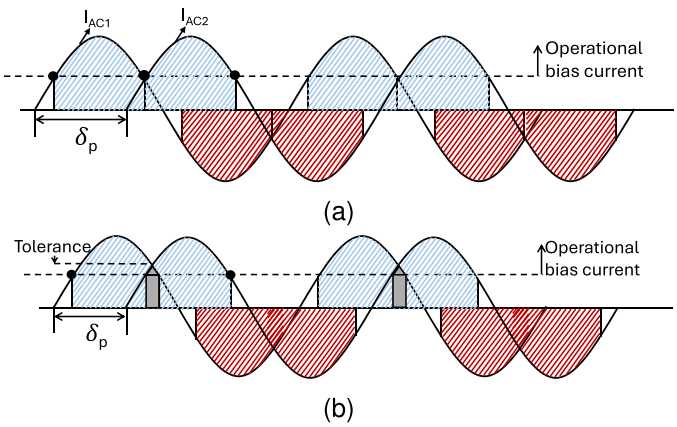

Fig. 10. Phase shift due to the insertion of a bias current source to restore the bias timing margin, (a) ideal, and (b) practical with overlap timing margin to tolerate fabrication variations.

Substituting (18) into the expression for $I_s(t)$

$$\alpha I_0 \sin(\omega \Delta t_{\text{op}} + \phi) = 0.01 I_c$$

which yields the required phase shift

$$\phi = \arcsin\left(\frac{0.01 I_c}{\alpha I_0}\right) - \omega \Delta t_{\text{op}}. \tag{19}$$

Expressed in degrees, the phase shift is

$$\delta_p = \arcsin^{\circ}\left(\frac{0.01 I_c}{\alpha I_0}\right) - 360^{\circ} \cdot f \cdot \Delta t_{\text{op}}. \tag{20}$$

This expression ensures that the second ac bias source delivers $0.01 I_c$ when the time margin of the preceding bias source ends, preserving a safe operating range across all branches within the clock tree.

Phase Overlap with Tolerance for Fabrication Variations

To ensure uninterrupted delivery of bias current to all branches of the RSFQ splitter tree, multiple ac bias sources are phase shifted. While the ideal phase shift δ_p aligns with the start of the operational current window of the second source with the end of the first source, practical considerations, such as fabrication variations, can cause small changes in component values (k, L, and I_c), as depicted in Fig. 10(b). These variations can shrink the operational time margin and introduce discontinuities in current delivery.

To mitigate this risk, the ac bias sources are slightly overlapped, ensuring that the second source begins supplying current slightly before the first source drops below the minimum threshold, as depicted in Fig. 10(b). This intentional phase overlap provides a margin of tolerance, ensuring that the continuous flow of bias current is preserved to compensate for process induced uncertainties despite the presence of small parameter variations.

The amplitude of the ac current to maintain correct operation $I_{\text{AC}}^{\text{min}}$ remains relatively low (0.4 mA) at low frequencies and few branches but gradually increases as the frequency and/or number of branches increase. This increase in current reflects the additional current source(s) to maintain sufficient timing margin in deep trees. As depicted in Fig. 11, the output of a six branch splitter tree biased by two ac sources at 20 GHz with $I_{AC} = 700\,\mu$A is shown. As the operational time margin of the first bias source elapses, the second bias source, phase shifted by -70°, continues to supply bias current. From (20), the estimated phase shift is -71.4°; however, -70° is used to incorporate some tolerance to fabrication variations. This waveform validates SFQ pulse propagation and demonstrates consistent splitter behavior across all of the branches.

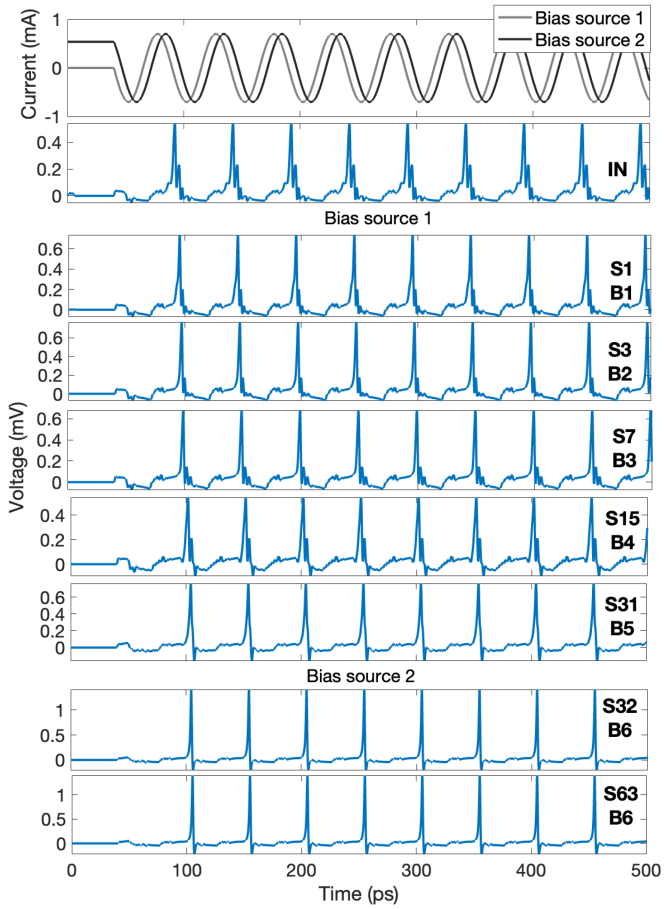

Fig. 11. Clock output waveform of final splitter in each branch, corresponding to the splitter tree structure shown in Fig. 7. The labels follow the convention S–splitter and B–branch format. The input clock (IN) operates at 20 GHz and is applied to the root splitter. Both ac bias sources provide sinusoidal waveforms at 20 GHz with a peak amplitude $I_{AC} = 700\,\mu$A. Bias Source 2 is phase shifted by -70° relative to Bias Source 1 to extend the operational bias margin beyond Branch 5. The transition between Bias Sources 1 and 2 occurs between Branches B5 and B6. SFQ pulse propagation is observed in all of the branches.

At frequencies greater than 100 GHz, the timing margins shrink significantly and may be less than the delay of a single splitter, requiring an unpractical number of additional ac sources. This constraint reflects a fundamental limitation of high frequency ac biasing [28], [29], [30]. A comparison of dc and ac biasing for clock splitters, as listed in Table III, highlights the advantages and drawbacks of both biasing methods for a splitter tree. Nevertheless, ac biasing remains robust: Reliable operation is provided for high fanout while maintaining signal integrity with relatively low current, as depicted in Fig. 9. Unlike AQFP logic [18], where the ac waveform functions as a clock signal requiring strict phase alignment, the proposed method

TABLE III
COMPARISON OF DC AND AC BIASING FOR CLOCK SPLITTERS

Feature	DC Biasing	AC Biasing
Bias current	Constant per frequency and Increases steeply with fanout	Varies with frequency and Increases gradually with fanout
Current for 2^1 fanout	0.3 mA	0.4 mA (all freq.)
Current for 2^{15} fanout	9,830 mA	0.4–2.0 mA
Number of bias sources	One	Up to five for practical circuits (depends on depth/ frequency)
Static power dissipation	High	None (zero average)
Scalability for deep trees	Poor	Scalable with source insertion

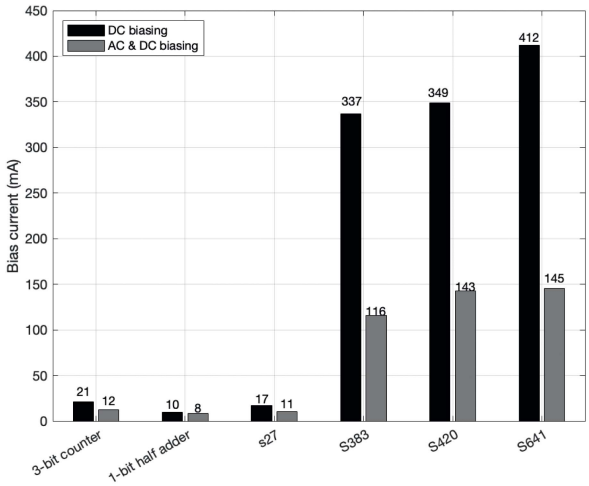

Fig. 12. Bias current of ac biasing of splitter tree and dc biasing of RSFQ circuits in modified ISCAS'89 benchmark and other RSFQ circuits.

uses the ac waveform solely for biasing. Intersource jitter and phase drift do not affect logic operation, since data propagation relies on the SFQ pulses generated within the RSFQ clock tree.

C. Application of AC Biased Clocked Splitters to RSFQ Circuits

An ac biased clock splitter has been applied to SFQ modified ISCAS'89 benchmark circuits [31] with a fanout of at most 512. The circuits operate correctly with some delay, as listed in Table II. The total current consumed by the circuits using ac biased clock splitters is significantly reduced, as depicted in Fig. 12. DC biasing is used to address the critical path of the logic circuits, while ac biasing is used to address the noncritical paths within the clock networks. The bias current utilized by the RSFQ gates, illustrated in Fig. 12, is the same for both ac and dc biasing. The reduction in current is achieved through the use of ac biased clock splitters, requiring only 400 μA (ac source at 10 GHz) for a fanout of 512 while full dc biasing requires 153.3 mA.

V. ARCHITECTURAL AND DESIGN CONSTRAINTS OF AC BIASED CLOCK SPLITTERS

Architecture and related design constraints of the proposed method of selectively applying an ac bias to the clock splitters in RSFQ circuits to reduce the total current is explored in this section. A comparison of the proposed method with other superconductive logic families is discussed in Section IV-A. Area challenges are explored in Section IV-A. Physical design and timing synchronization are, respectively, discussed in Sections IV-C and IV-D.

A. Comparison With Other Superconductive Logic Families

As compared to RQL [4] and AQFP [18], the proposed approach retains the speed and architectural circuit topology of RSFQ while utilizing energy saving elements from AC biased systems. RQL circuits achieve power efficiency by AC biasing standard logical operations. This effect, however, requires strict clock phase requirements and limited circuit complexity. AQFP circuits offer exceptionally low energy dissipation through adiabatic switching although operate at relatively slow frequencies (less than 5 GHz) [18], [32]. In contrast, the method proposed here operates at gigahertz frequencies while avoiding the complexity of multiphase, multiclock synchronization required by RQL and AQFP. The key differences between the proposed ac biasing method and more common ac-to-dc converter-based approaches are summarized in Table IV. The proposed approach descibed here offers an accessible path for reducing current demand in large scale RSFQ circuits.

ERSFQ (energy efficient rapid single flux quantum) does not employ ac biasing, but provides an alternative method for eliminating static power dissipation in RSFQ circuits [33], [34], [35]. ERSFQ replaces resistive biasing with inductors and Josephson junctions and uses a feeding JTL to maintain a dc bias without dissipating static power. Compatibility with standard RSFQ gate structures is preserved, and the complexity of an ac distribution system is avoided. The ERSFQ method, however, introduces additional design constraints, including bias current balancing and additional circuitry. The proposed approach applies inductively coupled ac biasing exclusively to the clock splitters.

B. Transformer Count and Area Optimization

A key design issue in the proposed approach is the number of transformers, a common issue in all inductively coupled ac biased superconductive circuits. Each bias junction demands a dedicated transformer or mutual inductor, both of which require significant area. This requirement is, however, only within the clock distribution network—where uniformity and regularity in the layout of the clock splitters can be exploited. Design techniques, such as transformer sharing schemes, multi-output coupling, and hierarchical ac distribution networks [36], are viable strategies to lower the transformer overhead while preserving signal integrity and timing margins. These transformer related overheads are not unique to this approach but are common to all inductively coupled ac biased systems, including RQL and AQFP [29].

TABLE IV
COMPARISON OF PROPOSED AC BIASING IN SPLITTER TREES VERSUS AC-TO-DC CONVERTERS IN RSFQ CIRCUITS

Method	JJ Overhead	Current Reduction	Delay Impact
AC-to-DC converter [22]	Nine JJs per bias point	Not reported	Not reported
AC-to-DC converter [23]	Five JJs per bias point	Not reported	Not reported
This work Fig.12	One JJ per bias point	94% (splitters), 62% (total)	∼1.8 ps per branch

C. Physical Layout Congestion

Integrating ac biasing into RSFQ circuits introduces layout considerations. The placement and routing of the ac transmission lines and coupled transformers need to be considered to ensure minimal crosstalk, uniform phase alignment, and balanced current delivery [21]. However, since the proposed technique is limited to clock splitters, the layout complexity is significantly reduced as compared to applying ac biasing to a complete system. The need for alternating ground schemes is avoided in passive cells such as splitters and confluence buffers, further simplifying the design process.

D. Timing Synchronization and Clock Tree Planning

The proposed approach enables highly predictable timing within the clock distribution network. By determining the timing margins, fanout, and bias current supplied to the splitters, deterministic timing behavior is achieved. The design methodology systematically adjusts the number of ac bias sources to maintain operational windows across the clock network. The clock arrival times are decreased, and large scale splitter trees can be constructed while satisfying tight timing margins. Clock tree planning ensures robust synchronization across wide fanouts despite operating at high frequencies.

As compared to conventional dc biasing, the ac biasing method exhibits a narrower global operating margin for the bias amplitude. For dc biased RSFQ gates, a typical current margin is approximately $\pm 25\%$, reflecting relatively static and robust current delivery. In the proposed AC biasing approach, the corresponding margin for I_{AC} across all splitter branches is approximately $\pm 17\%$. This margin sets the acceptable ac amplitude that maintains correct switching in all splitters without distortion or underbiasing. In addition, ac biasing introduces a local timing margin due to the phase dependent nature of the induced current. This behavior necessitates the use of additional bias sources with controlled phase shifts to preserve reliable operation over large splitter trees, as shown in Fig. 10(a). These considerations highlight the tradeoffs between dc and ac biasing strategies for scalable RSFQ clock distribution networks.

VI. CONCLUSION

As superconductive digital systems continue to evolve, managing power consumption while scaling circuit complexity remains a critical challenge. RSFQ logic offers fast switching times and low dynamic power, but reliance on resistive dc biasing leads to significant static power dissipation and high bias currents which limits large scale integration. Reducing these overheads without altering established RSFQ architectures is essential for the broader adoption of superconductive electronics. A hybrid biasing approach to reducing current consumption in RSFQ circuits by applying ac biasing to the clock splitters and dc biasing to the logic gates is proposed. This technique significantly lowers the bias current requirements, achieving an average reduction of 94% in clock splitter current and a 62% reduction in total current in SFQ benchmark circuits. This approach introduces a JJ overhead of 6.5% while maintaining compatibility with existing RSFQ logic families. An additional benefit of the proposed ac biasing approach is the elimination of static power dissipation, a primary issue in dc biased RSFQ circuits. Since the bias current is inductively delivered during specific clock phases, the resistive current paths are removed, improving overall energy efficiency. The ac biased splitter network can exhibit significant deterministic delay characteristics governed by a sinusoidal bias waveform. This delay issue, however, can be mitigated through strategic clock tree design [37]. Furthermore, by isolating the ac bias to the clock network, the complexity and delay penalties associated with clocked logic gates in fully ac biased systems are less pronounced. The scalability of this method is demonstrated on benchmark circuits and supports the practical use in large scale SFQ systems. As superconductive technologies advance, this hybrid biasing technique represents a path forward for low power, high density SFQ circuit integration without requiring fundamental changes to existing logic cell libraries. The proposed ac biasing method is selectively applied to the splitters within the clock distribution network, while the RSFQ logic gates remain dc biased, ensuring compatibility with existing RSFQ design practices and cell libraries and reducing current without altering the logical operation. Future directions include transformer sharing, multi-output coupling, and ac aware clock tree synthesis to reduce transformer overhead.

APPENDIX A
DERIVATION OF TIMING MARGIN

The induced current is

$$I_s(t) = \alpha I_0 \sin(\omega t) \tag{A.1}$$

where

$$\alpha = \frac{k\sqrt{L_1 L_2}}{L_2 + \frac{\Phi_0}{2\pi I_c}}. \tag{A.2}$$

As established earlier, the normalized current must satisfy

$$0 < \frac{I_s(t)}{I_c} \leq 1. \tag{A.3}$$

To determine the time interval for which this condition holds, the lower bound must be greater than zero. The lower bound is approximated as $0.01 \cdot I_c$, representing a small nonzero induced current sufficient for stable biasing.

Thus, the inequality is

$$\frac{0.01I_c}{\alpha I_0} \leq \sin(\omega t) \leq \frac{I_c}{\alpha I_0}. \tag{A.4}$$

Solving for time

$$\omega t_1 = \arcsin\left(\frac{0.01I_c}{\alpha I_0}\right), \tag{A.5}$$

$$\omega t_2 = \arcsin\left(\frac{I_c}{\alpha I_0}\right). \tag{A.6}$$

The time margin is

$$\Delta t_{\text{op}} = \frac{1}{\omega}\left[\arcsin\left(\frac{I_c}{\alpha I_0}\right) - \arcsin\left(\frac{0.01I_c}{\alpha I_0}\right)\right]. \tag{A.7}$$

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