Current Recycling in Heterogeneous RSFQ Circuits

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***Abstract*—As single flux quantum (SFQ) circuit complexities scale, larger bias currents are required. The large current produces excessive heat and greatly complicates the design process. Current recycling offers a solution by reducing the required bias current through serially biased circuit blocks. Serial biasing is typically achieved in homogeneous SFQ systems where similar bias currents are required in similar circuits. Each of these homogeneous circuits is often placed on different ground planes and serially biased to reuse the bias currents. To address heterogeneous circuits with varying bias current requirements, a novel serial biasing technique is proposed. An interface between the ground planes with unequal bias current is presented that exhibits a current balancing capability. The interface supplies additional current before passing the current to the next ground plane. The ground planes are arranged in ascending order of bias current to manage the complexity of these heterogeneous circuits. Using a one bit SFQ full adder as an example, the proposed approach demonstrates several key benefits: a 49% reduction in the number of driver-receiver pairs, a 6.5% reduction in power dissipation, and a 35% reduction in bias current across a heterogeneous SFQ circuit placed on three isolated ground planes. The performance, bias current margins, and methods for current reduction are also discussed, showcasing the effectiveness of current recycling in improving the efficiency of complex heterogeneous SFQ systems.**

***Index Terms*—Current recycling, driver-receiver pairs, heterogeneous circuits, non-galvanic signal transfer, RSFQ, serial biasing, single flux quantum, superconductive integrated circuits.**

I. Introduction

THE complexity of rapid single flux quantum (RSFQ) circuits grows with advances in the fabrication of superconductive electronics [1], [2]. The Josephson junctions (JJs) in RSFQ circuits require a DC bias current to operate [2]. The DC bias current is typically chosen as 70% of the critical current of a JJ [2], [3]. The significant DC current required to bias JJs has raised concerns, particularly in large scale RSFQ systems exceeding two amperes per integrated circuit. Practical limits affect how much current can flow in niobium wires and layer-to-layer vias [4]. These large currents cause detrimental effects such as excessive heat, electromagnetic interference, reduced operating margins, and magnetic coupling [1], [4]. Excess heat dissipation results from substantial DC bias currents, often tens to hundreds of amperes. The heat dissipation also contributes to the heat load of the cryocooler since RSFQ circuits operate at cryogenic temperatures below 4 K to maintain superconductive properties. To successfully scale SFQ circuits, it is crucial to reduce on-chip currents in large scale SFQ systems [5].

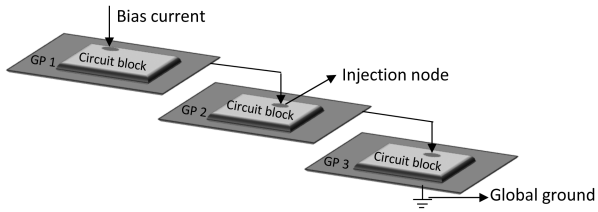

Fig. 1. Isolated ground plane for extraction and reuse of bias currents with the last ground plane connected to the global ground.

Current recycling is explored to reduce the DC bias currents required by SFQ circuits [6], [7]. Serial biasing of SFQ systems is used to achieve current recycling. Serial biasing passes the required bias currents to circuits placed on different grounds, as shown in Fig. 1. The method allows current to be reused by other circuit blocks on separate ground planes provided that the required bias current used by each circuit is similar [4], [8]. These circuits are individually grounded, each ground referred to here as a ground plane (GP), as depicted in Fig. 1. Serial biasing reduces the externally supplied DC current, scaling down the total current by a factor corresponding to the number of circuit blocks (or ground planes). Since the ground planes are isolated from each other, the clock and data signals are non-galvanically transferred without a physical connection between the ground planes. Non-galvanic signal transfer can be achieved using either inductive or capacitive coupling. Inductive coupling is typically preferred since less area is required [7]. Inductive coupling is used in a driver-receiver pair (DRP) to transfer SFQ signals across isolated islands, as depicted in Fig. 2. The DRP overhead grows as the number of isolated ground planes increases.

Serial biasing is typically achieved in circuits with similar bias currents (or circuit functions). Serial biasing of repetitive circuits with similar current is known as current recycling in homogeneous RSFQ circuits. Serial biasing in homogeneous RSFQ circuits has been previously demonstrated [4], [6], [9], [10]. For example, current is recycled within a seven stage counter [9] and a digital decimation filter [10]. In the filter, current is recycled across four isolated ground planes, with each plane consisting of master clock and toggle flip flops (TFFs), both non-destructive

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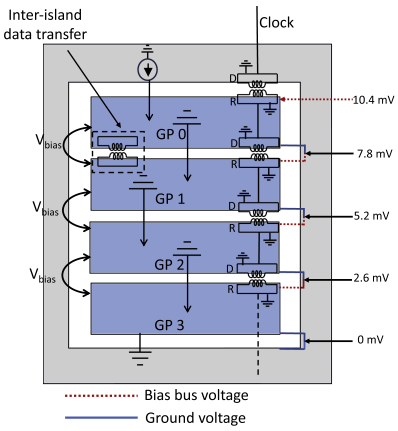

Fig. 2. Serial biasing with similar bias currents with a different bias bus and ground voltage at each ground plane (D - Driver, R - Receiver, and GP - Ground plane).

read out (NDRO) and destructive read out (DRO) [10]. Circuits with different logic functions and unequal bias current requirements, referred to as heterogeneous circuits, encompass various cells such as TFFs, NDROs, and logic gates such as AND, OR, and NOR. These circuits are collectively classified as heterogeneous circuits due to the varying bias current demand and function.

Current recycling in heterogeneous RSFQ circuits is the focus of this discussion. The proposed current recycling topology reduces the bias currents and number of inter-island DRPs, supporting current recycling within heterogeneous systems.

The structure of the paper is organized as follows: A brief background on current recycling, serial biasing, and driver-receiver pairs is provided in Section II. Classification of heterogeneous RSFQ circuits is discussed in Section III. A bias current balancing topology to aid current recycling in heterogeneous circuits is proposed in Section IV. Some conclusions are offered in Section V.

II. Principle of Current Recycling

The fundamental principles of current recycling are discussed in this section. The topology and operation of serial biasing are described in Section II-A. Non-galvanic signal transfer of the driver-receiver pair is described in Section II-B. DRP overhead is quantified in Section III-C.

A. Serial Biasing

Circuits with large bias currents are serially biased by partitioning the ground plane to reuse the bias currents [6]. Isolated ground planes are serially biased by connecting the GP to the DC bias current bus of the next isolated ground plane to achieve current recycling, as shown in Fig. 2. In serial biasing, the required DC bias current for each isolated ground plane should be similar to prevent both overbiasing and underbiasing of the logic circuits. A reduction of 1/N in DC bias current is achieved, where N denotes the number of isolated ground planes. The extracted bias current from the first isolated ground plane is supplied to the next isolated ground plane through a bias node called the bias injection node. Due to the resistive distribution of bias current to the bias injection node of the logic circuits, the bias bus voltage must be significantly higher than the maximum voltage at the injection nodes. The maximum voltage $V_{\max}$ is set by the highest frequency in the logic circuits, $V_{\max} = \phi f_{\max}$, where ϕ is the flux constant, $\phi = h/2e \approx 2.07$ mV $*$ ps (or 2.07 Webers) [3], and $f_{\max}$ is the maximum frequency. In this discussion, a difference in the bias bus voltage V_{bias} of 2.6 mV with respect to ground is assumed between adjacent isolated ground planes, as depicted in Fig. 2. If V_{bias} is insufficiently large, the voltage drop across the resistors distributing bias current may not be sufficiently close to the bias bus voltage, which may cause bias current allocation skew. This allocation skew is the improper distribution of current to bias the injection nodes [11]. Therefore, $V_{bias} >> V_{\max}$ to maintain stable operation.

B. Non-Galvanic Signal Transfer of the Driver-Receiver Pair

Most logic gates on each isolated ground plane are individually synchronized. As additional ground planes are introduced, the voltage across each ground plane increases by 2.6 mV, as shown in Fig. 2. This voltage increment is carefully chosen for several reasons:

- Proper operation of Josephson junctions: The voltage aligns with the characteristic gap voltage of niobium-based Josephson junctions, ensuring optimal circuit performance [12].
- Low static power dissipation: The 2.6 mV level minimizes power consumption while maintaining functionality [13].
- Noise immunity and stability: 2.6 mV provides a balanced choice to ensure signal integrity and system robustness [12].
- Standardization: Adopting the gap voltage of all-niobium Josephson junctions (2.6 mV) as a standard DC power supply ensures consistency across RSFQ circuits [3], [13].

This standard voltage level of 2.6 mV reflects the accepted gap voltage of all-Nb Josephson junctions and ensures reliable operation in RSFQ systems. The bias bus and preceding grounds maintain the same voltage, as the bias current is extracted by connecting the ground to the bias bus, as illustrated in Fig. 1. However, the voltage difference between the bias bus and ground voltage increases by 2.6 mV for each additional partition. The expression, 2.6 mV $*$ $(N - n)$, describes the bias bus voltage of each isolated plane, where N is the number of partitions and n is the index number of the ground plane (with $n = 0$ for the first current recycling stage). Due to this voltage difference, the clock and data signals cannot be directly transferred across isolated ground planes, as depicted in Fig. 2. To enable signal transfer, a DRP is employed. The driver is grounded on the transmitting ground plane, while the receiver is grounded on the receiving ground plane [6], [7], [14]. A DRP, shown in Fig. 3, uses an inductively coupled superconductive transformer for non-galvanic signal transfer between ground planes. The magnetic flux is stored in the driver for a duration longer than the switching time of the receiver but shorter than the

TABLE I
DRP OVERHEAD IN MODIFIED ISCAS'89 BENCHMARK CIRCUITS WITH BIAS IMBALANCE

Benchmark circuits	Parallel biasing (mA)	Serial biasing									
		N=2					N=4				
		Maximum bias current (mA)	DRP overhead		Balancing JTL overhead		Maximum bias current (mA)	DRP overhead		Balancing JTL overhead	
			Bias current (mA)	JJ count	Bias current (mA)	JJ count		Bias current (mA)	JJ count	Bias current (mA)	JJ count
s27	27	13.7	7.8	65	0.6	2	6.9	4	150	0.4	2
s298	382	192	15	147	2.5	8	96	30	995	1.3	4
s344	279	191	19	183	2.8	8	96	41	1340	1.6	5
s420	552	278	26	255	2.9	9	139	53	1700	1.8	7

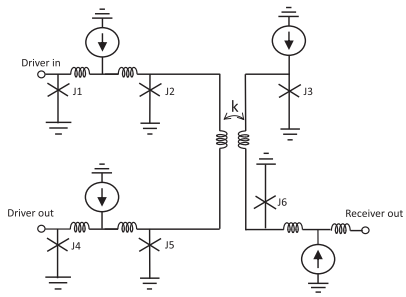

Fig. 3. Driver-receiver pair: the driver and receiver are on separate ground planes.

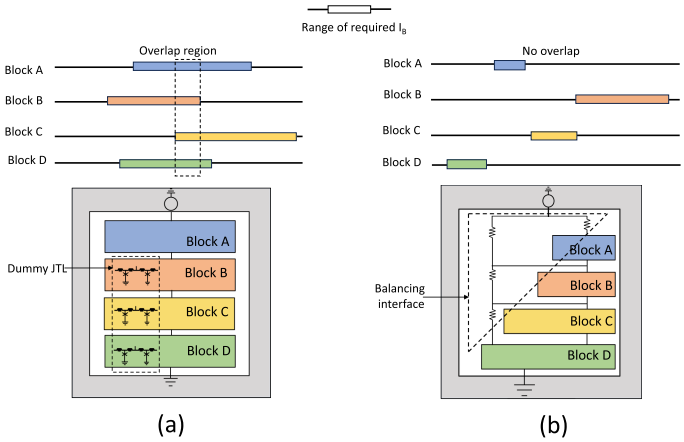

Fig. 4. Heterogeneous circuit classification for serial biasing, (a) overlap bias current range, and (b) non-overlap bias current range. The blocks represent circuits on isolated ground planes.

signal transmission speed, ensuring effective and reliable signal transfer [7].

C. Driver-Receiver Overhead

A DRP is necessary in current recycling to transfer clock and data signals across ground planes. The DRP overhead is composed of two components: the DC bias current overhead, which consists of the additional current required by a DRP, and the additional area of the JJ and superconductive transformer. The DC bias overhead is typically not significant, as any additional current can be recycled with current from the logic circuits. In large systems with many data paths, however, a large number of DRPs is necessary. The DRP overhead, characterized by the number of JJs and additional bias current for several ISCAS'89 benchmark circuits, is listed in Table I. The DRP overhead increases as additional partitions are required. Although the overall bias current is less, a large number of DRPs and superconductive transformers are required, presenting a tradeoff between the recycled current and physical area.

III. HETEROGENEOUS RSFQ CIRCUITS

Current recycling in SFQ systems is typically applied to repetitive circuit structures, homogeneous circuits, such as a shift register [6], [9], [10]. The assumption of homogeneous biasing, however, limits the generality of current recycling. A methodology for current recycling in heterogeneous circuits is necessary to support more complex and a wider variety of circuit applications. In complex heterogeneous circuits, the current should be recycled without requiring the individual circuit blocks to be similar. Heterogeneous circuits are not the same in terms of both logic gates and current requirements. Heterogeneous circuits can be different circuits with similar bias currents or different circuits with unequal bias currents. In different circuits with unequal bias currents, a bias imbalance occurs, which is the difference between the maximum and minimum bias current required by each isolated ground plane after partitioning [8].

The concept of serial biasing in heterogeneous circuits can be classified into two categories. The first category, known as the overlap bias range, pertains to those circuits that share a common operational range for bias currents; essentially, different circuits with a similar bias current. The second category, termed the non-overlap bias range, describes circuits that do not share a common operational range of bias currents; essentially, different circuits with unequal bias current. Serial biasing in the overlap bias range is explored in Section III-A. Serial biasing in the non-overlap bias range is explored in Section III-B.

A. Overlap Bias Range

Each circuit on each isolated ground plane has an individual bias margin. This bias margin characterizes the operating range of bias current for each circuit block with a local ground plane. If the operating range of a circuit block overlaps with another circuit block on a different local ground plane, as illustrated in Fig. 4(a), current can be successfully recycled. Serial biasing of the overlap bias current reduces the overall bias margin of a

system since the operating bias current range after serial biasing becomes smaller. If the bias margin is relatively low, device failure may occur [1]. To increase the bias margin, a Josephson transmission line (JTL) can be inserted into those circuits with a lower DC bias current to prevent overbias [8]. To minimize the number of JTLs, the isolated ground planes are arranged in descending order. The JTLs consume any excess bias current supplied by the preceding isolated block. This biasing scheme is most suitable for systems with a small imbalance in bias current between circuit blocks.

B. Non-Overlap Bias Range

Circuits with a larger bias imbalance, where the bias range does not overlap, fall into the non-overlap bias range category. A significant number of JTLs are inserted to achieve overlap of the bias current in subsequent blocks while maintaining satisfactory bias margins. For serially biased circuits with a large imbalance in bias current, the bias current requirement of each local ground plane is significantly different. An interface to balance these current requirements is therefore needed. The balancing interface supplies additional bias current to the underbiased circuits, eliminating the need to insert JTLs in those circuits with a non-overlap bias range. In heterogeneous circuits with a non-overlap bias range, the circuit blocks on isolated ground planes are arranged in an ascending order of required current. Additional current is supplied while recycling the current from the preceding ground plane, as depicted in Fig. 4(b).

IV. Bias Current Balancing Topology

As previously discussed, a bias balancing interface is needed to supply additional bias current in heterogeneous circuits with a non-overlap bias range. A resistive tree can be used to supply additional current directly from a DC current source to the injection node of each isolated block, as shown in Fig. 7. The resistors are not directly connected to the injection node of each isolated circuit block due to the difference between the bias bus voltage and ground voltage. A resistive tree is therefore adopted rather than directly supplying additional bias current from the global bias bus. The resistive tree supplies additional current to the individual blocks and establishes a new voltage across the subsequent resistor to maintain an accurate bias bus voltage and ground voltage at each injection node.

Current recycling in heterogeneous circuits is demonstrated using a one bit SFQ full adder with path balancing DFFs, as illustrated in Fig. 5, assuming the 10 KA/cm ^{2} MIT Lincoln Laboratory SFQ5ee fabrication process [1]. The full adder is demonstrated using both dummy JTL insertion and resistive tree bias balancing, as depicted, respectively, in Figs. 6 and 7. The DRP is placed between adjacent GPs, with the driver and receiver requiring, respectively, 425 μA and 175 μA. The ground plane that shares a common ground with the global ground does not require a DRP, as no voltage difference exists between the bias bus and the ground between the last isolated ground plane (GP3) and the global ground.

Dummy JTL insertion requires fewer number of JJs while maintaining balanced bias currents using the approach described

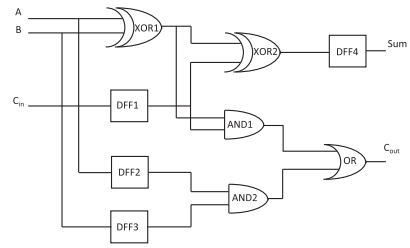

Fig. 5. One bit SFQ full adder.

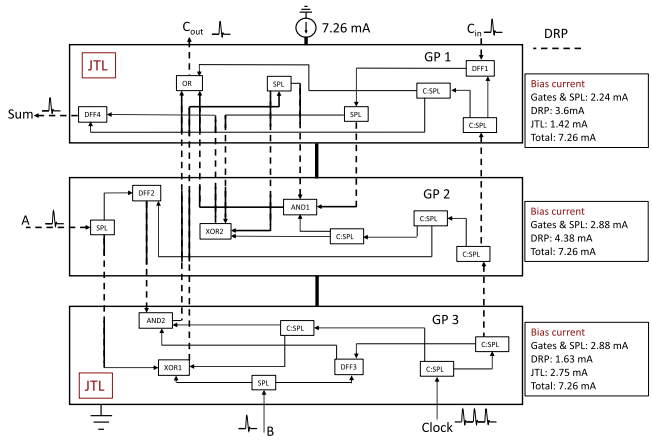

Fig. 6. Current recycling in one bit RSFQ full adder with inserted dummy JTL. 21 DRPs are used to transfer the signals. The cells are placed to prioritize the number of DRPs while balancing the bias current required by each GP (ground plane) [15].

in [15]. This approach uses 21 DRPs for a one bit full adder, as depicted in Fig. 6. After assigning several gates to a GP, the bias current for each GP is 2.24 mA, 2.88 mA, and 2.88 mA, respectively, for GP1, GP2, and GP3. The difference in bias current between the GPs after DRP insertion is 1.42 mA between GP1 and GP2 and 2.73 mA between GP2 and GP3. As previously discussed, these differences are due to the different bias current required by the driver and receiver. To address this issue, those JTLs with the bias requirement matching these differences are placed on the GP with lower bias requirements after DRP insertion. The total current supplied to the system is

$$T_{\text{current}} = I_l + I_d(n_{dL} + n_{dG}) + I_r(n_{rL} + n_{rG}), \quad (1)$$

where I_l is the current required by the last isolated ground plane, n_{dL} is the number of drivers on the last ground plane, n_{dG} is the number of drivers on the global ground, I_d is the bias current of the driver, n_{rL} is the number of receivers on the last ground plane, n_{rG} is the number of drivers on the global ground, and I_r is the bias current of the receiver.

The resistive tree uses eleven DRPs. Due to the choice of bias current, additional gates and splitters are placed on the last GP, which is connected to the global ground. This arrangement also contributes to the reduction in the number of DRPs, as no DRP is needed to transfer signals between the global ground plane and the last GP. As depicted in Fig. 7, nodes 1, 2, and

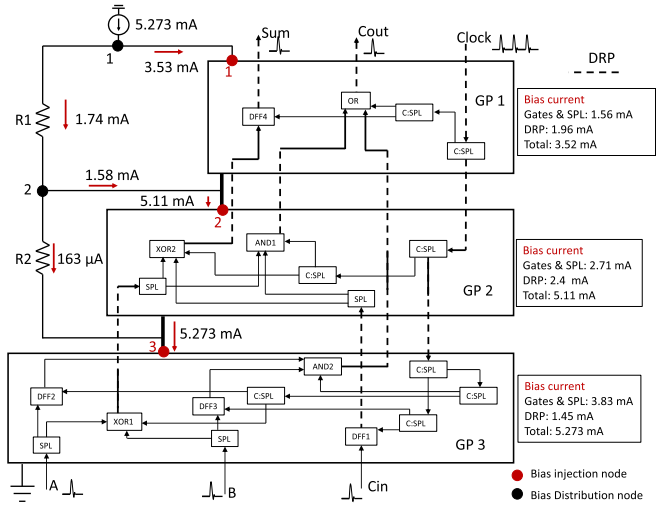

Fig. 7. Current recycling in one bit RSFQ full adder with resistive tree balancing to supply additional current to each isolated GP (ground plane), $R1 = 1.49\ \Omega$ and $R2 = 16\ \Omega$. The total number of DRPs is 11.

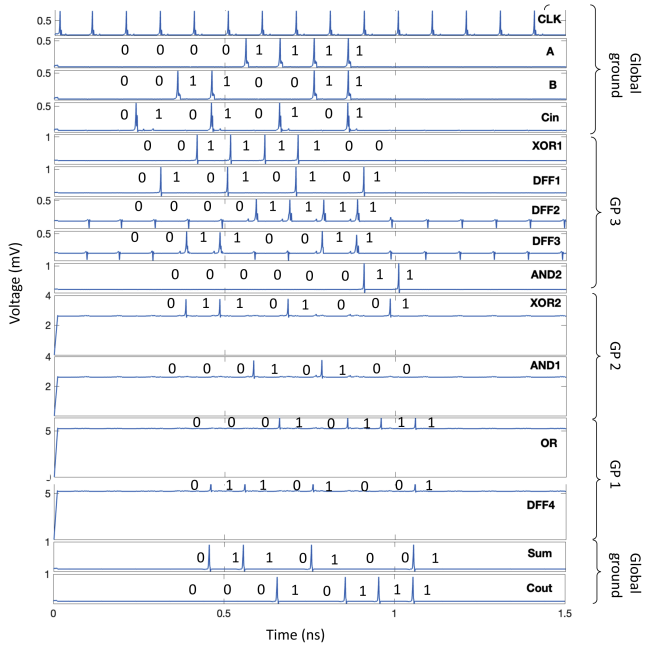

Fig. 8. Waveform characteristics of the heterogeneous circuits depicted in Fig. 7.

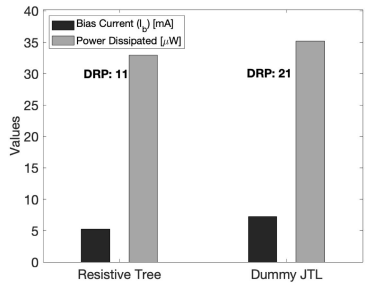

Fig. 9. Comparison between resistive tree and dummy JTL insertion topologies applied to a one bit full adder.

3 of both the bias distribution node and bias injection node, respectively, are 7.8 mV, 5.2 mV and 2.6 mV. All bias distribution lines maintain a voltage of 2.6 mV, the difference between the bias bus and the ground voltage. The size of the resistor is based on the difference in voltage across the bias distribution line rather than the individual node voltages. At bias distribution node 1, depicted in Fig. 7, the input DC bias current of 5.27 mA is split into two. Resistor $R1$ passes a bias current of 1.74 mA to node 2. The remaining 3.53 mA is passed to the first injection node to bias GP1. The current needed to bias the DRP is supplied along with current for the DRP. At bias distribution node 2, 1.74 mA is redistributed, 163 μA through resistor $R2$ to node 3 and 1.58 mA to injection node 2. The connection between the bias distribution node 2 and injection node 2 supplies the additional bias current needed for injection node two and also establishes the ground voltage for $R1$ and bias voltage for $R2$. A bias current of 1.53 mA is supplied to injection node 2, along with a bias current of 3.53 mA extracted from GP1 to bias the GP2 circuits. Resistor $R2$ passes the remaining 163 μA to bias GP3. The distribution nodes supply additional bias current to the injection nodes and establish a bus voltage for the next resistor, ensuring the bias bus voltage of each balancing resistor matches the bias bus voltage on each local ground plane.

A clock signal of 20 GHz is transferred from the global ground through the three isolated GPs. Signals A, B, and C_{in} are transferred from the global ground to GP3 without DRPs. The clock and other input signals are routed through a different circuit block on each GP, passing through the DRP between an adjacent GP. In this heterogeneous circuit, each circuit block consists of a different number of gates and splitters with different current requirements. The output of each gate on each isolated GP is shown in Fig. 8. The ground voltage of each GP and bias current of each gate are also illustrated. The current decreases from 8.1 mA, the combined bias current of the three islands without the overhead of the DRP bias current, to 5.27 mA, the input DC bias current. A 34.9% reduction in bias current is therefore achieved by serially biasing the heterogeneous circuit, as described in Fig. 7. Note that the per cent reduction depends upon the bias current of each ground plane. The operating margin of the heterogeneous circuit, a one bit full adder, is +31% . The serially biased cells do not operate correctly if the current is below the required bias current. Due to the resistive distribution of the tree, as the bias current increases, V_{bias} also increases. Note that the bias balancing technique can be extended to larger SFQ circuits with higher bias current requirements, consistent with the proposed resistive tree bias distribution guidelines.

The number of DRPs, bias current, and power dissipation for the two bias balancing topologies discussed in Section III are shown in Fig. 9. Although the resistive tree method dissipates 4.35 μW due to the bias balancing resistors, a significant reduction in DRPs is achieved as compared to inserting dummy JTLs which reduces the overall dissipated power. In a one bit full adder, the resistive tree method dissipates 6.42% less power

than the JTL insertion method with a 47.2% reduction in the number of DRPs. A 34.9% reduction in bias current is achieved as compared to a system without current recycling.

V. Conclusion

Current recycling can be achieved in heterogeneous circuits with unequal bias current requirements. The proposed balancing topology supplies additional current to the subsequent isolated ground plane to prevent larger blocks from being underbiased. Overlap and non-overlap bias current range categories are proposed to reduce the complexity of current recycling in heterogeneous RSFQ circuits. The isolated blocks are arranged in an ascending order of bias current for those circuits with a non-overlap bias range and in a descending order of bias current for those circuits with an overlap bias range. With heterogeneous current recycling, greater flexibility in current management is achieved. Current can be recycled across the entire system, resulting in a 34.9% reduction in current for a case study example. Future research will explore partitioning heterogeneous benchmark circuits with larger bias currents with the resistive tree bias balancing method, ensuring an ascending order of bias currents for each isolated ground plane and identifying other partitioning constraints.

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