Single Source SFQ Multiclock Generator Using Resistor–JTL Branches

Tejumadejesu Oluwadamilare, *Graduate Student Member, IEEE*, Shay Hacohen-Gourgy, and Eby G. Friedman, *Life Fellow, IEEE*

***Abstract*—Systems requiring multiple clock frequencies are becoming more common in digital superconductive electronics. In rapid single flux quantum circuits, precise frequencies are applied to different clock domains. A diverse variety of SFQ clock generators have been employed to produce a single frequency. A clock generator that uses a single voltage source to deliver multiple frequencies is presented here. The operating principle, performance, area, and power of the proposed SFQ multiclock generator are described. Previously published clock generators are limited to a fixed frequency or varied by changing the bias dc voltage—a parameter not typically changed in situ. In the proposed approach, the clock frequency is tunable by the SFQ logic circuit. In addition, a GALS system is presented to exemplify the practical application of the proposed multiclock generator.**

***Index Terms*—Rapid single flux quantum (RSFQ), SFQ ring oscillator, SFQ multiplexer, SFQ clock generator.**

I. Introduction

RAPID single flux quantum (RSFQ) logic is known for fast switching speeds and low power consumption, enabling system frequencies exceeding 100 GHz and energy consumption less than 10^{-19} joules per switching event [1], [2]. Clock signals in SFQ circuits are typically produced by converting a dc clock pulse into an SFQ clock pulse using a DC-to-SFQ converter [3]. As circuits scale, the need for on-chip clock generators arise. Several on-chip clock generators have been proposed for RSFQ integrated circuits [4], [5], [6]. Examples of on-chip clock generators are overbiased Josephson junctions (JJs), ring oscillators, and long JJs [4], [5]. A ring oscillator is a standard clock generator for SFQ clock signals; however, these clock generators require an external clock signal. This external signal is typically an input dc current which is converted into an SFQ clock signal through a DC-to-SFQ converter [2]. A programmable clock generator provides a specific number of pulses within a particular frequency range [6]. This feature reduces the power consumed by the clock source since a clock signal is only generated when needed. A programmable clock generator, however, cannot produce multiple stable frequencies with a single dc voltage. A four bit programmable clock generator is presented in [6] where an SFQ clock generator is programmed to produce a specific number of clock pulses (from 2^1 to 2^4) with an oscillation frequency ranging between 6.2 and 18.8 GHz with -1.4% to +20% dc bias margins [6].

In this article, a clock generator providing precise control of multiple SFQ clock frequencies is presented. This multiclock generator is used in systems where multiple frequencies are required. One important example is systems with multiclock domains as encountered in globally asynchronous locally synchronous (GALS) systems. The proposed clock generator selects two or three frequencies without requiring more than one input dc voltage. This approach reduces both physical area and power dissipation. The circuit can be expanded to accommodate additional frequencies while only requiring a single dc input voltage. The only additional requirement is a large multiplexer to select these additional frequencies. To illustrate practical use of this technique, the proposed multiclock generator is applied to a GALS data transfer circuit. This example demonstrates how multiple frequencies can be generated and synchronized from a single dc voltage source, enabling robust cross-domain communication in large scale SFQ systems.

This article is organized as follows: Several types of SFQ clock generators are reviewed in Section II. The operating principle of the proposed SFQ multiclock generator is described in Section III. The application of the proposed clock generator to a GALS system is discussed in Section IV. The proposed clock generator is compared to existing SFQ generators in Section V. Some conclusions are offered in Section VI.

II. Existing SFQ Clock Generators

Most RSFQ logic gates are clocked [2]. The importance of a clock generator in SFQ systems therefore cannot be overemphasized. To produce SFQ clock signals, different clock generators can be used. Each SFQ pulse exhibits an amplitude of ≈ 1 mV with a width of ≈ 2 ps. The relationship between the voltage and frequency of an SFQ pulse is

$$V = \Phi_0 * f \tag{1}$$

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Tejumadejesu Oluwadamilare and Eby G. Friedman are with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY 14627 USA (e-mail: toluwada@ur.rochester.edu; friedman@ece.rochester.edu).

Shay Hacohen-Gourgy is with the Department of Physics, Technion-Israel Institute of Technology, Haifa 3200003, Israel (e-mail: shayhh@physics.technion.ac.il).

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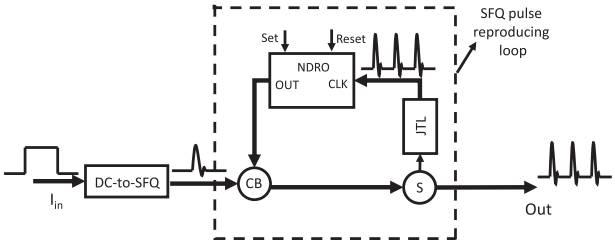

Fig. 1. SFQ-based ring oscillator, splitter (S), and confluence buffer (CB). The output of the DC-to-SFQ converter directly connects to the confluence buffer, and the output of the buffer connects to the splitter. A single JTL is used in the reproducing loop to reinforce the signal.

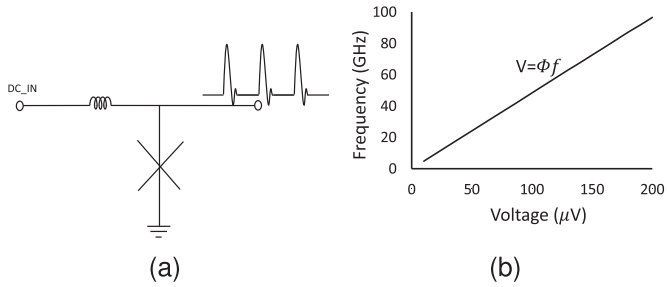

Fig. 2. SFQ clock generator, (a) circuit topology, and (b) frequency as a function of input dc voltage.

where Φ is the flux constant, and $\Phi = h/2e \approx 2.07$ mV $*$ ps or 2.07 webers [1]. The performance characteristics described in this article are based on the 10 KA/cm^2 MIT Lincoln Laboratory SFQ5ee fabrication process [7]. A ring oscillator, a standard type of clock generator, is reviewed in Section II-A. A frequency synchronizer, another type of clock generator, is discussed in Section II-B.

A. SFQ Ring Oscillator

An SFQ ring oscillator is composed of several cells, including a confluence buffer, splitters, Josephson transmission lines (JTLs), a switch or nondestructive readout (NDRO) flip flop, and a DC-to-SFQ converter [6]. The ring oscillator uses an external dc current pulse to drive a DC-to-SFQ converter. This converter transforms a dc current into an SFQ pulse. The SFQ pulse enters the confluence buffer and is passed through a JTL to a splitter. The JTL transfers and amplifies the SFQ pulse over short distances [8]. A two junction JTL (2J-JTL) introduces a delay of 2 to 5 ps depending upon the critical current of the JJs. The splitter duplicates an SFQ pulse [9], sending one pulse to the output of the ring oscillator and another pulse to the input of the NDRO. The clock pulse is generated within the SFQ reproducing loop (see Fig. 1), where the periodic pulses are produced. The set signals initialize the reproducing loop by activating the NDRO which passes the SFQ pulse received from the splitter to the input clock port of the NDRO. The pulse at the NDRO output is passed through the reproducing loop and returned to the clock input of the NDRO upon arrival of the subsequent clock pulse. The reproducing loop produces a clock signal at both the NDRO clock input and the output of the ring oscillator. Clock signal generation continues until a reset signal is received. In [1], an NDRO, confluence buffer, splitter, and JTL each contribute a time delay of, respectively, 11 ps, 8 ps, 3 ps, and 5 ps. Collectively, these delays produce a 27 ps clock period (37 GHz) ring oscillator, as illustrated in Fig. 1 for a standard niobium technology [1]. A lower frequency can be achieved using a toggle flip flop to divide the frequency until the target frequency is achieved. A ring oscillator is not effective in generating multiple frequencies.

B. Frequency Synchronized SFQ Oscillators

Frequency synchronization of SFQ oscillators offers an alternative method for generating a high-frequency clock signal without requiring external synchronization circuitry. The architecture typically consists of multiple SFQ oscillators, each oscillator based on a circular JTL loop composed of JJs, shunt resistors, and loop inductances [5]. These oscillators operate in pairs and are jointly biased by a constant current source. The synchronization is caused by the difference in the average output voltage across each oscillator redistributing the bias current. When an SFQ oscillator operates at a frequency f, an average voltage of $f\Phi_0$ across the junctions is produced, where Φ_0 is a quantum of magnetic flux.

Each oscillator may initially oscillate at a distinct frequency due to variations in the loop inductance. However, upon injection of a startup bias current I_{in} to both oscillators, any voltage mismatch between the oscillators redistributes the bias current, driving the oscillators to a common frequency. In simulations, synchronization is achieved with an initial frequency difference exceeding 50 GHz. Experimental results using niobium (Nb) technology confirm that the oscillators converge to a common frequency [5] depending upon the bias conditions and loop inductance. This method enables stable SFQ clock generation with zero static power dissipation, as no resistive biasing is required. Although primarily demonstrated for pairs of oscillators, the approach is extendable to multioscillator systems. A limitation is that the synchronized frequency is not independently tunable for each oscillator; rather, the frequency depends upon the distribution of the shared bias current and inductances.

III. Operating Principle of SFQ Multiclock Generator

The operation of the multiclock generator is discussed in this section. The effect of the dc voltage on frequency is described in Section III-A. The effect of inserting a small resistance on the generated frequency is discussed in Section III-B. The operation of the clock damping circuit is explored in Section III-C.

A. Voltage Controlled SFQ Clock Generator

A continuous stream of pulses is generated when a constant dc voltage flows through a JJ without a DC-to-SFQ converter, as depicted in Fig. 2(a). The frequency of the clock pulses depends upon the input voltage, as expressed by (1) and illustrated in Fig. 2(b), with an input voltage range of 10 to 207 μV producing a clock frequency ranging from 5 to 100 GHz.

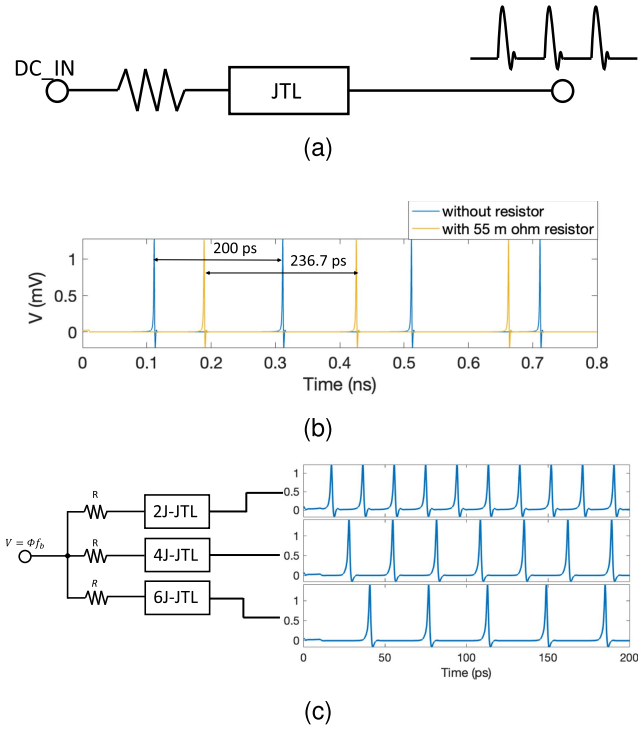

Fig. 3. Adjustable SFQ clock generator, (a) circuit topology, (b) clock pulses based on frequency adjusting resistor with the same input voltage, and (c) variation in frequency based on size of JTL.

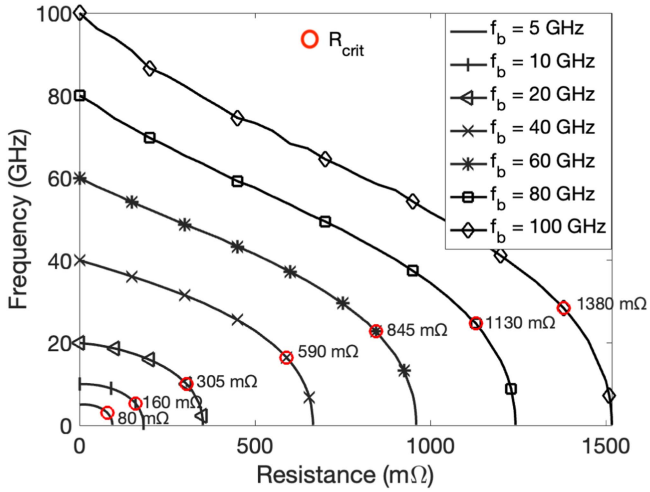

Fig. 4. Relationship between the resistance and frequency of an adjustable SFQ clock generator for several base frequencies f_b (the frequency produced without a resistor at the input of the JTL input). The marked R_{crit} denotes the critical resistance that defines the threshold beyond which the circuit becomes increasingly sensitive to parameter variations.

B. Adjustable Clock Generator

To produce a change in the clock period without altering the input voltage, a small resistor is inserted between the voltage source and the JTL, as shown in Fig. 3. As depicted in Fig. 3(a), this resistor degrades the effective voltage across the overbiased JJ, thereby reducing the oscillation frequency. For small resistances, this reduction is gradual and predictable. As the resistance increases, however, the circuit enters a hypersensitive region, where even minute variations in resistance lead to disproportionately large changes in oscillating frequency.

A base frequency f_b is established by applying a constant dc voltage V to a JTL without any resistor, where the frequency is governed by the Josephson relation $V = \Phi_0 \cdot f$. A resistor R degrades the effective voltage, increasing the clock period. This increase is initially linear and stable. But beyond a certain threshold resistance, the circuit becomes highly sensitive. This threshold is described here as the *critical resistance* R_{crit}, which represents the maximum resistance for a given frequency f_b. Beyond this critical resistance, fabrication induced variations as small as ± 0.1 mΩ can cause abrupt frequency shifts exceeding 10 MHz, compromising clock precision and timing margins. As the resistance increases, the voltage across the JTL drops. Since $f = V/\Phi_0$, the frequency also drops. This drop in voltage is initially linear since the current is sufficient to sustain oscillations. However, beyond a threshold, the current through the JJs is no longer sufficient to sustain SFQ switching. A small change in the resistance significantly lowers the junction voltage below the switching threshold, resulting in large changes in the frequency. The frequency with respect to resistance may be qualitatively approximated by

$$f(R) \approx \frac{V_{\text{eff}}(R)}{\Phi_0}, \quad \text{where} \quad V_{\text{eff}}(R) = V_{\text{DC}} - IR \tag{2}$$

with I denoting the current through the resistor before the JTL. As $R \to R_{\text{crit}}$, the derivative df/dR becomes large, indicating increasing sensitivity to fluctuations in the resistance. Specifically, R_{crit} is the lowest resistance for which the magnitude of the derivative of the frequency with respect to the derivative of the resistance exceeds a threshold

$$\left| \frac{df}{dR} \cdot \Delta R \right| \geq 0.01\ \text{GHz}, \quad \text{with } \Delta R = 0.1\ \text{m}\Omega. \tag{3}$$

The effect of the resistance on the frequency for several base frequencies or input voltages ($= f_b \cdot \Phi_0$) is illustrated in Fig. 4. The circular markers indicate R_{crit}, depicting the onset of the rapid degradation in frequency. For instance, at $f_b = 5$ GHz (where $V \approx 10.34\,\mu$V), a 55 mΩ resistor increases the clock period by 37 ps, as shown in Fig. 3(b). As the resistance approaches $R_{\text{crit}} = 80$ mΩ, a rapid degradation in frequency occurs due to the reduction in voltage at the input of the JTL. Beyond this value of resistance, small increases in resistance significantly lower the voltage below the switching threshold required for SFQ pulse generation, resulting in a disproportionately large drop in frequency. For higher base frequencies, R_{crit} increases, allowing a broader tuning range. The dependence of the generated base frequency f_b and other generated frequencies f_{Tn} on the dc input voltage for several values of series resistance is depicted in Fig. 5. The curves illustrate the expected linear scaling of frequency with dc input voltage with the reduction in slope in proportion to the series resistance due to the voltage drop expressed in (2).

The number of junctions in the JTL also affects the output frequency for a given input voltage and resistance. As depicted

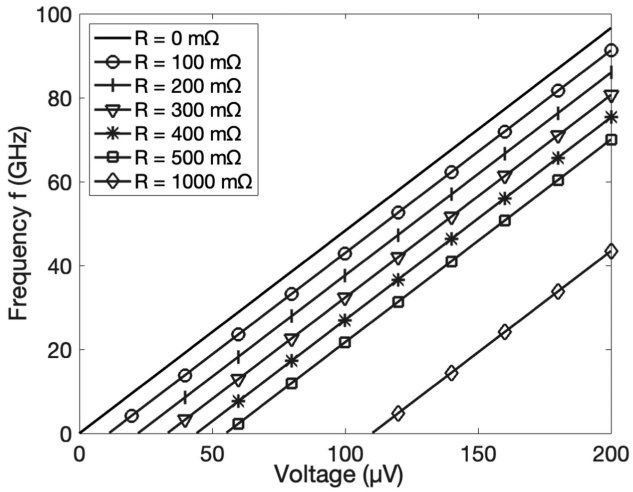

Fig. 5. Relationship between input voltage and the frequency of an adjustable SFQ clock generator for several values of resistance. The curve for $R = 0$ corresponds to the base frequency f_b, while the curves for $R > 0$ correspond to the other generated frequencies f_{Tn}.

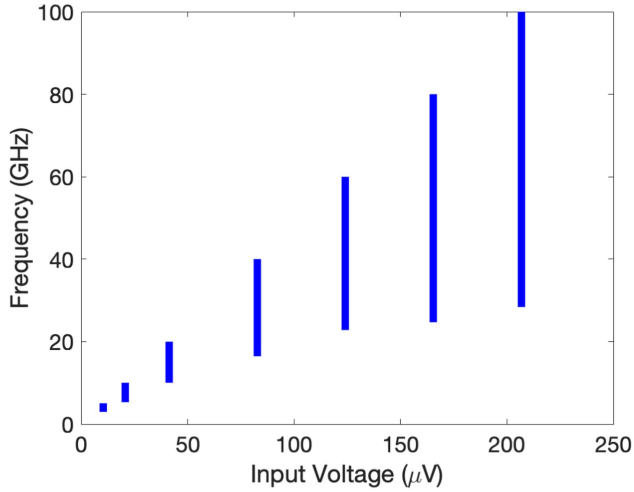

Fig. 6. Operational frequency range with input voltage $V = \Phi_0 \cdot f_b$.

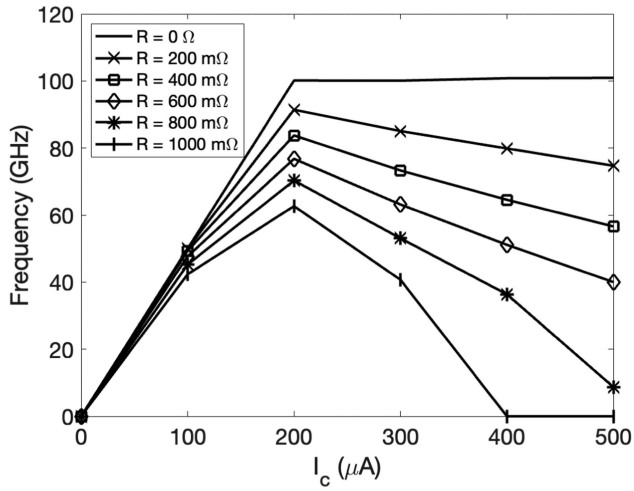

Fig. 7. Relationship between the critical current of the JJs within a JTL and the frequency of an adjustable SFQ clock generator for several values of resistance. The curve for $R = 0$ corresponds to the base frequency f_b, while the curves for $R > 0$ correspond to the other generated frequencies f_{Tn}.

in Fig. 3(c), the resulting periods are shown for two JJ 2J-JTL, 4J-JTL, and 6J-JTL at $f_b = 50$ GHz ($V \approx 103.39\,\mu$V) and $R = 600$ mΩ. The corresponding periods are, respectively, 21 ps, 26 ps, and 36 ps. Additional junctions increase the voltage drop across each junction, changing the frequency despite a smaller resistance. As additional junctions are added to the JTL, the input voltage is distributed across a greater number of JJs. This redistribution reduces the voltage per junction, resulting in a slower switching speed and a corresponding decrease in the oscillation frequency, as observed in Fig. 3(c). This degradation in frequency with increasing number of junctions only occurs when a resistor is present at the JTL input. The resistor introduces a voltage drop proportional to the current drawn by the JTL. As the number of junctions increases, the transient current also increases, reducing the effective voltage delivered to the JTL and switching the junction more slowly.

At higher base frequencies, a larger resistance is required to achieve a significant change in frequency. The difference between f_b and the minimum tunable frequency f_Tmin increases with f_b. As depicted in Fig. 6, f_b sets the upper bound for the maximum achievable frequency while the frequency associated with R_{crit} sets the lower bound. As shown in Fig. 4, at $f_b = 60$ GHz, $f_{T\min}$ is 22 GHz, requiring up to 850 mΩ resistance. Both the maximum frequency and usable tuning range scale with the base frequency. The effect of the critical current I_c of the JJs within a JTL on the generated frequency is shown in Fig. 7. For a fixed dc input voltage, the frequency increases with increasing I_c until the frequency saturates, beyond which further increases in I_c reduce the oscillation frequency in those branches with a large series resistance since the voltage across the JTL drops below the switching threshold.

As previously mentioned, the frequency can be adjusted without altering the input voltage. By dividing the voltage into three branches, multiple frequencies close to the base frequency can be generated. The input voltage can directly feed a 2J-JTL to generate the base frequency, while the voltage across resistors R_1 and R_2 produce, respectively, frequencies f_{T1} and f_{T2}, as shown in Fig. 8. This approach enables flexible multifrequency generation without requiring additional voltage sources.

Although this analysis focuses on deterministic circuit parameters, thermal fluctuations at 4.2 K can induce timing jitter and small deviations in the junction switching threshold for clock periods approaching 1 ps. For the technology node considered ($J_c = 10\,\mathrm{kA/cm^2}$), these effects are small relative to the deterministic variations caused by the input voltage, I_c, and R [10]. These effects may further limit the precision at higher operating temperatures and/or subpicosecond clock periods.

C. Clock Damping Circuits

In RSFQ circuits, the oscillation frequency of a clock generator is sensitive to both the size of the damping resistor and the

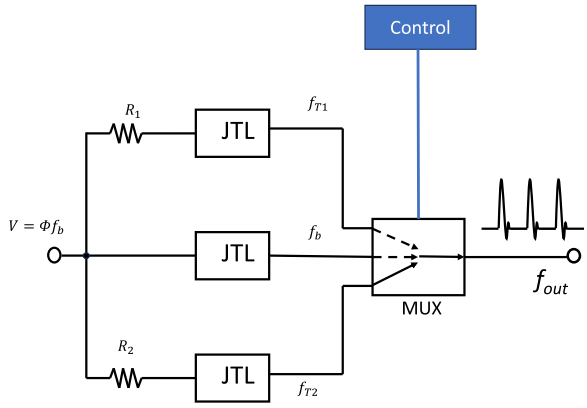

Fig. 8. SFQ-based multiclock generator with multiplexer.

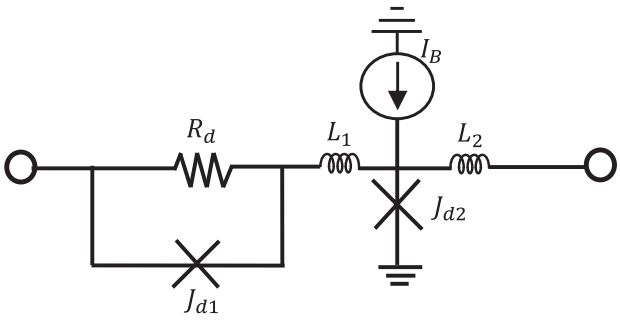

Fig. 9. Clock damping circuit, $J_{d1} = 125\ \mu$A, $J_{d2} = 250\ \mu$A, $R_d = 7\ \Omega$, and $I_b = 175\ \mu$A.

number of JJs along the signal path. As the clock signals propagate through the splitters and gates, each additional junction adds delay and also increases the parasitic inductance and capacitance along the path. These effects lead to timing distortion, pulse broadening, and an increase in the clock period (a reduction in the output frequency).

To address these issues and maintain timing integrity, each output branch of the proposed multiclock generator is terminated with a *clock damping circuit*. This circuit consists of a resistor R_d connected in parallel with a JJ J_{d1}, followed by another JJ J_{d2}, as depicted in Fig. 9. The $R_d \parallel J_{d1}$ pair serves as a damping element that suppresses reflections caused by the inductor and the degrading resistor. The junction J_{d2} ensures delivery of the SFQ pulse to subsequent logic stages operating at the target frequency.

The damping circuit performs two key functions:

1) *Damping and Isolation:* The resistor R_d acts as a low impedance path for the high-frequency clock signal, absorbing excess energy and preventing signal reflections from propagating back into the clock distribution network. The JJ J_{d1} allows normal propagation of the SFQ pulse while limiting damping to only when active switching is required.
2) *Pulse Stabilization:* The output junction J_{d2} buffers the signal and maintains the timing and shape of the SFQ pulse, reducing delay uncertainty introduced by the downstream fanout.

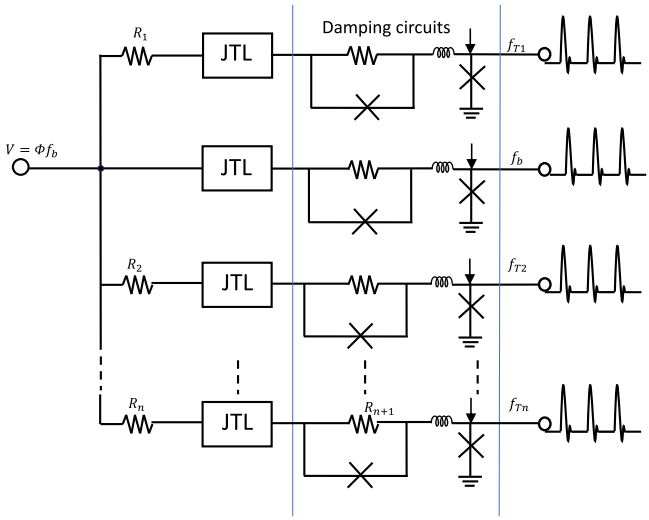

Fig. 10. SFQ-based multiclock generator with damping circuits.

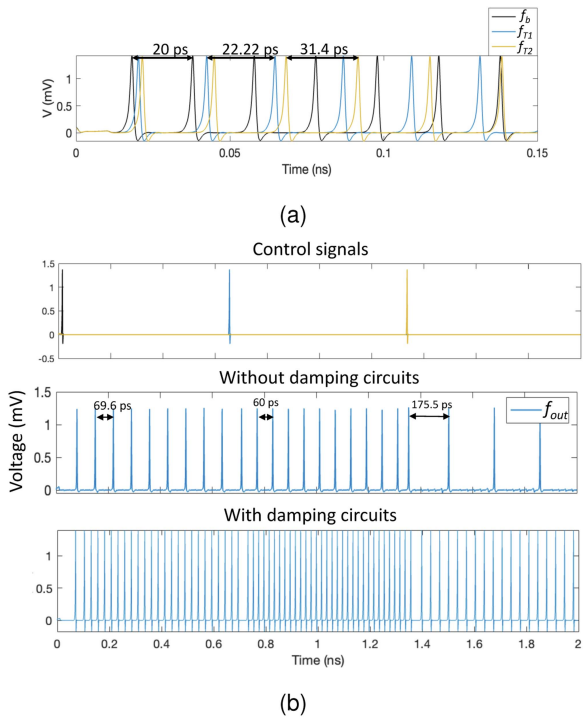

Fig. 11. SFQ clock pulses generated by a multiclock generator, (a) before the multiplexer stage, and (b) after the multiplexer stage with and without the damping circuit

To demonstrate the effects of the damping circuits, a circuit is evaluated with a 103.4 μV dc bias, producing a base frequency of approximately 50 GHz. The multiclock generator drives three branches with frequencies f_{T1}, f_b, and f_{T2}, which feed into a 3:1 multiplexer [11], as shown in Fig. 8. To include clock damping, circuits are connected as shown in Fig. 10 before sending the generated clock signal through a multiplexer. The small resistors R_1 and R_2 are set, respectively, to 100 mΩ and 150 mΩ, resulting in a clock period of 22.2 ps (45 GHz) and 31.2 ps (31.9 GHz) at, respectively, f_{T1} and f_{T2} [see Fig. 11(a)]. The damping resistor

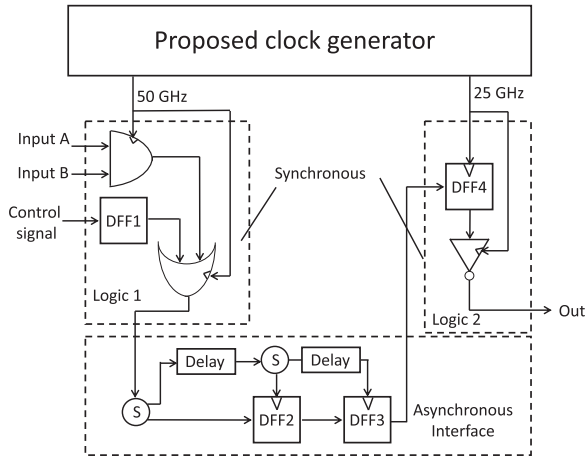

Fig. 12. Two clock domain GALS SFQ system using the proposed multiclock generator.

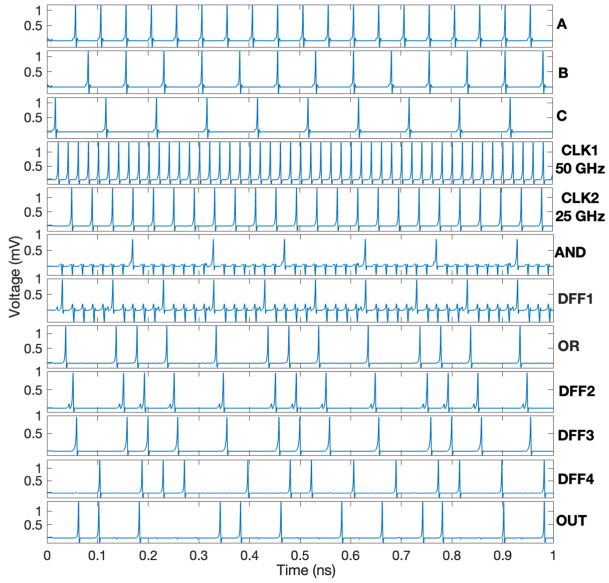

Fig. 13. Output waveform of each gate shown in Fig. 12.

and critical current of J_{d1} for each branch are, respectively, 7 Ω and 125 μA.

The circuit is evaluated with and without damping circuits, as depicted in Fig. 11. Without the damping circuits, significant degradation in the clock frequency occurs after the multiplexer. The output period increases to 69.6 ps, 60.0 ps, and 175.5 ps for, respectively, f_{T1}, f_b, and f_{T2}, corresponding to a frequency of, respectively, 14.4 GHz, 16.0 GHz, and 5.7 GHz [see Fig. 11(b)]. When the damping circuits are included, the output frequencies remain the same as the premultiplexer frequencies, confirming the effectiveness of the damping circuits in preserving timing integrity, as depicted in Fig. 11(b). The analysis is based on the WRCAD Verilog model of a JJ [12]. The damping circuit enables robust and scalable multifrequency clock distribution from a single voltage source while maintaining waveform integrity across a variety of fanout conditions.

IV. Example of GALS Data Transfer

To demonstrate the effectiveness of the proposed multifrequency SFQ clock generator, a GALS data transfer circuit is considered. As depicted in Fig. 12, the system is comprised of two clock domains operating at different frequencies and connected via an asynchronous interface.

The circuit consists of the following components:

1) *Logic 1:* A 50 GHz domain containing an AND gate that generates data pulses.
2) *Logic 2*: A 25 GHz domain that receives and latches the data.
3) *Asynchronous interface:* A two stage synchronizer using self-timed SFQ D flip flops (DFFs) for safe cross domain signal transfer.

A third input signal C is optionally merged with the AND gate output using a two input OR gate to control when data transmission is initiated. Signal C uses a path balancing DFF1 to preserve the data signal [13], [14], [15]. The 50 and 25 GHz clock signals are both supplied by the proposed multiclock generator.

In Logic 1, a two input OR gate merges the output of the AND gate with an optional control signal to trigger data transmission. The resulting pulse is stored in the first DFF of the asynchronous interface, DFF2, which is clocked by the delayed output from the OR gate [16]. A second DFF, also clocked by the delayed output, transfers the signal into the slower Logic 2 domain. A third DFF in Logic 2 captures the signal and drives an inverter to provide a buffered output. The SFQ pulses at the output of each gate are shown in Fig. 13.

Successful operation of this GALS data transfer circuit demonstrates the capability of the proposed multiclock generator to synchronize independent SFQ clock domains. By supplying multiple synchronized SFQ pulse trains at different frequencies, the generator enables modular, frequency diverse operation without the need for additional clock trees or global oscillators.

This evaluation demonstrates the feasibility of scalable multidomain SFQ systems, underscoring the potential for more flexible and energy efficient superconductive digital systems. The GALS example represents a functional block commonly used in larger SFQ systems. This example also validates the correct functionality of the proposed generator and highlights the practicality of multidomain clocking in superconductive digital systems. Applications such as multicore SFQ processors, asynchronous memory interfaces, and interconnect routers rely on cross domain synchronization.

Beyond GALS data transfer, the proposed multiclock generator can be combined with a multiplexer [11] to deliver selectable clock frequencies for a variety of practical applications. For example, during circuit testing, different clock frequencies can be supplied to the system under test by selecting from multiple generator outputs with a control signal. This capability enables frequency dependent characterization without modifying the circuit topology. In addition, in dual clock systems such as those used in path balancing techniques [17], the multiclock generator can dynamically provide both fast and slow clock signals from

TABLE I
COMPARISON OF CLOCK GENERATION TECHNIQUES

Feature	Ring Oscillator	Frequency Synchronizer	Proposed Multi-Clock Generator
Number of JJs per frequency	25	16 (two pairs)	4
Static power dissipation	High	Zero	Medium
External sources	Yes	No	No
Frequency range	30 to 40 GHz	Up to 100 GHz	Up to 100 GHz
Number of frequencies per clock generator	Single	Single	Multiple
Area and scalability	Medium	High	Low
Power consumption	1.35 μW	0.31 μW	0.70 μW
Bias current consumption	1.7 mA	1.2 mA	0.4 mA

a single source. This capability eliminates the need for multiple discrete clock sources and improves timing alignment. The setup is also appropriate for FIFO synchronization between distinct clock domains, where data are written and read at different rates by separate functional blocks. The ability to route multiple clocks from a single compact source enhances design flexibility, simplifies routing, and dissipates less power in multifrequency SFQ systems.

V. COMPARISON OF ON-CHIP SFQ CLOCK GENERATORS

As superconductive systems scale in complexity, selecting an efficient and scalable on-chip clock generator becomes critical. Three SFQ clock generation techniques are compared: ring oscillator, frequency synchronized oscillator, and proposed multiclock generator (see Table I). The proposed system exhibits improvements in scalability, efficiency, and functionality over existing clock generators.

In terms of circuit complexity, the proposed multiclock generator requires only four JJs per frequency, significantly fewer than the 25 JJs required by a typical ring oscillator and the 16 JJs (organized as two pairs of eight JJs) in a frequency synchronizer. Moreover, unlike a ring oscillator, which requires external DC-to-SFQ conversion to initiate operation and suffers from high static power dissipation, the proposed generator operates without an external dc waveform or synchronization circuitry and consumes moderate static power. The frequency synchronizer achieves zero static power dissipation by eliminating the on-chip bias resistors. This advantage, however, increases circuit complexity and physical area due to the large number of passive inductors required to redistribute the bias current.

Functionally, the proposed architecture supports the simultaneous generation of multiple frequencies from a single circuit, in contrast to the ring oscillator and frequency synchronizer, which are inherently single frequency generators. The range of output frequency of the proposed multiclock generator extends to 100 GHz, matching or exceeding the other techniques. From a systems integration perspective, the multiclock generator not only reduces the number of components but also simplifies routing and clock domain management.

A notable reduction in dynamic power as compared to a ring oscillator is achieved in the multiclock generator primarily due to the shunt resistors. The estimated dynamic power for the ring oscillator is 1.35 μW and the frequency synchronizer is 0.31 μW while the multiclock generator consumes 0.7 μW, based on the energy dissipation model $E_D \approx I_c\Phi_0$ per GHz [2]. This efficiency is particularly beneficial for energy constrained or heat load sensitive cryogenic systems, where power savings translate to reduced cooling load.

VI. CONCLUSION

A scalable and energy efficient multiclock generator for RSFQ systems is presented. Unlike conventional SFQ clock generators, such as ring oscillators and frequency synchronizers, which are limited to a single output frequency, the proposed circuit topology can simultaneously generate multiple stable clock frequencies from a single dc voltage source. This capability is achieved through controlled tuning of the resistances and the use of damping circuits to maintain pulse integrity under different fanout conditions. The proposed multiclock generator significantly reduces circuit complexity and bias current as compared to traditional solutions. The compact architecture, low junction count, and integrated multiplexer output selection provide an efficient solution for modern superconductive systems that demand frequency flexibility. Examples of these systems include GALS architectures, path balancing circuits, FIFO synchronization, multiple clock domains, and functional testing. The example of a GALS system highlights the potential of the proposed clock generator for system-level integration of SFQ circuits.

The proposed multiclock generator assumes a low noise dc voltage input. These voltages can be generated using cryogenic bandgap reference sources or filtered voltage dividers. Ensuring low ripple and thermal noise is critical, as fluctuations in the voltage directly translate to jitter in the clock frequency. Future research will evaluate low noise voltage regulation circuits specifically designed for superconductive applications. Additional topics include achieving finer frequency granularity and dynamic programmability targeting sub-GHz resolution without significantly increasing the dissipated power or circuit complexity.

REFERENCES

[1] K. Likharev and V. Semenov, "RSFQ logic/memory family: A new Josephson-junction technology for sub-Terahertz-Clock frequency digital systems," *IEEE Trans. Appl. Supercond.*, vol. 1, no. 1, pp. 3–28, Mar. 1991.
[2] G. Krylov, T. Jabbari, and E. G. Friedman, *Single Flux Quantum Integrated Circuit Design*, 2nd Ed. Berlin, Germany: Springer, 2024.
[3] O. Mukhanov, "RSFQ 1024-bit shift register for acquisition memory," *IEEE Trans. Appl. Supercond.*, vol. 3, no. 4, pp. 3102–3113, Dec. 1993.
[4] C. Mancini and M. Bocko, "Short-term frequency stability of RSFQ ring oscillators," *IEEE Trans. Appl. Supercond.*, vol. 9, no. 2, pp. 3545–3548, Jun. 1999.
[5] Y. Yamanashi, R. Kinoshita, and N. Yoshikawa, "Frequency synchronization of single flux quantum oscillators," *Supercond. Sci. Technol.*, vol. 34, no. 10, Sep. 2021, Art. no. 105004.

[6] M. Ito et al., "Design and implementation of SFQ programmable clock generators," *Physica C, Supercond.*, vol. 412-414, pp. 1550–1554, Feb. 2004.
[7] MIT Lincoln Laboratory, Superconducting Electronics, MIT Lincoln Laboratory, 2014, [Online]. Available: https://www.ll.mit.edu/r-d/projects/superconducting-electronics
[8] T. Jabbari, G. Krylov, S. Whiteley, E. Mlinar, J. Kawa, and E. G. Friedman, "Interconnect routing for large-scale RSFQ circuits," *IEEE Trans. Appl. Supercond.*, vol. 29, no. 5, Aug. 2019, Art. no. 1102805.
[9] T. Jabbari, G. Krylov, J. Kawa, and E. G. Friedman, "Splitter trees in single flux quantum circuits," *IEEE Trans. Appl. Supercond.*, vol. 31, no. 5, Aug. 2021, Art. no. 1302606.
[10] K. K. Likharev, *Dynamics of Josphson Junctions and Circuits*, New York, NY, USA: Taylor & Francis Group, 1986.
[11] T. Oluwadamilare and E. G. Friedman, "Multi-input SFQ multiplexers," *IEEE Trans. Appl. Supercond.*, vol. 35, no. 5, Aug. 2025, Art. no. 1301206.
[12] S. R. Whiteley, "PWL-RCSJ Josephson junction model," 2012. [Online]. Available: http://www.wrcad.com/ftp/pub/jj.va
[13] R. Yang et al., "A local optimization method for single flux quantum logic circuits design utilizing synchronizer IPs," *IEEE Trans. Appl. Supercond.*, vol. 33, no. 3, Apr. 2023, Art. no. 1301308.
[14] G. Krylov and E. G. Friedman, "Wave pipelining in DSFQ circuits," *IEEE Trans. Appl. Supercond.*, vol. 32, no. 8, Nov. 2022, Art. no. 1301560.
[15] G. Pasandi and M. Pedram, "PBMap: A path balancing technology mapping algorithm for single flux quantum logic circuits," *IEEE Trans. Appl. Supercond.*, vol. 29, no. 4, Jun. 2019, Art. no. 1300114.
[16] Y. Yamanashi, T. Fujisawa, Z. Li, and N. Yoshikawa, "Asynchronous single flux quantum logic gates using self-clocking," *IEEE Trans. Appl. Supercond.*, vol. 33, no. 5, Aug. 2023, Art. no. 1301705.
[17] G. Pasandi and M. Pedram, "An efficient pipelined architecture for superconducting single flux quantum logic circuits utilizing dual clocks," *IEEE Trans. Appl. Supercond.*, vol. 30, no. 2, Mar. 2020, Art. no. 1300412.