

An *RLC* Interconnect Model Based on Fourier Analysis

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Abstract—Based on a Fourier series analysis, an analytic interconnect model is presented which is suitable for periodic signals, such as a clock signal. In this model, the far-end time-domain waveform is approximated by the summation of several sinusoids. Closed-form solutions of the 50% delay and overshoots/undershoots are provided when the fifth and higher order harmonics are ignored. Good accuracy is observed between the model and SPICE simulations. The model is applied to resistance–capacitance–inductance interconnect trees and the computational complexity of the model is linear with the size of the tree and the model order. The tree model is shown to be an effective method to analyze clock distribution networks. The single interconnect model is also extended to coupled multi-interconnect systems to analyze crosstalk noise and a general waveform solution is obtained. It is noted that in addition to the transition time, the period of the aggressor signal also has a significant effect on the crosstalk noise.

Index Terms—Clock tree synthesis, Fourier analysis, interconnect, noise analysis, resistance–capacitance–inductance (RLC), very large scale integration (VLSI).

I. INTRODUCTION

IN DEEP submicrometer integrated circuits, interconnect delay dominates gate delay. Furthermore, wire inductance can no longer be ignored, due to higher signal frequencies and longer wire lengths [1]. Accurate and efficient resistance–capacitance–inductance (*RLC*) interconnect models are, therefore, critical in the design of high-performance integrated circuits.

Based on modified Bessel functions, expressions characterizing the transient response of an *RLC* interconnect have been rigorously developed in [2] and [3]. These results, however, are highly complicated and are not suitable for an exploratory design process. In order to produce a more efficient solution, the transfer function of the interconnect is truncated and approximated with a few dominant poles, for example, one or two poles in [4] and [5], and four poles in [6]. Four pole expressions are

highly accurate, however, no closed-form solution has been developed in [6]. In all of these models, a step or ramp input is assumed and no initial conditions are considered. For a periodic signal, however, the initial conditions can have a significant effect on the output waveform.

The performance of a synchronous circuit is heavily dependent on the design of a clock distribution network. *RLC* interconnect trees are common structures in clock networks. An accurate model of an *RLC* interconnect tree, therefore, is critical in modern digital circuit design. In [4] and [7], second-order models are used to analyze *RLC* trees. The accuracy of these models, however, is limited. In order to obtain a more accurate result, model order-reduction techniques can be adopted at the expense of additional computational complexity, such as asymptotic waveform evaluation (AWE) [8].

With the scaling of semiconductor technologies, interconnect crosstalk has become another important issue. Crosstalk can be caused by either (or both) capacitive coupling and inductive coupling. Capacitive coupling is a short-range effect, where typically only adjacent lines need be considered. On the contrary, inductive coupling is a long range effect and is significantly more difficult to analyze. For multiconductor transmission lines, modal analysis [9], [10] is a widely used decoupling method. This decoupling method is extended to drivers and loads in [11] and [12] for two and more interconnects. The extensions, however, are only valid for identical lines with identical drivers and loads. Furthermore, a homogeneous dielectric environment is assumed in [12].

In this paper, a new interconnect model is presented. The model is based on a Fourier series analysis of a periodic input signal. No approximation is made to the transfer function of the interconnect. The far-end response is approximated by the summation of several sinusoids. Since the solution is the steady-state response to a periodic signal, the initial conditions are considered. The model is verified by SPICE simulations and successfully extended to *RLC* trees and multiple transmission lines. The paper is organized as follows. In Section II, the Fourier series-based interconnect model for a single line is described. In Section III, the model is applied to *RLC* trees, and a tree model with linear computational complexity is obtained. Combined with the modal analysis, the proposed model is extended to multiple interconnect lines in Section IV to analyze crosstalk noise. Finally, some conclusions are offered in Section V.

II. SINGLE INTERCONNECT MODEL

The exact transfer function of a widely used interconnect model is described in Section II-A, and compared with the transfer functions of some approximate models. A Fourier

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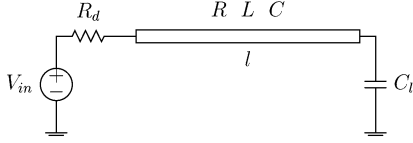


Fig. 1. Equivalent circuit model of a distributed *RLC* interconnect.

series analysis of a typical on-chip signal is presented in Section II-B. Based on this analysis, an expression for the time-domain response at the far end of an interconnect is presented in Section II-C. Closed-form solutions for the 50% delay and overshoot/undershoots are presented in Section II-D. In Section II-E, results from this model are compared with SPICE. A maximum error of about 11% is exhibited.

A. Interconnect Transfer Function

A classical interconnect model is shown in Fig. 1. The interconnect is represented by a distributed *RLC* transmission line, where l is the interconnect length, and R , L , and C are the resistance, inductance, and capacitance per unit length, respectively. The driver is linearized as a voltage source V_{in} serially connected with a driver resistance R_d . The load of the interconnect is modeled as a capacitor C_l .

This equivalent circuit is a linear time-invariant (LTI) system. For LTI systems, the time-domain response can be solved by an inverse Laplace transform. From the *ABCD* parameters [13] of a transmission line, the transfer function from the input to the far end of a line is

$$H(s) = \frac{1}{(1 + R_d C_l s) \cosh \theta + (R_d / Z_c + Z_c C_l s) \sinh \theta} \quad (1)$$

where $\theta = l\sqrt{(R + sL)sC}$ and $Z_c = \sqrt{(R + sL)/sC}$. Since (1) includes hyperbolic functions of the complex frequency s , the inverse Laplace transform is difficult to derive directly. In order to simplify the problem, the denominator of the transfer function is expanded into an infinite series. By truncating this series, the transfer function is approximated by a few dominant poles [4], [6]. A distributed *RLC* line can also be modeled by lumped elements through moment matching [14].

In Fig. 2, the transfer function of some existing models [4], [6], [14] are compared with the exact transfer function described in (1). In this example, the interconnect parameters are $l = 2$ mm, $R = 8.829$ m $\Omega/\mu\text{m}$, $L = 1.538$ pH/ μm , and $C = 0.18$ fF/ μm . The per unit length parameters are calculated with FastHenry [15] and FastCap [16] for the top-layer metal interconnect in a standard 0.18- μm CMOS technology. The interconnect has a width $w = 2$ μm and a height $h = 1$ μm . The driver resistance and load capacitance are $R_d = 30$ Ω and $C_l = 50$ fF, respectively. The interconnect parameters from this example are used in the rest of this paper. As illustrated in Fig. 2, for this example, a simple L-type lumped model produces the poorest approximation. The two-pole model can be accurate up to 5 GHz. A nonuniform two stage L-type lumped model is a fourth-order approximation and has a similar accuracy range as the four-pole model, which is accurate up to 9 GHz; however, no closed-form solutions for these two models have been reported.

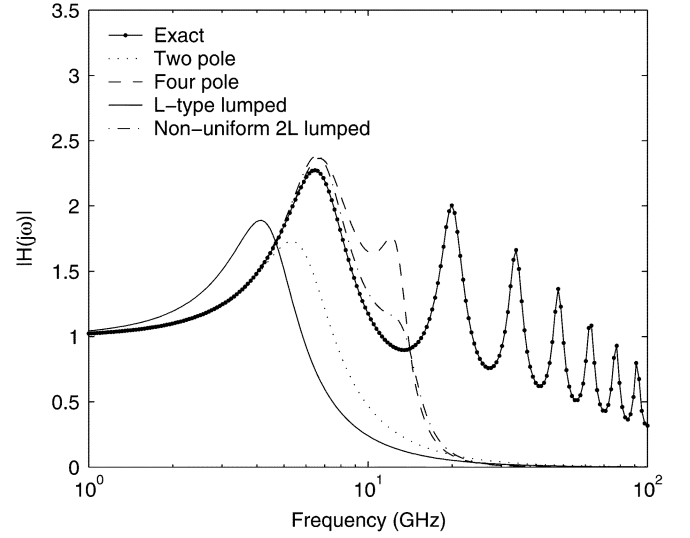


Fig. 2. Amplitude transfer function of different models of an *RLC* interconnect.

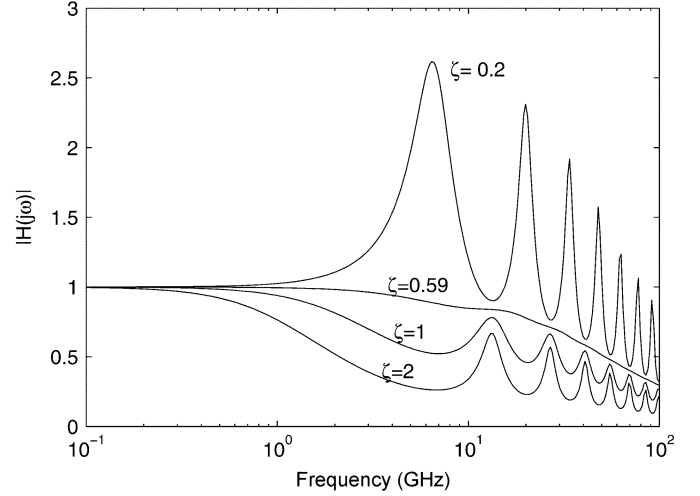


Fig. 3. Amplitude transfer functions of an *RLC* interconnect with different inductive effects.

The resonance frequencies (where the peaks occur in the exact transfer function) of the system are related to the poles of the transfer function. A nonuniform 2L model and a four-pole model can track the first peak of the exact transfer function, which means these two models can accurately model two poles of the system (the other pole is in the negative-frequency domain). The resonance frequencies are due to the reflection of the signal at the terminals; therefore, the resonance frequencies are approximately multiples of $1/4t_f$, where $t_f = l\sqrt{LC}$ is the time-of-flight. The high peaks in the transfer function are due to strong inductive effects. If the interconnect is *RC* dominant, the amplitude transfer function has no overshoots and decreases quickly with increasing frequency. In Fig. 3, the transfer functions with different inductive effects are shown. The inductance effects are characterized by a parameter ζ [1], and, in this example, ζ is varied by changing R_d . A small ζ implies significant inductive effects. As shown in Fig. 3, when $\zeta = 0.59$, which corresponds to $R_d = \sqrt{L/C}$ (the characteristic impedance at high frequencies), the reflection coefficient

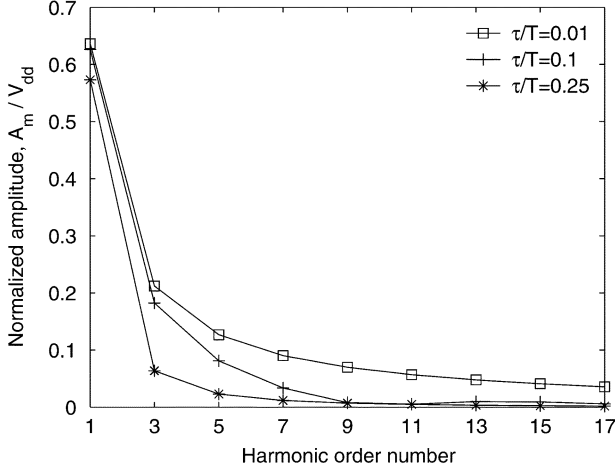


Fig. 4. Normalized amplitude of odd order harmonics.

Γ_s at the source is zero, thus, no resonance effects occur. When R_d is greater than $\sqrt{L/C}$, ζ is greater than 0.59, Γ_s is positive, and the basic resonance frequency is about $1/2t_f$. Alternatively, when R_d is less than $\sqrt{L/C}$, ζ is less than 0.59, Γ_s is negative, and the basic resonance frequency is about $1/4t_f$.

B. Fourier Series Representation of Input Signal

In previous work, the excitation signal is modeled as a step or ramp function, and most of the effort is focused on the transfer function. In this paper, however, a different approach is presented which focuses on the input signal. The input signal is approximated by a periodic ramp signal [17]

$$V_{in}(t) = \begin{cases} \frac{t}{\tau} V_{dd} & nT \leq t < nT + \tau \\ V_{dd} & nT + \tau \leq t < (n + \frac{1}{2})T \\ (1 - \frac{t}{\tau} + \frac{T}{2\tau}) V_{dd} & (n + \frac{1}{2})T \leq t < (n + \frac{1}{2})T + \tau \\ 0 & (n + \frac{1}{2})T + \tau \leq t < (n + 1)T \end{cases} \quad (2)$$

where T is the period of $V_{in}(t)$, n is an integer, and τ is the transition time. As is well known, a periodic signal can be represented as a summation of a Fourier series. The Fourier series representation of $V_{in}(t)$ is

$$V_{in}(t) = \frac{V_{dd}}{2} + \sum_{m=1,3,\dots} A_m \sin(m\omega_0 t + \phi_m) \quad (3)$$

$$\phi_m = -\frac{m\omega_0 \tau}{2} \quad (4)$$

$$A_m = \frac{2TV_{dd}}{\tau m^2 \pi^2} |\sin \phi_m| \quad (5)$$

where $\omega_0 = 2\pi/T$ is the basis angular frequency, and A_m and ϕ_m are the amplitude and phase of the m th-order harmonic, respectively. From (3), $V_{in}(t)$ is composed of the dc component and odd-order harmonics. Since A_m decreases quadratically with m , $V_{in}(t)$ can be approximated by the first several harmonics [17]. The normalized amplitude of the odd-order harmonics is shown in Fig. 4 for different τ/T . Note in Fig. 4 that the decrease in A_m slows with decreasing τ/T . In the limiting case, $\tau/T = 0$ and $A_m = 2V_{dd}/(m\pi)$, which is reciprocally proportional to m .

C. Far-End Time Domain Response

Since the circuit shown in Fig. 1 is linear and the input signal can be represented by a summation of harmonics, the superposition rule can be used to determine the output signal. The transfer function at each angular frequency ω can be represented as

$$H(j\omega) = H(s)|_{s=j\omega} = A(\omega)e^{j\beta(\omega)}. \quad (6)$$

From (1), the gain of the dc component is $H(0) = 1$. The output, therefore, is

$$V_{out}(t) = \frac{V_{dd}}{2} + \sum_{m=1,3,\dots} A'_m \sin(m\omega_0 t + \phi'_m) \quad (7)$$

$$A'_m = A_m A(m\omega_0) \quad (8)$$

$$\phi'_m = \phi_m + \beta(m\omega_0). \quad (9)$$

$V_{out}(t)$ can also be approximated by the first several lower order harmonics. In this paper, the Fourier series-based models are referred to as Fb3 and Fb5, with the largest harmonic order number of three and five, respectively. The results from Fb3 and Fb5 are compared with SPICE in Fig. 5. The input signal parameters are $T = 500$ ps, $\tau/T = 0.1$, and $V_{dd} = 1.5$ V. In the SPICE simulation, the interconnect line is divided into 200 segments and each segment is represented by an L-type lumped model. As shown in Fig. 5, two harmonics (Fb3) are sufficient to provide a good approximation of the output voltage waveform for this example.

D. 50% Delay and Overshoots/Undershoots

The 50% delay and overshoots/undershoots can be solved numerically from (7). In this paper, the 50% delay is assumed to be less than $T/2 - \tau/2$ (valid in most practical cases), and the overshoots/undershoots caused by the rising edge are measured between the waveform and ground, as shown in Fig. 5. For Fb3, since only two harmonics are considered, a closed-form solution is available. In this case

$$V_{out}(t) \approx \frac{V_{dd}}{2} + A'_1 \sin(\omega_0 t + \phi'_1) + A'_3 \sin(3\omega_0 t + \phi'_3). \quad (10)$$

To determine the 50% delay, (10) is set to $V_{dd}/2$. By applying the multiple-angle formulas [18], a third-order trigonometric expression can be obtained as

$$a_3 x^3 + a_2 x^2 + a_1 x + a_0 = 0 \quad (11)$$

where $x = \tan(\omega_0 t)$ and

$$a_0 = A'_1 \sin \phi'_1 + A'_3 \sin \phi'_3 \quad (12)$$

$$a_1 = A'_1 \cos \phi'_1 + 3A'_3 \cos \phi'_3 \quad (13)$$

$$a_2 = A'_1 \sin \phi'_1 - 3A'_3 \sin \phi'_3 \quad (14)$$

$$a_3 = A'_1 \cos \phi'_1 - A'_3 \cos \phi'_3. \quad (15)$$

A third-order expression has either one or three real roots, and a closed-form solution exists [11]. If (11) has only one real root x_0 , the output waveform crosses $V_{dd}/2$ only once from low-to-high during the first half of a period, therefore, the undershoot

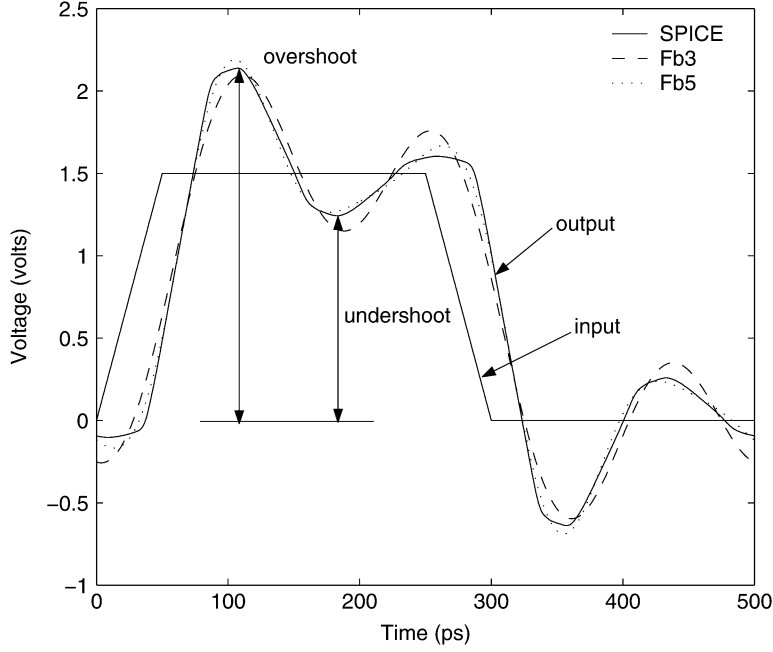


Fig. 5. Comparison of the time-domain response from Fb3 and Fb5 with SPICE.

is greater than $V_{dd}/2$. From this real root, the 50% delay can be expressed as

$$t_d = \frac{\arctan x_0}{\omega_0} - \frac{\tau}{2}. \quad (16)$$

The value of $\arctan x_0$ is in the range of $[0, \pi]$. If (11) has three real roots, the output waveform crosses $V_{dd}/2$ three times during the first half of the period, therefore the undershoot is less than $V_{dd}/2$. In this case, the output waveform is not shaped like a square wave and can no longer represent logic values.

The process for determining the overshoots/undershoots is similar to that of the delay. From (10), the derivative of V_{out} is

$$\frac{dV_{out}}{dt} \approx A'_1 \omega_0 \cos(\omega_0 t + \phi'_1) + 3A'_3 \omega_0 \cos(3\omega_0 t + \phi'_3). \quad (17)$$

Setting (17) to zero and applying the multiple-angle formulas, the following third-order trigonometric expression is obtained as

$$b_3 y^3 + b_2 y^2 + b_1 y + b_0 = 0 \quad (18)$$

where $y = \tan(\omega_0 t)$ and

$$b_0 = A'_1 \omega_0 \cos \phi'_1 + 3A'_3 \omega_0 \cos \phi'_3 \quad (19)$$

$$b_1 = -A'_1 \omega_0 \sin \phi'_1 - 9A'_3 \omega_0 \sin \phi'_3 \quad (20)$$

$$b_2 = A'_1 \omega_0 \cos \phi'_1 - 9A'_3 \omega_0 \cos \phi'_3 \quad (21)$$

$$b_3 = -A'_1 \omega_0 \sin \phi'_1 + 3A'_3 \omega_0 \sin \phi'_3. \quad (22)$$

The time when the extremum occurs can be obtained from the real roots of (18). Note that the time obtained can be less than t_f . This behavior occurs because the voltage response described by (7) is a steady-state response. The extremum which occurs before t_f is the response to the previous period of the input

signal. For the response to the current period, the time when the extremum occurs should be

$$t_p = \begin{cases} \arctan y_0 & \arctan y_0 > t_f \\ \arctan y_0 + \frac{T}{2} & \arctan y_0 \leq t_f \end{cases} \quad (23)$$

where y_0 is a real root of (18). Inserting t_p into (10), the corresponding extremum is

$$V_{ex} \approx \frac{V_{dd}}{2} + A'_1 \sin(\omega_0 t_p + \phi'_1) + A'_3 \sin(3\omega_0 t_p + \phi'_3). \quad (24)$$

The overshoot and undershoot are chosen as the maximum and minimum of the results obtained in (24), respectively.

If higher accuracy is required, more harmonics should be included in the model, and higher order (fifth, seventh, ...) equations should be solved. Since only real roots are of interest, some efficient root-finding algorithms can be used, such as the Newton–Raphson method. The complexity, however, increases.

Since the output waveform is approximated by a summation of sinusoids, some of the undershoots obtained are not real undershoots (called *pseudundershoots* in this paper) and should be discarded. By comparing the waveforms obtained by the model with SPICE simulations, three such cases are found.

- 1) There is only one extremum.
- 2) The last extremum (according to the time index) is the largest.
- 3) All extremum values are greater than V_{dd} .

In these cases, either the output is overdamped or the period is too short for the waveform to achieve the undershoot within half a period. Examples of different cases are shown in Fig. 6.

E. Model Verification and Discussion

The 50% delay calculated with the proposed model is compared with SPICE in Table I. The interconnect parameters for $w = 6 \mu\text{m}$ are $R = 3.35 \text{ m}\Omega/\mu\text{m}$, $L = 1.36 \text{ pH}/\mu\text{m}$, and $C =$

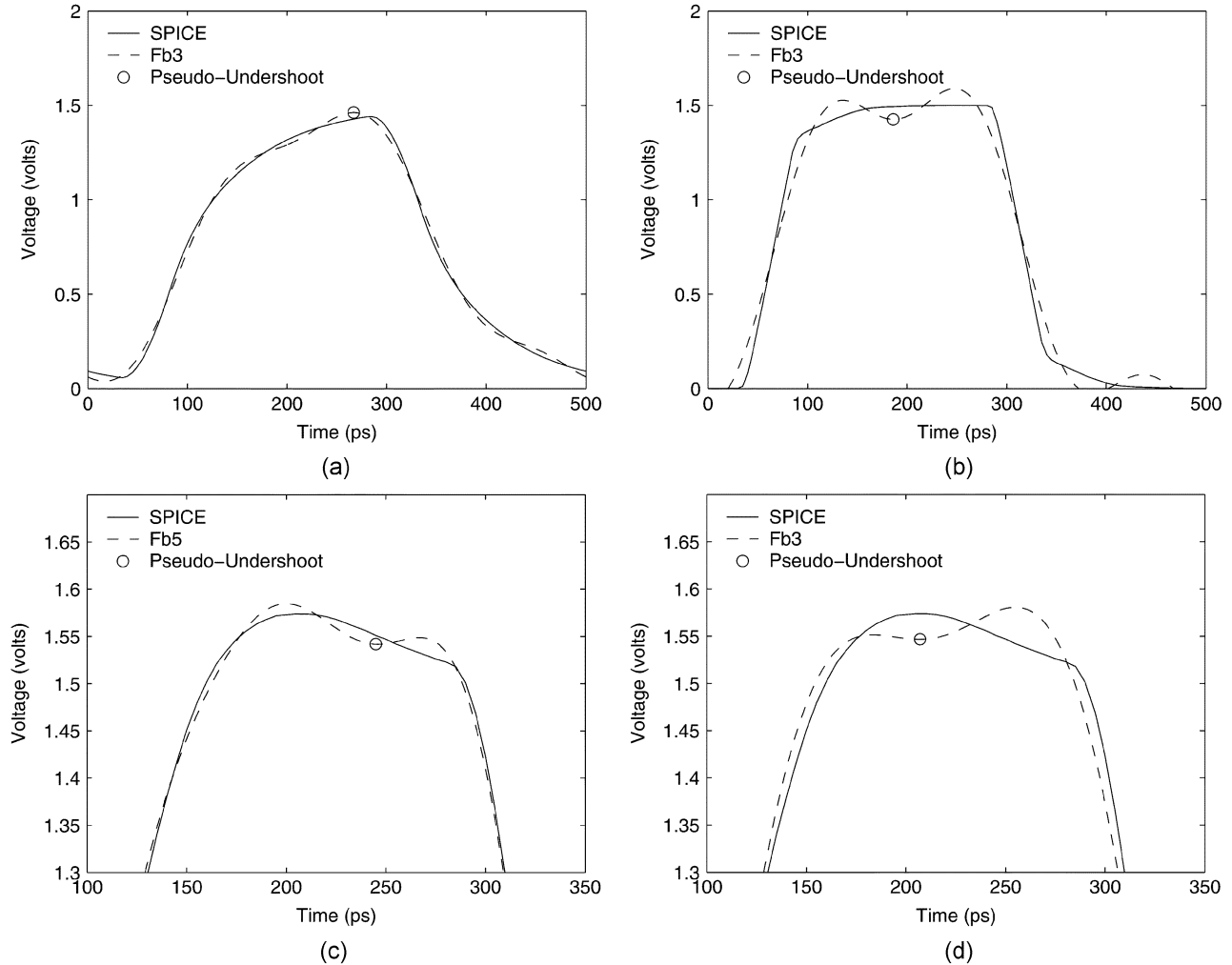


Fig. 6. Examples of pseudoundershoots for different cases. (a) Case1, $R_d = 100 \Omega$ and $C_l = 500$ fF. (b) Case2, $R_d = 100 \Omega$ and $C_l = 50$ fF. (c) Case3, $R_d = 60 \Omega$ and $C_l = 500$ fF. (d) Case2 and case3, $R_d = 60 \Omega$ and $C_l = 500$ fF. The input signal parameters are $T = 500$ ps, $\tau/T = 0.1$, and $V_{dd} = 1.5$ V.

TABLE I

COMPARISON OF THE 50% DELAY FROM Fb3 AND Fb5 WITH SPICE AND A SINGLE POLE MODEL. THE INPUT SIGNAL PARAMETERS ARE $T = 500$ ps, $\tau = 50$ ps, AND $V_{dd} = 1.5$ V. THE INTERCONNECT PARAMETERS ARE $l = 2$ mm AND $h = 1 \mu\text{m}$

w (μm)	R_d (Ω)	C_l (fF)	SPICE (ps)	1-pole (ps)	Fb3 (ps)	Fb5 (ps)
2	20	50	28.9	11.5	25.9	29.0
2	60	100	40.1	25.7	39.1	40.0
2	100	500	73.5	69.0	77.0	74.2
6	20	50	41.8	14.8	40.7	42.0
6	40	100	45.4	26.1	44.4	45.4
6	60	500	68.6	53.5	71.3	69.5
10	20	50	47.2	19.0	45.9	46.9
10	40	100	53.1	34.0	52.6	52.9
10	60	500	74.5	65.7	77.1	75.3
Maximum Error				64.6%	10.4%	1.3%
Average Error				37.7%	3.7%	0.6%

TABLE II

COMPARISON OF OVERSHOOTS/UNDERSHOOTS FROM Fb3 AND Fb5 WITH SPICE SIMULATIONS. THE INPUT SIGNAL PARAMETERS ARE $T = 500$ ps, $\tau = 50$ ps, AND $V_{dd} = 1.5$ V. THE INTERCONNECT PARAMETERS ARE $l = 2$ mm AND $h = 1 \mu\text{m}$

w (μm)	R_d (Ω)	C_l (fF)	Overshoot (volts)			Undershoot (volts)		
			SPICE	Fb3	Fb5	SPICE	Fb3	Fb5
2	20	10	2.30	2.11	2.29	1.08	1.08	1.08
2	30	50	2.14	2.10	2.19	1.24	1.15	1.26
2	60	100	1.71	1.77	1.75	1.47	1.40	1.44
6	20	10	2.29	2.35	2.40	1.13	1.00	1.12
6	30	50	2.00	2.08	2.08	1.34	1.25	1.31
6	40	100	1.80	1.89	1.85	1.44	1.38	1.40
10	20	10	2.11	2.21	2.17	1.26	1.21	1.19
10	30	50	1.85	1.96	1.91	1.42	1.38	1.36
10	40	100	1.65	1.75	1.69	1.49	1.44	1.44
Maximum Error			8.3%	4.8%	—	11.5%	5.6%	—
Average Error			4.7%	2.8%	—	4.9%	2.5%	—

0.33 fF/ μm . The interconnect parameters for $w = 10 \mu\text{m}$ are $R = 2.2$ m $\Omega/\mu\text{m}$, $L = 1.26$ pH/ μm , and $C = 0.49$ fF/ μm . Results from a single pole model with a ramp input [5] are also listed. As expected, the single pole model is accurate only when the circuit is dominated by the RC impedance. When the circuit is dominated by the LC impedance, the error is large. However, the proposed Fourier series-based method provides accurate delay estimates for both RC -dominated and LC -dominated

circuits. The average error of Fb5 is only 0.6% over a wide range of circuit parameters (the parameters are selected such that the bandwidth requirement is satisfied). The overshoots/undershoots for underdamped responses resulting from Fb3 and Fb5 are compared with SPICE in Table II. As listed in Tables I and II, the model becomes more accurate with additional harmonics.

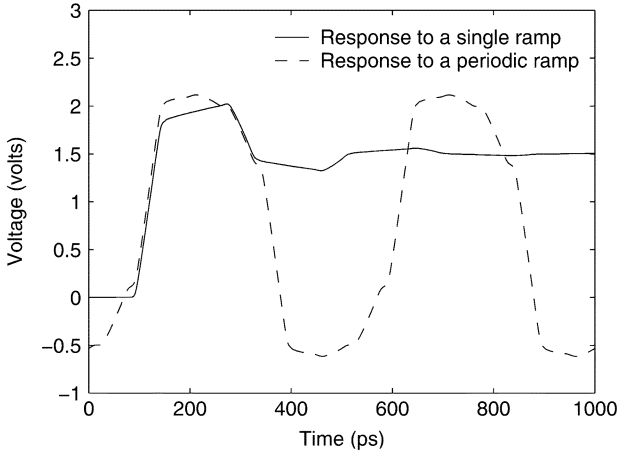


Fig. 7. Effect of initial conditions on the periodic signals. $l = 5$ mm.

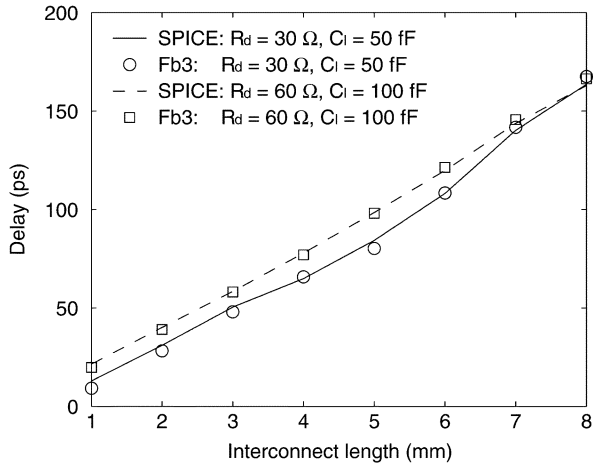


Fig. 8. 50% delay versus interconnect length. $w = 2$ μ m, $T = 500$ ps, and $\tau = 50$ ps.

In Tables I and II, the delay and overshoots/undershoots obtained from Fb3, Fb5, and SPICE characterize the steady-state response. If the response to a rising edge (or falling edge) cannot converge to V_{dd} (or 0) within half a period, the charge and current at the end of a period become the initial conditions of the following period. These initial conditions, however, can have a significant effect on propagating high-frequency signals along long interconnects. The far-end response to a single ramp input and a periodic ramp input are compared in Fig. 7. As shown in Fig. 7, the position and value of the overshoot are quite different for the two responses. For periodic signals, the method presented here is more suitable than other models in which zero initial conditions are assumed. In Fig. 8, the delay model is examined for various interconnect lengths. The interconnect inductance is determined for each interconnect length, since the inductance does not increase linearly with line length. Another advantage of the proposed model is that frequency-dependent effects of the interconnect can be directly included, since the transfer function is calculated at each individual frequency.

The accuracy of the proposed model depends on the frequency spectrum of the far-end response. If most of the signal energy is allocated in the lower order harmonics, neglecting those higher order harmonics will cause little error and the

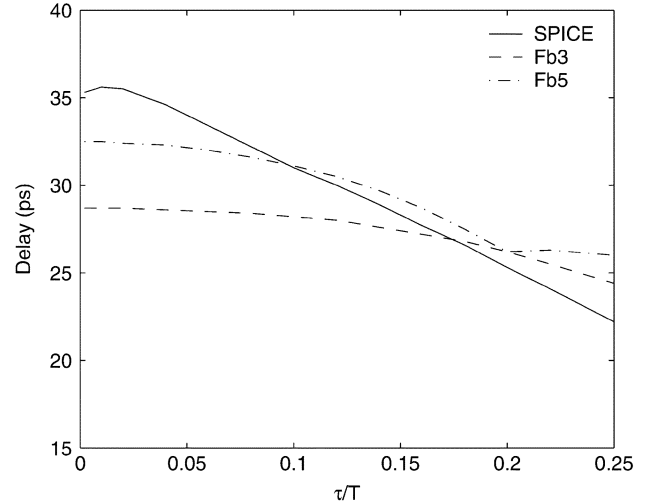


Fig. 9. 50% delay for different τ/T . $w = 2$ μ m, $l = 2$ mm, $T = 500$ ps, $V_{dd} = 1.5$ V, $R_d = 30$ Ω , and $C_l = 50$ fF.

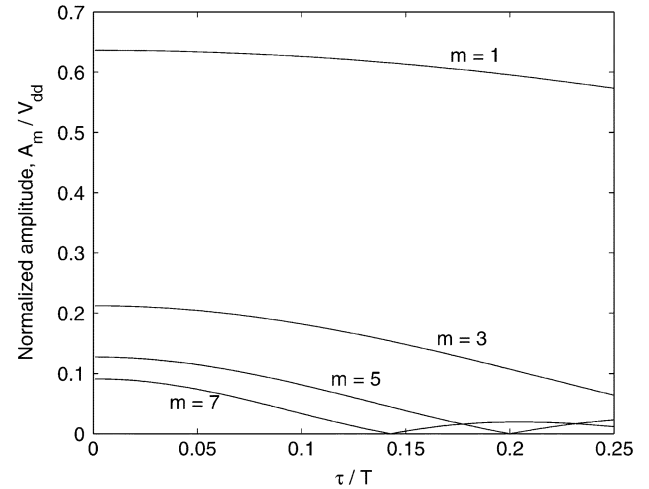


Fig. 10. Normalized amplitude of harmonics with different τ/T .

model is accurate; otherwise, the accuracy of the model will decrease. From Figs. 3 and 4, it can be concluded that the accuracy becomes worse for signals with small τ/T propagating along highly inductive interconnects. The 50% delay with different τ/T is shown in Fig. 9. Note that the accuracy of the model increases when τ/T increases from zero. From (5), when m is large, A_m no longer decreases monotonically with τ/T , as shown in Fig. 10, since the term $|\sin \phi_m|$ also depends on τ/T . This effect is demonstrated in Fig. 9. Note that when τ/T is greater than 0.2, the results from Fb3 and Fb5 start to deviate from the SPICE simulations and the highest accuracy of Fb3 and Fb5 occurs when τ/T is between 0.1 and 0.2.

For highly LC dominant interconnects, the accuracy of the model also depends on the frequency of the signal. The 50% delay and overshoots for different signal frequencies are shown in Fig. 11. For a fixed τ/T , changing the frequency of the input signal corresponds to stretching the Fourier series in the frequency domain. When the signal frequency is much less than the resonance frequencies, all of the primary harmonics are located in the flat region of the transfer function curve. Those harmonics which are close to the resonance frequencies are suffi-

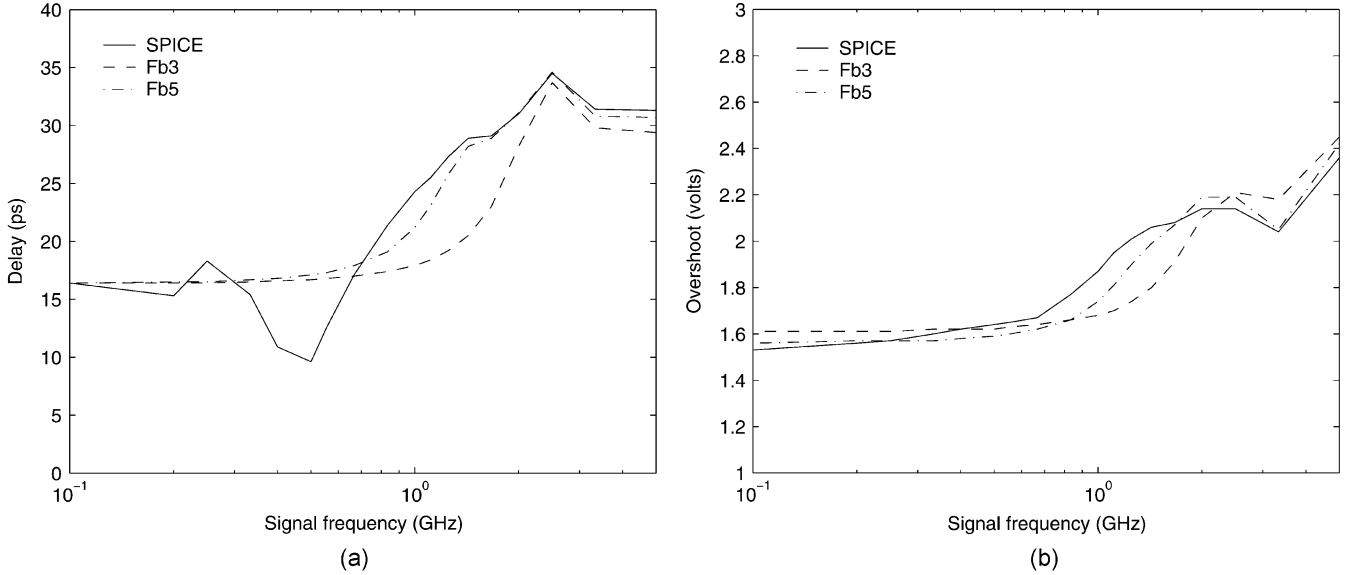


Fig. 11. Effects of signal frequency on the accuracy of the proposed model. (a) 50% delay. (b) Overshoot. The circuit parameters are $w = 2 \mu\text{m}$, $l = 2 \text{ mm}$, $\tau/T = 0.1$, $V_{\text{dd}} = 1.5 \text{ V}$, $R_d = 30 \Omega$, and $C_l = 50 \text{ fF}$.

ciently small that they can be safely neglected. The interconnect line behaves as a pure delay segment and the proposed model exhibits good accuracy. With the frequency increasing, the first two or three harmonics remain in the flat region in the amplitude transfer function. The remaining harmonics, however, approach those resonance frequencies and are amplified. Neglecting these harmonics will produce significant error. As shown in Fig. 11(a), the maximum error of the 50% delay for this example circuit occurs at 500 MHz. With the signal frequency continuously increasing, the first several harmonics also approach the resonance frequencies and are amplified, therefore, the ratio between the harmonics which are included in the model and the harmonics which are neglected increases, making the proposed model more accurate. Since the resonance frequency is related to t_f , when the interconnect length increases, the resonance frequency decreases. With technology scaling, the global interconnect becomes longer and the clock frequency becomes higher. The proposed model is expected to become more accurate with higher speed circuits.

III. DISTRIBUTED *RLC* TREES

Interconnect trees are widely used in clock distribution networks. In this section, the proposed Fourier series-based model is extended to tree structures. Arbitrarily accurate results can be obtained by including a different number of harmonics. The computational complexity is linear with the size of the tree and the number of harmonics. In Section III-A, the transfer function of a distributed *RLC* tree is developed. In Section III-B, a tree example is analyzed with the Fourier series-based model.

A. Transfer Function of Distributed *RLC* Trees

An example of a distributed *RLC* tree is shown in Fig. 12. In this example, a driver with an output resistance R_d is connected to the root of the tree N_0 . All of the output nodes ($N_5 \dots N_9$) are called leaves and connected with load buffers which can be used to drive the *RLC* trees in the next level. The load buffers

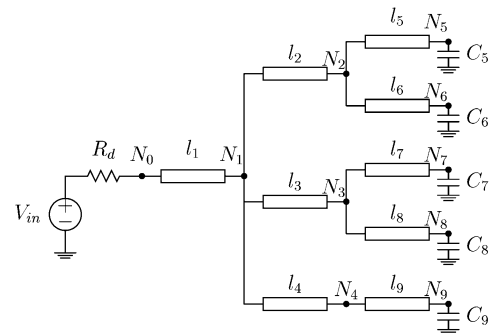


Fig. 12. Distributed *RLC* tree.

are modeled by capacitors. All of the branches in the tree are represented by distributed *RLC* lines. The tree can be balanced or unbalanced; however, unbalanced trees exhibit more complex characteristics than balanced trees [7].

The transfer function from N_0 to a certain node N_i is the product of the transfer function of all of the branches along the unique path from N_0 to N_i . For a transmission line of length l with load Z_L at the far end, the input impedance seen from the near end is

$$Z_{\text{in}} = Z_c \frac{Z_L + Z_c \tanh \theta}{Z_c + Z_L \tanh \theta} \quad (25)$$

where θ and Z_c are defined in Section II-A. For a node with multiple fanout, the load impedance seen at this node is the parallel combination of the input impedance of the downstream branches which are connected to this node. The computational complexity of computing the input impedance at the nodes in the tree is $O(n_{\text{tr}})$, where n_{tr} is the number of branches in the entire tree. The transfer function of a single branch can be obtained by replacing R_d by 0 and C_i s by $1/Z_L$ in (1)

$$H(s) = \frac{1}{\cosh \theta + (Z_c/Z_L) \sinh \theta}. \quad (26)$$

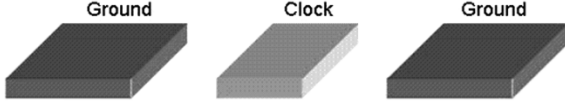


Fig. 13. Example of a shielded clock-wire structure.

TABLE III
INTERCONNECT LENGTHS SHOWN IN FIG. 12 NORMALIZED TO l_x

Index	l_1	l_2	l_3	l_4	l_5	l_6	l_7	l_8	l_9
Length	0.5	1	2	0.5	1	0.5	2	1	1

TABLE IV
LOAD CAPACITANCES SHOWN IN FIG. 12 NORMALIZED TO C_x

Index	C_5	C_6	C_7	C_8	C_9
Capacitance	2	0.5	2	5	1

The transfer function from the voltage source to a certain node N_i , therefore, is

$$H_i(s) = \frac{Z_{L,0}}{R_d + Z_{L,0}} \prod_k \frac{1}{\cosh \theta_k + (Z_{c,k}/Z_{L,k}) \sinh \theta_k} \quad (27)$$

where $Z_{L,0}$ is the input impedance seen from N_0 , and k is the index covering each branch in the path from N_0 to N_i . From (27), the computational complexity of computing the transfer function at node N_i for one frequency is $O(n_i)$, where n_i is the number of branches along the path from N_0 to N_i . Upon obtaining $H_i(s)$, the Fourier series-based model can be applied. The total computation complexity to determine the time domain response at node N_i is

$$\Theta(n_f, n_{tr}, n_i) = n_f \cdot O(n_{tr}) + n_f \cdot O(n_i) \quad (28)$$

where n_f is the number of harmonics included in the model. Note that the first term in (28) is related to calculating the input impedances of the branches, which are calculated only once for a specific tree. To determine the response at another node, the additional computational complexity is the second term in (28).

B. Examples

The tree structure shown in Fig. 12 is evaluated in this section. The branches in the tree can have different parasitic interconnect impedances. For simplicity, the branches are assumed to have the same width of $6 \mu\text{m}$. In high-speed clock networks, ground wires are often placed at each side of the signal line as shields [19], [20], as shown in Fig. 13. Since these ground wires provide a nearby current return path, the effective inductance of the signal wire is greatly reduced. The width of the shield wire is assumed to be $10 \mu\text{m}$ and the space between the shield and the clock line is $6 \mu\text{m}$. The interconnect parameters of such a structure are $R = 3.9 \text{ m}\Omega/\mu\text{m}$, $L = 0.43 \text{ pH}/\mu\text{m}$, and $C = 0.36 \text{ fF}/\mu\text{m}$. An effective conductivity of $2.2 \mu\Omega\text{-cm}$ is used to determine the resistance and inductance. The normalized wire length and load capacitance shown in Fig. 12 are listed in Tables III and IV, where l_x and C_x are the normalized reference length and capacitance, respectively.

TABLE V
50% DELAYS AT NODES $N5$ AND $N7$ AS SHOWN IN FIG. 12
WITH DIFFERENT CIRCUIT PARAMETERS

l_x (mm)	R_d (Ω)	C_x (fF)	Node	SPICE (ps)	[4] (ps)	[7] (ps)	Fb3 (ps)	Fb5 (ps)
0.2	10	20	$N5$	13.1	10.3	10.2	9.0	10.3
0.2	10	20	$N7$	11.6	14.0	13.8	10.6	11.2
0.2	10	500	$N5$	35.5	50.0	49.1	49.0	37.1
0.2	10	500	$N7$	59.9	60.8	58.6	60.1	60.0
0.2	30	20	$N5$	23.9	23.6	23.5	25.1	24.1
0.2	30	20	$N7$	23.5	25.6	25.4	25.7	24.5
0.2	30	100	$N5$	42.7	40.0	39.8	43.2	42.1
0.2	30	100	$N7$	39.4	43.1	42.5	44.1	41.2
1	10	20	$N5$	41.3	54.3	52.2	37.0	40.8
1	10	20	$N7$	75.8	79.7	75.1	77.5	75.3
1	10	100	$N5$	51.3	63.3	60.4	49.9	52.4
1	10	100	$N7$	89.6	93.0	86.9	89.6	89.2
1	20	20	$N5$	49.2	71.3	68.6	48.4	48.3
1	20	20	$N7$	86.4	96.1	89.4	90.6	88.1
1	20	100	$N5$	57.4	85.1	81.7	57.7	58.8
1	20	100	$N7$	104.1	114.0	105.4	103.4	102.9
Maximum Error					48.3%	42.3%	38.0%	21.4%
Average Error					18.0%	15.0%	7.6%	3.3%
Standard Deviation of Error					15.8%	14.7%	10.3%	5.0%

A 2-GHz clock signal with $\tau = 50 \text{ ps}$ is applied at the input of the tree. The 50% delay at nodes $N5$ and $N7$ are listed in Table V for a range of circuit parameters. Results from the two-pole model [4] and the equivalent Elmore delay model [7] are also listed for comparison. Since no closed-form solution for a ramp input signal is available with these methods, the values listed in Table V are obtained through curve measurement. The branches in the tree are represented by lumped L-type models in [4] and [7].

The methods presented in [4] and [7] have similar accuracy and complexity, since both of these models are based on second-order approximations. For a response which is low-frequency dominant, such as the response at node $N7$, these second order methods can produce accurate delay estimates. For a response which exhibits more high-frequency effects, such as the response at node $N5$, the error caused by these second-order methods becomes large. These high frequency effects originate not only from the complexity of the tree structure, but also from the distributed properties of the interconnect, which cannot be modeled by lumped elements. As listed in Table V, Fb3 and Fb5 produce higher accuracy than those second order approximations, particularly for node $N5$. The average error of Fb5 is only 3.3%. The time domain response obtained by different models at nodes $N5$ and $N7$ is compared with SPICE simulations in Fig. 14. As shown in Fig. 14, although the equivalent Elmore delay model provides satisfactory estimation of the 50% delay at node $N7$, other information characterizing the waveform is lost, such as the overshoots and transition times. The 10% to 90% transition times from different models are compared with SPICE in Table VI. As listed in Table VI, all of the models exhibit worse accuracy for the transition times as compared with the 50% delay, since additional high-frequency harmonics are required to characterize the signal transition times. Among the models, Fb5 is the most accurate, exhibiting an average error of 5.8%.

The accuracy of the Fourier series-based model can be enhanced to capture the fine details of the waveform by including

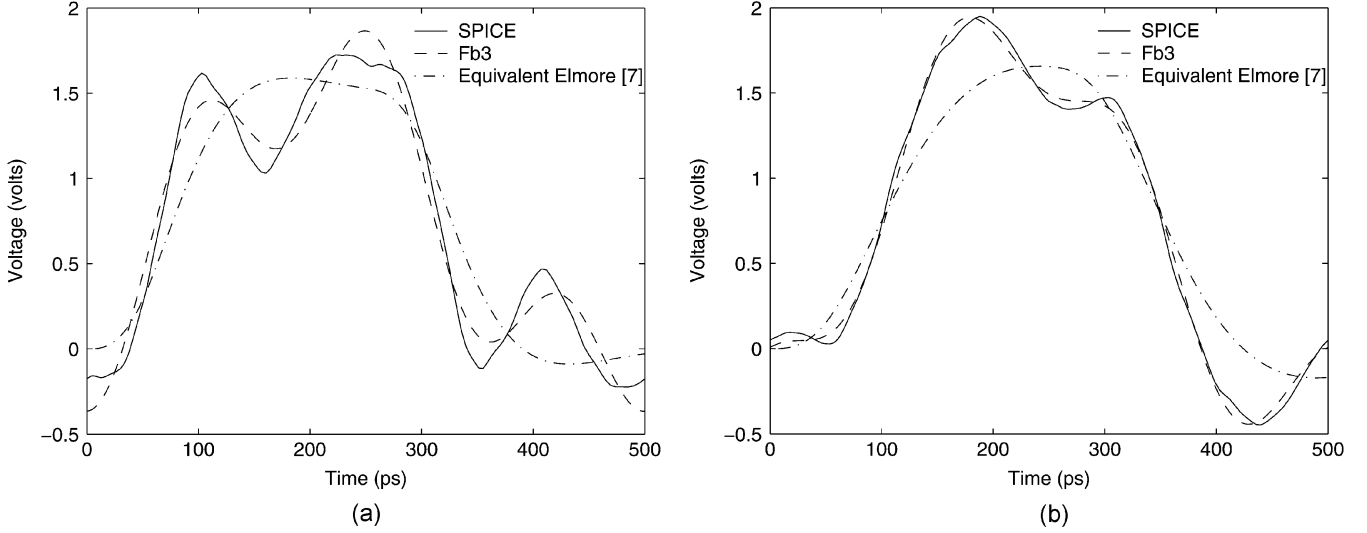


Fig. 14. Time-domain response at the leaves of the tree shown in Fig. 12. (a) Node N_5 . (b) Node N_7 . The circuit parameters are $l_x = 1$ mm, $\tau = 50$ ps, $T = 500$ ps, $V_{dd} = 1.5$ V, $R_d = 10$ Ω , and $C_x = 20$ fF.

TABLE VI
TRANSITION TIMES AT NODES N_5 AND N_7 AS SHOWN IN FIG. 12
WITH DIFFERENT CIRCUIT PARAMETERS

l_x (mm)	R_d (Ω)	C_x (fF)	Node	SPICE (ps)	[4] (ps)	[7] (ps)	Fb3 (ps)	Fb5 (ps)
0.2	10	20	N_5	40.0	38.9	39.0	60.4	46.3
0.2	10	20	N_7	32.1	36.3	36.4	56.5	39.6
0.2	10	500	N_5	130.5	127.2	130.4	159.3	132.8
0.2	10	500	N_7	97.7	119.8	124.9	98.9	99.9
0.2	30	20	N_5	69.3	68.3	68.9	75.8	68.9
0.2	30	20	N_7	60.1	63.2	64.3	71.3	61.0
0.2	30	100	N_5	132.9	118.5	119.4	126.8	124.2
0.2	30	100	N_7	106.3	113.7	115.9	111.6	117.0
1	10	20	N_5	39.1	81.4	81.3	53.8	39.7
1	10	20	N_7	60.5	107.1	104.9	65.6	58.8
1	10	100	N_5	45.2	97.1	97.6	52.1	52.4
1	10	100	N_7	79.2	128.2	126.2	81.7	80.5
1	20	20	N_5	157.9	149.5	156.9	176.0	156.1
1	20	20	N_7	90.6	158.4	165.4	88.4	88.0
1	20	100	N_5	188.3	188.5	198.6	195.3	193.3
1	20	100	N_7	135.3	198.6	212.3	138.7	139.1
Maximum Error					114.8%	115.9%	76.0%	23.4%
Average Error					34.6%	35.8%	17.0%	5.8%
Standard Deviation of Error					40.1%	40.6%	21.0%	6.8%

additional harmonics. As shown in (28), the complexity of higher order Fourier series-based models is linear with the number of harmonics. Furthermore, there are no stability and numerical problems such as suffered by AWE [8]. In Fig. 15, the Fourier series-based model with a different number of harmonics is compared with SPICE simulations. τ is reduced to 5 ps to emphasize the high-frequency effects. As shown in Fig. 15, results from the tenth-order Fourier series-based model are sufficiently close to the SPICE simulations. These experiments are performed on a SunBlade1000 workstation. In SPICE simulations, each branch is represented by 100 lumped elements. The time required by SPICE to simulate one clock period (500 ps) is 9.6 s. The run time of the tenth-order model (implemented by Matlab) is about 6.6 ms.

Clock distribution networks are typically hierarchically structured. A high-level interconnect tree distributes the clock signal

to several buffers, which drive the lower level interconnect trees. The buffers in the clock-distribution networks are nonlinear devices, and the clock signal is reshaped by these buffers. The proposed model, therefore, is limited to a single tree structure. By combining the signal waveform at the output node of a tree and the buffer model, the effective input signal for the tree of the next level can be obtained. The proposed model, therefore, can be applied to each individual tree in a specific clock network, permitting the entire network to be analyzed. The analysis of a hierarchical clock-distribution network, however, is omitted in this paper due to space limitations.

IV. MULTIPLE COUPLED INTERCONNECT LINES

The solution for a single distributed RLC line can also be extended to multiple coupled transmission lines. In Section IV-A, the modal analysis-based decoupling method is reviewed. A general solution for multiple transmission lines is presented in Section IV-B. The model is verified by SPICE in Section IV-C.

A. Decoupling Multiconductor Systems

For multiple transmission lines, the interconnect parameters per unit length are the resistance matrix \mathbf{R} , inductance matrix \mathbf{L} , and capacitance matrix \mathbf{C} . All of these matrices are symmetric with the dimension of $N \times N$, where N is the number of lines. From the telegrapher equations of N coupled transmission lines, the voltage vector \mathbf{V} and current vector \mathbf{I} have the following relationship in the frequency domain:

$$\frac{\partial}{\partial x} \begin{pmatrix} \mathbf{V} \\ \mathbf{I} \end{pmatrix} = - \begin{pmatrix} \mathbf{0} & \mathbf{Z} \\ \mathbf{Y} & \mathbf{0} \end{pmatrix} \begin{pmatrix} \mathbf{V} \\ \mathbf{I} \end{pmatrix} \quad (29)$$

where $\mathbf{Z} = \mathbf{R} + s\mathbf{L}$ and $\mathbf{Y} = s\mathbf{C}$.

Decoupling (29) can be achieved by applying a modal analysis [9], [10]. The matrix \mathbf{ZY} for a practical system is always diagonalizable [10]

$$\mathbf{ZY} = \mathbf{MQM}^{-1} \quad (30)$$

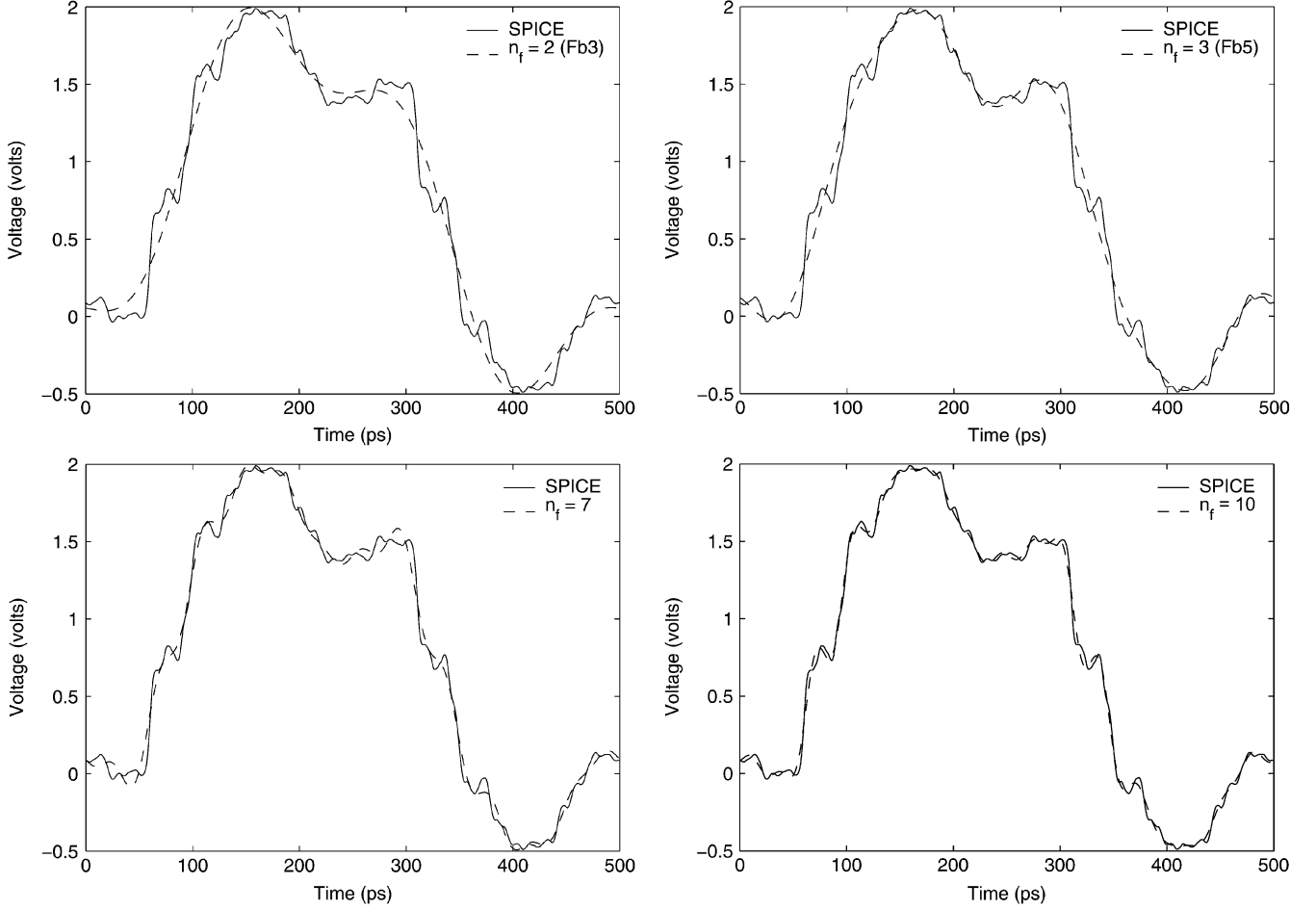


Fig. 15. Time-domain response at node $N7$ as shown in Fig. 12, evaluated by the Fourier series-based model with different n_f as compared with SPICE simulations. The circuit parameters are $l_x = 1$ mm, $\tau = 5$ ps, $T = 500$ ps, $V_{\text{dd}} = 1.5$ V, $R_d = 10$ Ω , and $C_x = 20$ fF.

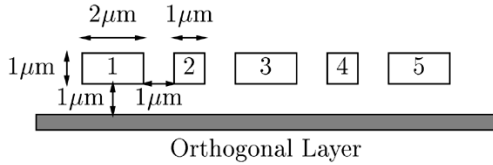


Fig. 16. Geometric characteristics of five parallel interconnect lines.

where \mathbf{Q} is a diagonal matrix with eigenvalues of \mathbf{ZY} as the diagonal elements, and matrix \mathbf{M} has the corresponding eigenvectors of \mathbf{ZY} as the columns. Performing a linear transformation of \mathbf{V} and \mathbf{I}

$$\mathbf{V} = \mathbf{M}\hat{\mathbf{V}} \quad (31)$$

$$\mathbf{I} = (\mathbf{M}^T)^{-1}\hat{\mathbf{I}} \quad (32)$$

and substituting (31) and (32) into (29), (29) becomes

$$\frac{\partial}{\partial x} \begin{pmatrix} \hat{\mathbf{V}} \\ \hat{\mathbf{I}} \end{pmatrix} = - \begin{pmatrix} \mathbf{0} & \hat{\mathbf{Z}} \\ \hat{\mathbf{Y}} & \mathbf{0} \end{pmatrix} \begin{pmatrix} \hat{\mathbf{V}} \\ \hat{\mathbf{I}} \end{pmatrix} \quad (33)$$

where $\hat{\mathbf{Z}} = \mathbf{M}^{-1}\mathbf{Z}(\mathbf{M}^T)^{-1}$ and $\hat{\mathbf{Y}} = \mathbf{M}^T\mathbf{Y}\mathbf{M}$. Since \mathbf{Z} and \mathbf{Y} are symmetric, $\hat{\mathbf{Z}}$ and $\hat{\mathbf{Y}}$ are both diagonal [9]. The N coupled interconnect lines are, therefore, decoupled into N independent

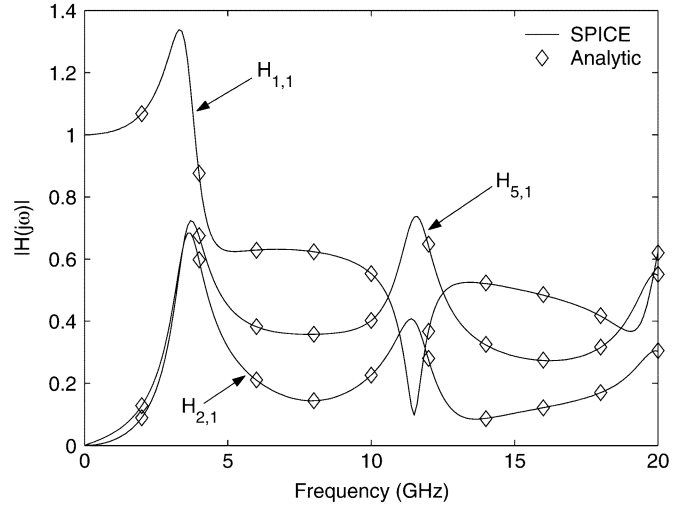


Fig. 17. Amplitude transfer functions of a five-line system.

lines. The characteristic impedance matrix $\hat{\mathbf{Z}}_c$ and the propagation coefficient matrix $\hat{\gamma}$ of the decoupled system are

$$\hat{\mathbf{Z}}_c = \sqrt{\hat{\mathbf{Z}}\hat{\mathbf{Y}}^{-1}} = \text{diag}(\hat{Z}_{c,1}, \hat{Z}_{c,2}, \dots, \hat{Z}_{c,N}) \quad (34)$$

$$\hat{\gamma} = \sqrt{\hat{\mathbf{Z}}\hat{\mathbf{Y}}} = \sqrt{\mathbf{Q}} = \text{diag}(\hat{\gamma}_1, \hat{\gamma}_2, \dots, \hat{\gamma}_N). \quad (35)$$

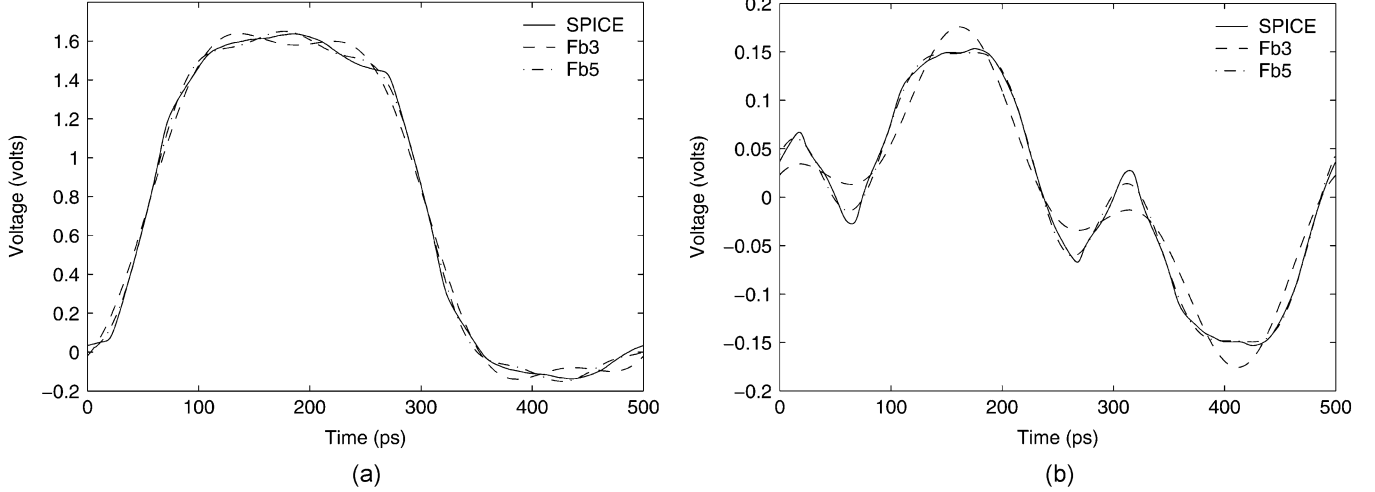


Fig. 18. Comparison of the far-end response from Fb3 and Fb5 with SPICE in a five-line coupled system, (a) line 1 and (b) line 2. The input-signal parameters are $T = 500$ ps, $\tau = 50$ ps, and $V_{dd} = 1.5$ V.

This decoupling method has been extended to drivers and loads in [11] and [12] for two and more interconnects. These extensions, however, are only suitable for identical lines with identical drivers and loads. Furthermore, the inductance matrix in [12] is obtained as $\mathbf{L} = \mathbf{C}^{-1}/v^2$, where v is the speed of light in a dielectric. This expression is only valid for a homogeneous dielectric environment with an ideal ground for the current return path. Due to these constraints, the practical generality of these models is greatly limited.

B. Far-End Response

Applying the $ABCD$ parameter concept to (33), the voltage and current vectors at the boundary have the following relationship:

$$\begin{pmatrix} \hat{\mathbf{V}}_d \\ \hat{\mathbf{I}}_d \end{pmatrix} = \begin{pmatrix} \hat{\mathbf{A}}_p & \hat{\mathbf{B}}_p \\ \hat{\mathbf{C}}_p & \hat{\mathbf{D}}_p \end{pmatrix} \begin{pmatrix} \hat{\mathbf{V}}_r \\ \hat{\mathbf{I}}_r \end{pmatrix} \quad (36)$$

where the subscript d and r represent the driver side (or near end) and receiver side (or far end), respectively. The $ABCD$ [13] matrices of the decoupled transmission lines are

$$\hat{\mathbf{A}}_p = \text{diag}(\cosh \hat{\gamma}_k, k = 1, 2, \dots, N) \quad (37)$$

$$\hat{\mathbf{B}}_p = \text{diag}(\hat{Z}_{c,k} \sinh \hat{\gamma}_k, k = 1, 2, \dots, N) \quad (38)$$

$$\hat{\mathbf{C}}_p = \text{diag}\left(\frac{\sinh \hat{\gamma}_k}{\hat{Z}_{c,k}}, k = 1, 2, \dots, N\right) \quad (39)$$

$$\hat{\mathbf{D}}_p = \text{diag}(\cosh \hat{\gamma}_k, k = 1, 2, \dots, N). \quad (40)$$

The boundary conditions of the N coupled interconnects are

$$\mathbf{V}_d = \mathbf{V}_{in} - \mathbf{R}_d \mathbf{I}_d \quad (41)$$

$$\mathbf{I}_r = s \mathbf{C}_l \mathbf{V}_r \quad (42)$$

TABLE VII
COMPARISON OF THE MAXIMUM CROSSTALK NOISE FROM Fb3 AND Fb5 WITH SPICE SIMULATIONS. THE INPUT SIGNAL PARAMETERS ARE $T = 500$ ps, $\tau = 50$ ps, AND $V_{dd} = 1.5$ V

Case	l (mm)	Victim	SPICE (mV)	Fb3 (mV)	Fb5 (mV)
Five lines	1	V2	207.1	184.2	210.2
		V3	200.4	166.6	205.2
		V4	197.1	160.9	200.7
		V5	197.4	157.4	199.0
		V2	153.3	175.9	149.3
Five lines	2	V3	146.2	180.8	140.6
		V4	154.3	183.6	147.9
		V5	165.5	184.4	152.3
		V2	204.9	139.7	197.1
		V3	175.6	105.3	171.2
Three lines	2	V2	227.6	253.6	233.9
		V3	246.9	231.0	204.1
		Maximum Error			40.0%
Average Error			18.8%	4.3%	

where \mathbf{R}_d and \mathbf{C}_l are the driver resistance matrix and load capacitance matrix, respectively. Both of these matrices are diagonal. Combining (36) with (31), (32), (41), and (42), the voltage vector at the far end of the interconnects is

$$\mathbf{V}_r = \mathbf{H} \mathbf{V}_{in} \quad (43)$$

$$\mathbf{H} = (\mathbf{R}_d \mathbf{C}_p + s \mathbf{R}_d \mathbf{D}_p \mathbf{C}_l + \mathbf{A}_p + s \mathbf{B}_p \mathbf{C}_l)^{-1} \quad (44)$$

where \mathbf{H} is the transfer function matrix. The $ABCD$ matrices of the coupled transmission lines are

$$\mathbf{A}_p = \mathbf{M} \hat{\mathbf{A}}_p \mathbf{M}^{-1} \quad (45)$$

$$\mathbf{B}_p = \mathbf{M} \hat{\mathbf{B}}_p \mathbf{M}^T \quad (46)$$

$$\mathbf{C}_p = (\mathbf{M}^T)^{-1} \hat{\mathbf{C}}_p \mathbf{M}^{-1} \quad (47)$$

$$\mathbf{D}_p = (\mathbf{M}^T)^{-1} \hat{\mathbf{D}}_p \mathbf{M}^T. \quad (48)$$

In general, \mathbf{M} is a matrix function of s and cannot be expressed in closed form [10]. Furthermore, the matrix inverse operation in (44) does not permit an analytic expression (or an analytic low-order approximation) of the transfer function to be obtained.

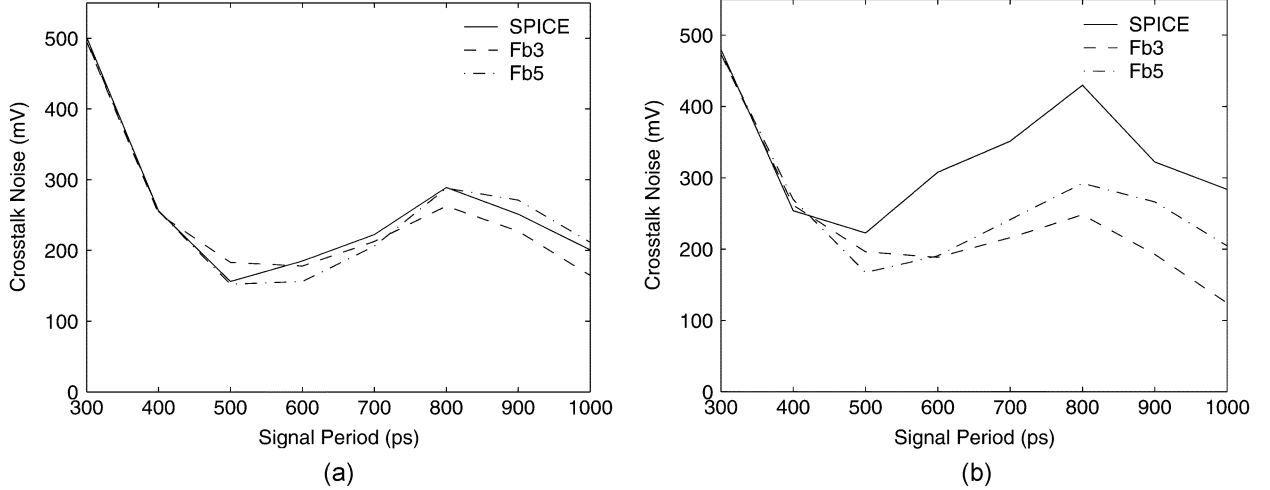


Fig. 19. Crosstalk noise in a five line system versus the period of the excitation signal, (a) victim 2 and (b) victim 5. The circuit and signal parameters are $l = 2$ mm, $\tau = 30$ ps, and $V_{dd} = 1.5$ V.

Conventional inverse Laplace transform-based methods [2]–[6], which assume a step or ramp input, can no longer be used. The proposed model, which assumes a periodic input signal, remains valid, since the solution of (44) is only required at certain discrete frequencies (e.g., the harmonic frequencies of the input signal), and can be solved numerically at each frequency. When N is less than five, closed-form solutions exist [12] to calculate \mathbf{M} and \mathbf{Q} . For a larger N , numerical methods have to be used, and the computing complexity increases. When $s = 0$, \mathbf{H} becomes an identity matrix. Since no approximation is made in this derivation, (44) is the exact transfer function of a coupled multiconductor system. For the structure shown in Fig. 16, the accuracy of (44) is illustrated in Fig. 17. The interconnect parameters are

$$\mathbf{R} = \text{diag}(9.0, 18.2, 9.1, 18.2, 9.0) \text{ m}\Omega/\mu\text{m} \quad (49)$$

$$\mathbf{L} = \begin{bmatrix} 1.54 & 1.28 & 1.14 & 1.06 & 1.00 \\ 1.28 & 1.61 & 1.28 & 1.14 & 1.06 \\ 1.14 & 1.28 & 1.54 & 1.28 & 1.14 \\ 1.06 & 1.14 & 1.28 & 1.61 & 1.28 \\ 1.00 & 1.06 & 1.14 & 1.28 & 1.54 \end{bmatrix} \text{ pH}/\mu\text{m} \quad (50)$$

$$\mathbf{C} = \begin{bmatrix} 207 & -56 & 0 & 0 & 0 \\ -56 & 187 & -56 & 0 & 0 \\ 0 & -56 & 232 & -56 & 0 \\ 0 & 0 & -56 & 187 & -56 \\ 0 & 0 & 0 & -56 & 207 \end{bmatrix} \text{ aF}/\mu\text{m}. \quad (51)$$

For simplicity, capacitive coupling is assumed to exist only between adjacent lines. The other circuit parameters are $l = 2$ mm, $\mathbf{R}_d = \text{diag}(50, 30, 40, 50, 30) \Omega$, and $\mathbf{C}_l = \text{diag}(50, 100, 80, 80, 50)$ fF. In Fig. 17, $H_{i,k}$ represents the amplitude transfer function from the input of line k to the far end of line i . Upon obtaining the transfer coefficient at each harmonic frequency, the output signal can be determined in the same manner as in (7). The time-of-flight t_f of a multiconductor system is the minimum t_f of all of the wave modes. In this multiconductor model, no constraints are made on the interconnect parameters, making the solution of general utility. With a periodic ramp signal applied to line 1, the far-end

response from Fb3 and Fb5 is compared with SPICE in Fig. 18. The model is implemented by Matlab and the runtime for this example is about 17 ms on a SunBlade1000 workstation. The time required by SPICE to simulate one clock period (500 ps) is 7.7 s.

C. Model Verification and Discussion

For simplicity, only one aggressor is considered in the following examples. Multi-aggressor circuits can be solved by applying superposition. The maximum crosstalk noise determined by the Fourier series-based model is compared with SPICE in Table VII for several cases: the five line system evaluated in Section IV-B with interconnect lengths of 1 and 2 mm, and a three-line system (composed of lines 1–3) with the same geometric characteristics as the five-line system. In these systems, line 1 is the aggressor, and all of the other lines are quiet victims (represented as V2–V5 in Table VII).

As shown in Table VII, Fb3 provides limited accuracy in multiconductor systems. Note that the error reaches 40% as compared with SPICE. This result is not surprising since, as shown in Fig. 17, the magnitude of the transfer function of the victims is small at low frequencies. Thus, the high-frequency components are comparable or greater than the low-frequency components at the output, and are, therefore, not negligible. By including one more frequency component, Fb5 is significantly more accurate, exhibiting an average error of 4.3%.

Note in Table VII that the noise on the victims far from the aggressor can be greater than the noise on a nearby victim. Since capacitive coupling is assumed to exist only between adjacent lines, the noise on the far victims is primarily due to inductive coupling. This noise, however, is not just a simple function of the mutual inductance between the victim and the aggressor, but a complicated function of all of the circuit parameters. Since no dedicated shield lines or ground planes are assumed, the mutual inductance decreases slowly with distance. By including the effects of different driver resistances and load capacitances of the victims, a victim line with a small mutual inductance can produce greater noise than a victim line with a large mutual inductance. Furthermore, with a rising edge on the aggressor, capaci-

tive coupling produces a positive response on the victim, while inductive coupling produces an oscillating response beginning with a negative peak. These two effects can cancel each other, thereby lowering the noise voltage on the nearby victim line.

Also note that there are peaks in the amplitude frequency response of the victims, as shown in Fig. 17. If a harmonic frequency at the input is located on or near a peak, the noise on that victim will be large. The crosstalk noise, therefore, depends not only on the transition time but also on the period of the excitation signal. For example, in Fig. 17, $H_{2,1}$ has a peak at 3.6 GHz. The third harmonic frequency of a 1.25 GHz ramp signal ($T = 0.8$ ns) is 3.75 GHz, which is near that peak. With the same transition time rate $\tau/T = 0.1$, the maximum coupling noise produced by the 1.25-GHz signal is 246.9 mV, which is 61.1% greater than the noise produced by a 2-GHz signal, although the 1.25-GHz signal has a longer transition time. The relationship between the maximum crosstalk noise and the signal period is shown in Fig. 19. The high-frequency response (which is ignored in the model) on the fifth victim is relatively more important as compared with the second victim. The proposed model therefore exhibits a larger error on the fifth victim than on the second victim.

In integrated circuits, since logic gates have a low pass filtering property [21], the sharp spikes in the time domain waveforms normally cannot cause a circuit to fail. The Fourier series-based model, which ignores these high frequency effects, is therefore an effective method to analyze crosstalk noise.

V. CONCLUSION

By exploiting a Fourier series representation of a typical on-chip signal, an analytic time-domain solution for an RLC interconnect is shown to be an effective modeling strategy, which can be used in early circuit-level design stages to estimate the time characteristics of periodic signals. Expressions for the 50% delay and the overshoots/undershoots are also provided and are within 11% of SPICE over a wide range of circuit parameters. The single-line model is applied to tree structures and a tree model with linear computational complexity is obtained, which is shown to be an effective analysis tool for clock distribution networks. Combined with the modal analysis-based decoupling method, the proposed model is also extended to coupled interconnect systems to analyze crosstalk noise. For three harmonic frequencies (Fb5), the average error is 4.3%. It is also noted that crosstalk noise depends not only on the transition time but also on the period of the excitation signal.

REFERENCES

- [1] Y. I. Ismail and E. G. Friedman, "Effects of inductance on the propagation delay and repeater insertion in VLSI circuits," *IEEE Trans. VLSI Syst.*, vol. 8, no. 2, pp. 195–206, Apr. 2000.
- [2] J. A. Davis and J. D. Meindl, "Compact distributed RLC interconnect models—Part I: Single line transient, time delay, and overshoot expressions," *IEEE Trans. Electron Devices*, vol. 47, no. 11, pp. 2068–2077, Nov. 2000.

- [3] R. Venkatesan, J. A. Davis, and J. D. Meindl, "A physical model for the transient response of capacitively loaded distributed RLC interconnects," in *Proc. ACM/IEEE Design Automation Conf.*, Jun. 2002, pp. 763–766.
- [4] A. B. Kahng and S. Muddu, "An analytical delay model for RLC interconnects," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 16, no. 12, pp. 1507–1514, Dec. 1997.
- [5] A. B. Kahng, K. Masuko, and S. Muddu, "Analytical delay models for VLSI interconnects under ramp input," in *Proc. ACM/IEEE Int. Conf. Computer-Aided Design*, Nov. 1996, pp. 30–36.
- [6] K. Banerjee and A. Mehrotra, "Accurate analysis of on-chip inductance effects and implications for optimal repeater insertion and technology scaling," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2001, pp. 195–198.
- [7] Y. Ismail, E. G. Friedman, and J. L. Neves, "Equivalent Elmore delay for RLC trees," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 19, no. 1, pp. 83–97, Jan. 2000.
- [8] L. T. Pillage and R. A. Rohrer, "Asymptotic waveform evaluation for timing analysis," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 9, no. 4, pp. 352–366, Apr. 1990.
- [9] F. Romeo and M. Santomauro, "Time-domain simulation of n coupled transmission lines," *IEEE Trans. Microwave Theory Tech.*, vol. 35, no. 2, pp. 131–137, Feb. 1987.
- [10] S. Lin and E. Kuh, "Transient simulation of lossy interconnects based on the recursive convolution formulation," *IEEE Trans. Circuits Syst.*, vol. 39, no. 11, pp. 879–892, Nov. 1992.
- [11] L. Yin and L. He, "An efficient analytical model of coupled on-chip RLC interconnects," in *Proc. IEEE Design Automation Conf. Asian South Pacific*, Jan. 2001, pp. 385–390.
- [12] J. Chen and L. He, "A decoupling method for analysis of coupled RLC interconnects," in *Proc. ACM Great Lakes Symp. VLSI*, Apr. 2002, pp. 41–46.
- [13] L. N. Dworsky, *Modern Transmission Line Theory And Applications*. New York: Wiley, 1979.
- [14] A. B. Kahng and S. Muddu, "Optimal equivalent circuits for interconnect delay calculations using moments," in *Proc. Eur. Design Automation Conf.*, Sep. 1994, pp. 164–169.
- [15] M. Kamon, M. J. Tsuk, and J. White, "Fasthenry: A multipole accelerated 3-D inductance extraction program," *IEEE Trans. Microwave Theory Tech.*, vol. 42, no. 9, pp. 1750–1758, Sep. 1994.
- [16] K. Nabors and J. White, "Fastcap: A multipole accelerated 3-D capacitance extraction program," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 10, no. 11, pp. 1447–1459, Nov. 1991.
- [17] K. T. Tang and E. G. Friedman, "Lumped versus distributed RC and RLC interconnect impedance," in *Proc. IEEE Midwest Symp. Circuits Syst.*, Aug. 2000, pp. 136–139.
- [18] T. J. Bromwich and T. M. MacRobert, *An Introduction to the Theory of Infinite Series*, 3rd ed. New York: Chelsea, 1991.
- [19] R. Escovar and R. Suaya, "Optimal design of clock trees for multigigahertz applications," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 23, no. 3, pp. 352–366, Mar. 2004.
- [20] J. Zhang and E. G. Friedman, "Crosstalk noise model for shielded interconnects in VLSI-based circuits," in *Proc. IEEE Int. SOC Conf.*, Sep. 2003, pp. 243–244.
- [21] S. H. Choi, B. C. Paul, and K. Roy, "Dynamic noise analysis with capacitive and inductive coupling," in *Proc. IEEE Int. Conf. VLSI Design*, Jan. 2002, pp. 65–70.



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