# Latching Characteristics of a CMOS Bistable Register

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***Abstract*—Closed-form solutions describing the output response of a CMOS bistable register are presented. From these results, the fundamental latching behavior of a CMOS register is developed in terms of its physical and circuit characteristics. Necessary and sufficient conditions for latching data are described in terms of small signal circuit parameters. From these necessary and sufficient conditions, the limiting requirement for latching, which provides the minimum set-up time and conditions for defining the onset of metastability, is presented and verified.**

## I. Introduction

In this paper the fundamental limitations of latching data in a pipelined synchronous digital system are presented. Specifically, the minimum latch time (or set-up time) of a CMOS bistable register is quantitatively described. The time for the final register of a data path to latch is one of the primary delay components within a synchronous data path. To the author's knowledge, the work described in this paper represents the first effort to quantify this delay value in terms of physically meaningful parameters. Up to now, the minimum set-up time of a register has been extracted directly from circuit simulation, where a designer iteratively determines at what relative time point of the input data signal (with respect to the clock signal), the register fails to successfully latch the input signal. With the results described in this paper, the basic regenerative latching phenomena of a CMOS bistable register is both qualitatively and quantitatively described and the fundamentally limiting condition for ensuring that a data signal is latched within a CMOS bistable register is presented. The results described herein provide the theoretical framework for understanding an important fundamental limitation to the processing of signal waveforms in high-speed synchronous pipelined digital systems.

Early work in the area of sensing and latching input waveforms has focused on the design of sense amplifiers in memory circuits. Lynch and Boll [1] derive an optimal waveform shape for latching data into a two transistor (with pull-ups) sense amplifier cell. Recently, Yuan and Liou [2] expanded their work by considering effects such as capacitive coupling on the waveform shape required for latching data in a DRAM sense amplifier. In this paper, the optimal latching requirements of a different, though related and very common circuit structure, a CMOS bistable register, is described. The latching characteristics of a data signal in a bistable register have also been investigated in the context of metastability analysis [3]–[8]. In this phenomena, the voltage levels and the temporal coincidence of the input signals determine the likelihood and duration of a register entering a metastable state. The resolution time of a metastable register is further affected by the shape of the input waveforms. The slower the input waveforms, the longer the time required for the register to resolve its state and leave the metastable state [9]. In [10], the latching behavior of a CMOS register based on waveform considerations is described. This paper is similar to the related research on metastability in that the set of conditions which define the onset of metastability are determined; in addition, necessary and sufficient conditions for latching data into a bistable register are also determined, defining the minimum temporal requirement for latching (i.e., the set-up time of the register).

A register can respond to an input signal in one of three different ways: 1) the data signal is successfully latched into the register; 2) the data signal is not successfully latched into the register and the register returns to its initial state; and 3) the register enters a state of metastability in which neither binary state is reached within a time period consistent with the normal operation of the register. The register will remain in this tenuous state of equilibrium until some circuit parameter varies sufficiently to drive the state of the register into one of the two binary states [11]. Thus, this state of metastability is categorized as a type of reliability problem. The register could easily remain in this state for milliseconds, thereby forcing the overall system to function incorrectly.

The basic circuit configuration of the bistable NAND gate latch is described in Section II of this paper. An overview of the circuit operation of the CMOS bistable latch driven by clock and data ramp signals is discussed in Section III. The circuit behavior of the latch can be broken up into four separate regions of operation. Each of these regions is analyzed in detail, and small signal closed-form solutions of the output response for each region are summarized in Section IV. The closed-loop regenerative latch behavior occurs in the third region of operation. This permits the development of necessary and sufficient conditions for latching data into a register. From these conditions, the fundamental limiting requirement for latching data into a CMOS bistable register is presented and verified through simulation. This relation also provides a limiting definition of metastability. These concepts are described in Section V of this paper. Some concluding remarks are made in Section VI. Finally, the complete closed form solution of region 3 is provided in the appendix.

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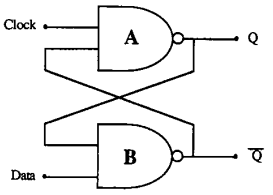


Fig. 1. Bistable NAND gate register.

## II. Bistable NAND Gate Configuration

A primary form of a register element is the bistable latch configuration which can be constructed from either two NAND gates or two NOR gates. Either circuit performs the basic latching operation upon which other more complicated types of latches and registers can be constructed. The cross-coupled NAND gate implementation of the bistable latch, shown in Fig. 1, is the fundamental element of a flip-flop circuit. The NAND gate configuration of the latch has been chosen instead of the NOR gate version, since its performance is greater in CMOS technology (due to the higher mobilities of the serial N-channel devices than the serial P-channel devices) and is therefore more commonly used. However, all physical theory and algorithmic solutions described in this paper are equally applicable to a cross-coupled NOR gate implementation of a CMOS bistable register. Classical large signal Shichman–Hodges MOSFET I-V equations [12] are used to derive the small signal circuits and conductance parameter values described in Section IV. In order to make the solution of the problem tractable, the assumption is made that the output load capacitances of both NAND gates dominate any internal device dependent parasitic capacitances, and therefore these device capacitances are lumped into the output load capacitance of both NAND gates.

A CMOS implementation of the bistable NAND gate structure has been chosen to evaluate how data is fundamentally performance limited by the ability to latch data into a register. The CMOS bistable register circuit is shown in Fig. 2. The clock signal drives the input of one NAND gate (labeled with subscript "A" in Fig. 2); the data signal is the input to the second NAND gate (labeled with subscript "B" in Fig. 2). The other input of each NAND gate is furnished by the output signal of its complementary NAND gate. Given an initial voltage at $V_1$ and its complement at $V_2$, the input data and clock signal are chosen so as to maintain or flip the output logic state. Once the new state of the register is reached and necessary and sufficient conditions for latching are satisfied, the input data is considered to have been latched into the register.

## III. Latching Data into a CMOS Register

In order to latch data into a register, the clock and data signals must appear at the input of the register at the correct relative time and at the correct voltage magnitudes. These time and voltage requirements are described in analytical form in Sections IV and V of this paper. In this analysis, the input clock and data waveforms are assumed to behave as ramp

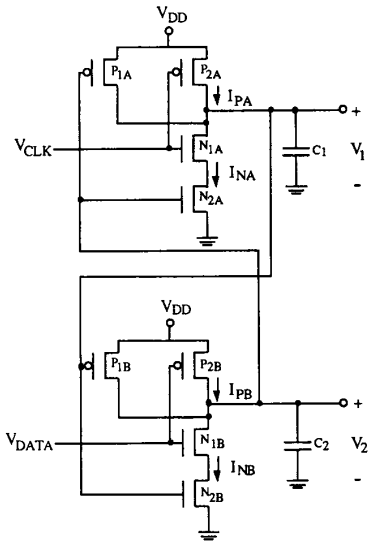


Fig. 2. CMOS implementation of bistable register.

signals, not as step inputs, so as to better represent the effects of the waveform shape on the output response.

The initial conditions of $V_1(0) = G_{ND}$ and $V_2(0) = V_{DD}$ have been chosen to exemplify the latching phenomenon, where $G_{ND}$ and $V_{DD}$ are the lower and upper power supply voltages, typically 0 V and 5 V, respectively. Assuming the clock signal $V_{CLK}$ is at $V_{DD}$ and the data signal $V_{DATA}$ is at $G_{ND}$, the circuit exists in a restoring equilibrium state. In order to change the polarity of the output voltages at $V_1$ and $V_2$, both the clock and the data input signals must switch. The clock signal must decrease from $V_{DD}$, and the data signal must increase from $G_{ND}$.

As shown in Fig. 2, as $V_{CLK}$ decreases from $V_{DD}$ to $V_{DD} + V_{TP}$, where $V_{DD}$ is the power supply voltage and $V_{TP}$ is the threshold voltage of the P-channel transistor, no current will flow in the upper NAND gate, since both of the P-channel transistors are cutoff. Once $V_{CLK}$ equals $V_{DD} + V_{TP}$, $P_{2A}$ turns on and enters the saturation region. This permits current to flow within the upper NAND gate. Once $I_{PA}$ becomes greater than $I_{NA}$, $V_1$ will increase. When $V_1$ equals $V_{TN}$, the threshold voltage of the N-channel transistor, the lower N-channel transistor of the lower NAND gate ($N_{2B}$) turns on. If $V_{DATA}$ is greater than $V_{TN}$ of the top transistor plus $V_{DS}$ of the lower transistor, the lower NAND gate will also conduct current. Assuming these conditions exist and $V_{CLK}$ continues to decrease (thereby increasing $V_1$), the bistable NAND gate register will enter the regenerative latch mode. Thus, as $V_1$ increases above $V_{TN}$ and assuming $V_{DATA}$ remains above $V_{TN}$, the N-channel tree of the lower transistor will sink current to ground. Once $I_{NB}$, shown in Fig. 2, becomes greater than $I_{PB}$, $V_2$ will decrease from its equilibrium potential of $V_{DD}$ volts. As $V_2$ decreases below $V_{DD} + V_{TP}$, $P_{1A}$ turns on, and this further accelerates the rising voltage at $V_1$, which in turn further decreases $V_2$. This closed loop regenerative action permits the bistable register to respond quickly to its changing input signals and to latch the input data, and, in effect, to

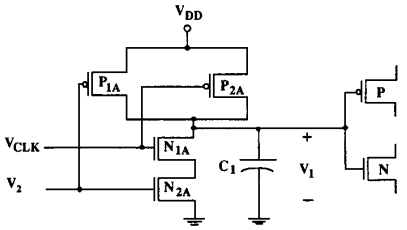


Fig. 3. Circuit diagram of upper NAND gate in region 1.

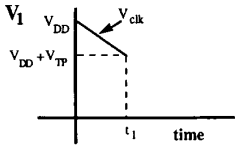


Fig. 4. Region 1 timing diagram.

change the state of the register. Finally, as $V_1$ approaches $V_{DD}$, $V_{DS}$ across both of the P-channel transistors in the upper NAND gate becomes very small, and the amount of output voltage change due to a change in input voltage decreases until the regenerative loop becomes decoupled. The final region of operation is a nonregenerative open loop in which the P-channel transistors charge the output capacitor $C_1$ up to $V_{DD}$. Each of these four regions of operation are quantitatively described in the following section.

## IV. Regions of Operation of Bistable Register

The response of the bistable register to its changing input signals can be broken down into four separate regions. Each region describes the bistable register operating under different circuit conditions, and therefore each region has a different output response.

### *Region 1*

As $V_{CLK}$ decreases from $V_{DD}$ to $V_{DD} + V_{TP}$, no current can flow through the upper NAND gate (see Fig. 3) since both P-channel transistors are in cutoff, $P_{2A}$ due to $V_{CLK} \geq V_{DD} + V_{TP}$ and $P_{1A}$ due to $V_2 \geq V_{DD} + V_{TP}$, and $V_1$ is at the same potential as the sources of the two N-channel transistors. Thus, region 1 represents the time required for $V_{CLK}$ to reach $V_{DD} + V_{TP}$ and turn on $P_{2A}$, thereby permitting current to flow. Throughout this region $V_1$ remains at 0 V, as shown in Fig. 4, and the time delay $t_1$ of this region is given by (1):

$$t_1 = \left| \frac{V_{TP}}{k_c} \right| \tag{1}$$

where $k_c$ is the decreasing rate of change of the clock signal in volts per second and $V_{TP}$ is negative for an enhancement mode P-channel transistor.

### *Region 2*

Once $V_{CLK}$ decreases below $V_{DD} + V_{TP}$, current will flow between $V_{DD}$ and ground. As $V_{CLK}$ decreases further, the current supplied by $P_{2A}$ will become greater than the current sunk by the N-channel tree. Once this occurs, $V_1(t)$ will begin to rise. In this region, the bistable NAND gate register can be represented by a single NAND gate with one changing input (since $V_2 = V_{DD}$), as shown in Fig. 5, where $V_{x1}$ is $V_{DS}$ across the lower N-channel transistor, $N_{1A}$. The circuit of Fig. 5 can be represented by the small signal model shown in Fig. 6, where $v_c$ represents the incremental change in $V_{CLK}$ and $v_1$ represents the incremental change in $V_1$.

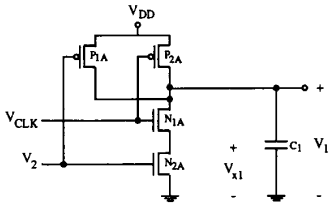


Fig. 5. Region 2 circuit configuration.

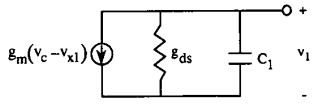


Fig. 6. Small signal model of region 2.

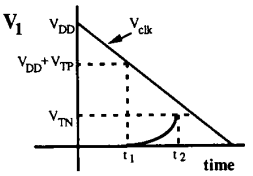


Fig. 7. Region 2 timing diagram.

From this model, $V_1(t)$ can be determined for a ramp input clock signal decreasing at a rate of $k_c$ volts per second. $V_1(t)$ for region 2 is

$$V_1(t) = k_c \frac{AC_1}{B^2}\left(e^{-Bt/c_1} + \frac{Bt}{C_1} - 1\right). \tag{2}$$

Note that in region 2, $V_1(t)$ increases from $G_{ND}$ and terminates at $V_{TN}$ volts, as shown in Fig. 7. Assuming $V_{DATA}$ is greater than $V_{TN}$, the circuit will enter region 3, the regenerative region of operation. $A$ and $B$ in (2) represent the transconductance and output conductance of the single NAND gate ($A$) in region 2, respectively, and are given by (3) and (4), respectively:

$$A = g'_m + g_{mp} - \frac{g'_m g_{mn}}{g_{n1} + g_{n2} + g_{mn}} \tag{3}$$

$$B = g_{ds} - \frac{g'_m g_{n1}}{g_{n1} + g_{n2} + g_{mn}} \tag{4}$$

where

$$g'_m = \frac{g_{mn} g_{n2}}{g_{n1} + g_{n2}} \tag{5}$$

$$g_{ds} = \frac{g_{n1} g_{n2}}{g_{n1} + g_{n2}}. \tag{6}$$

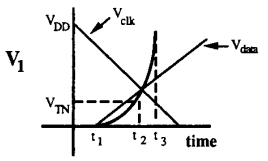


Fig. 8. Region 3 timing diagram.

$g_{mn}$ and $g_{mp}$ are the transconductance of the N-channel tree and the P-channel tree of NAND gate $A$, respectively, when driven by the input clock signal. $g_{n1}$ and $g_{n2}$ are the output conductances of the two serial N-channel transistors of NAND gate $A$. For added ease and simplicity, in (3)–(6) the subscript $a$ is not included since in region 2 only NAND gate $A$ is considered.

*Region 3*

Once $V_1$ reaches $V_{TN}$ volts, $N_{2B}$ is turned on (see Fig. 2). If $V_{DATA}$ is also greater than $V_{TN}$ of the top N-channel transistor plus $V_{DS}$ of the lower N-channel transistor ($V_{x2}$), $N_{1B}$ will also be turned on; with both on, current can flow between $V_{DD}$ and ground. At some point in time, depending upon the transistor characteristics and the magnitude of $V_{DATA}$ and $V_1$, the N-channel tree will sink more current than the P-channel tree will source. At this point, $V_2(t)$ will decrease from $V_{DD}$ volts. Once $V_2$ decreases below $V_{DD} + V_{TP}$, $P_{1A}$ will turn on and source additional current, furthering the rate of increase of $V_1$, as shown in Fig. 8. This, in turn, will enhance the current sinking capability of the N-channel tree of the lower NAND gate, further decreasing $V_2$. Herein lies the closed loop regenerative mode of operation inherent to the bistable NAND gate circuit configuration and fundamental to the latching behavior of a register. Note that the circuit in this region operates as a two time constant system.

At a certain operating point, the data is fully latched into the register and the clock input signal can be returned to $V_{DD}$ and the state of the register will still enter its correct state ($V_1 = V_{DD}$ and $V_2 = 0$). This irreversible latching point represents the limiting ability to latch data into a register and is further explored in Section V of this paper.

This concept of an irreversible latching point is similar to that described by Kim *et al.* in [7], where they show that the resolving time of the metastable register is inversely proportional to the gain-bandwidth of the positive feedback system. Thus, the point at which the register irreversibly latches is dependent upon the gain of the positive feedback system during region 3.

The circuit configuration of region 3 is shown in Fig. 9. This regenerative circuit can be represented by the small signal models depicted in Figs. 10 and 11, where Fig. 10 represents the small signal model for the upper NAND gate $A$ and Fig. 11 represents the small signal model for the lower NAND gate $B$. Note that Figs. 10 and 11 are coupled together through $v_1$ and $v_2$.

In the regenerative mode of region 3 with a decreasing ramp shaped clock input signal, $V_1(t)$ is composed of three terms [as shown in (7)]: one due to the initial condition of region 3, where $V_{23}(0) = V_{TN}$; the second due to the input clock signal; and the third due to the input data signal.

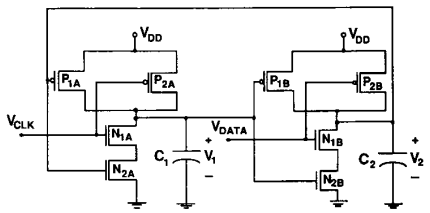


Fig. 9. Circuit diagram of region 3.

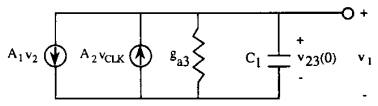


Fig. 10. Small signal model of NAND gate $A$ in region 3.

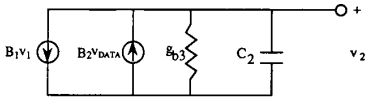


Fig. 11. Small signal model of NAND gate $B$ in region 3.

$$V_1(t) = V_{1A} + V_{1C} + V_{1D} \tag{7}$$

The complete solution to (7) is provided in the appendix.

Each of the transconductance and output conductance terms shown in Figs. 10 and 11 require definition. $A_1$ and $B_1$ represent the transconductance of the two feedback output voltages, $V_2$ and $V_1$, respectively. $A_2$ and $B_2$ are the transconductances of the input clock and data signals, respectively. $A_1$, $B_1$, $A_2$, and $B_2$ are shown in (8)–(11) in terms of their small signal parameters:

$$A_1 = \frac{g_{mn1a}g_{mn2a}}{g_{n2a} + g_{mn1a}} - g_{mp1a} \tag{8}$$

$$B_1 = \frac{g_{mn1b}g_{mn2b}}{g_{n2b} + g_{mn1b}} - g_{mp1b} \tag{9}$$

$$A_2 = \frac{g_{mn1a}g_{n2a}}{g_{mn1a} + g_{n2a}} - g_{mp2a} \tag{10}$$

$$B_2 = \frac{g_{mn1b}g_{n2b}}{g_{mn1b} + g_{n2b}} - g_{mp2b} \tag{11}$$

where $g_{n2a}(g_{n2b})$ is the output conductance of the lower N-channel transistor of NAND gate $A$ (NAND gate $B$), $g_{mn1a}$ and $g_{mn2a}$ ($g_{mn1b}$ and $g_{mn2b}$) are the transconductances of the top and bottom N-channel transistors of NAND gate $A$ (NAND gate $B$), and $g_{mp1a}$ and $g_{mp2a}$ ($g_{mp1b}$ and $g_{mp2b}$) are the transconductances of the two P-channel transistors of NAND gate $A$ (NAND gate $B$), as shown in Figure 9.

The output conductances of NAND gate $A$ and NAND gate $B$ in region 3 are given in (12) and (13):

$$g_{a3} = 0 \tag{12}$$

$$g_{b3} = g_{p1b} + g_{p2b} \tag{13}$$

where $g_{p1b}$ and $g_{p2b}$ are the output conductances of the two parallel P-channel transistors of NAND gate $B$. Since in region 3 all of the ON transistors in the upper NAND gate ($A$) are

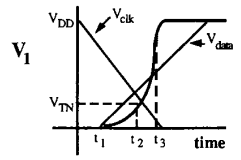


Fig. 12. Region 4 timing diagram.

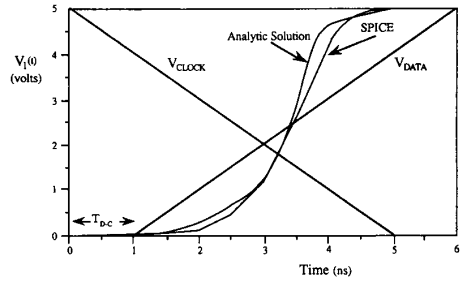


Fig. 13. Transient response of bistable register.

saturated and the channel length modulation $\lambda$ is assumed to be zero, $g_{a3}$ is equal to zero.

*Region 4*

As $V_1$ increases toward $V_{DD}$ and as $V_2$ decreases toward ground, $V_{DS}$ across $P_{1A}$, $P_{2A}$, $N_{1B}$, and $N_{2B}$ becomes very small, and both $A_1$ and $A_2$ approach zero. This breaks the regenerative loop of region 3, the two NAND gates become decoupled from each other, and the bistable register becomes once again an open loop single time constant system in which the P-channel transistors of NAND gate $A$ charge the capacitor $C_1$ up to $V_{DD}$ (see Fig. 12). Equations (14) and (15) define $V_1(t)$ within region 4, where $V_{34}(0)$ is the initial condition of region 4.

$$V_1(t) = V_{DD} - [V_{DD} - V_{34}(0)]e^{-g_{a4}t/C_1} \tag{14}$$

and the output conductance of NAND gate $A$ in region 4 is

$$g_{a4} = g_{p1a} + g_{p2a} \tag{15}$$

and $g_{p1a}$ and $g_{p2a}$ are the output conductances of the two parallel P-channel transistors of NAND gate $A$.

*Register Output Waveform*

Fig. 13 shows the output voltage waveform at node $V_1$ of the bistable register for an input clock signal decreasing at 1 V/ns and a data signal increasing at 1 V/ns skewed from the clock signal, $T_{D-C}$, by 1 ns. This analytically derived output waveform is compared to a waveform generated from the SPICE circuit simulator program [13] using Level 2 I-V MOSFET equations with the same circuit, geometric, and process characteristics. In particular, note the high gain in region 3. Close agreement between the analytical solution and SPICE within each region is apparent. A BASIC program which generates the output waveform for any clock signal fall time, data signal rise time, data-to-clock timing skew, as well as $K'_p$, $K'_n$, and geometric W/L ratio was developed to calculate the bistable register output response.

## V. Conditions for Latching

As noted earlier, necessary and sufficient conditions are required to irreversibly latch data into a bistable register. This latch condition, which occurs in region 3, permits the development of fundamental limiting relationships which define whether the bistable register will latch, not latch, or become metastable. Once a register has correctly latched, the clock signal can be returned to $V_{DD}$ and still the register will maintain its correct state. The time required to satisfy these limiting conditions is the minimum necessary time for a CMOS bistable register to latch, assuming a given set of input signal, geometric, and process conditions.

*Necessary and Sufficient Conditions for Latching*

Inequalities (16) through (19) provide the four necessary and sufficient conditions for latching data into a bistable register:

$$V_{DD} + V_{TP} > V_{CLK} \tag{16}$$

$$V_{TN} + V_{x2} < V_{DATA} \tag{17}$$

$$A_1V_2 + A_2V_{CLK} > 0 \tag{18}$$

$$B_1V_1 + B_2V_{DATA} > 0. \tag{19}$$

$V_{X2}$ is the voltage across $N_{2B}$ in the lower NAND gate ($B$). The terms $A_1$, $A_2$, $B_1$, and $B_2$ are the transconductance parameters described in region 3 and given as (8)–(11). Inequality (18) states that the P-channel tree in NAND gate $A$ sources more current than the N-channel tree in NAND gate $A$ sinks, thereby increasing $V_1$. Inequality (19) states that the N-channel tree in NAND gate $B$ sinks more current than the P-channel tree in NAND gate $B$ sources, thereby decreasing $V_2$. If these four conditions are satisfied for all operating points within region 3, the bistable register will latch.

*Limiting Requirement for Latching*

Inequality (18) provides the fundamentally limiting condition for latching. If in NAND gate $A$, the P-channel tree sources more current than the N-channel tree sinks, $V_1$ will increase. As $V_1$ increases, it turns on $N_{2B}$ more strongly, increasing $I_{NB}$ of NAND gate $B$, thereby decreasing $V_2$. This, in turn, further turns on $P_{1A}$ which increases $V_1$. Thus, the transconductance term $A_1$, used in (18) and defined in (8), contains the limiting condition for latching.

To further exemplify the latching requirement, consider the situation, shown in Fig. 14, where the clock signal $V_{CLK}$ decreases from $V_{DD}$. If the limiting condition for latching can be satisfied before $V_{CLK}$ reaches 0 V, then the clock waveform can be returned to $V_{DD}$ before it reaches 0 V while still successfully latching the data signal. The minimum value of voltage that $V_{CLK}$ reaches just before it returns to $V_{DD}$ is described as $V_{CLK}(\min)$. Once $V_{CLK}(\min)$ is reached (see Fig. 14) and the clock signal is returned to $V_{DD}$, $V_2$ will continue to decrease further from $V_{DD}$. If at the operating point, $V_{CLK} = V_{DD} + V_{TP}$ ($P_{2A}$ becomes cutoff), the current supplied by $P_{1A}$ (and driven by $V_2$) is larger than the current sunk by the N-channel tree of NAND gate $A$, thereby maintaining a monotonically increasing voltage at $V_1$, the bistable register will latch. The time for $V_{CLK}$ to decrease

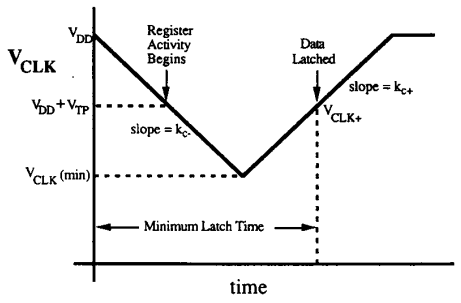


Fig. 14. Timing diagram of limiting condition for latching.

TABLE I
EXAMPLE OF LIMITING LATCH CONDITION

| $V_{DATA}$ | $g_{mp}$ | $g_{mn}$ | Latch? |
|---|---|---|---|
| 2.55 volts | $6.578\times10^{-4}$ Ʊ | $6.603\times10^{-4}$ Ʊ | no |
| 2.60 volts | $7.907\times10^{-4}$ Ʊ | $7.907\times10^{-4}$ Ʊ | breakpoint |
| 2.65 volts | $1.548\times10^{-3}$ Ʊ | 0 | yes |

from $V_{DD}$ to $V_{CLK}(\min)$ and return to $V_{DD} + V_{TP}$ is the minimum amount of time (i.e., the minimum latch time) for the data to successfully latch into the bistable register. The minimum latch time is the minimum set-up time of the register. The condition for ensuring that the bistable register will latch can be represented by the inequality

$$A_1V_2 > A_2V_{CLK} \text{ and } A_1V_2 \text{ is a positive quantity.} \quad (20)$$

In terms of the small signal parameters of (8), (20) can be presented as

$$g_{mp1a} > g_{mn} = \left.\frac{g_{mn1a}g_{mn2a}}{g_{n2a} + g_{mn1a}}\right|_{V_{CLK+}=V_{DD}+V_{TP}} \quad (21)$$

where $V_{CLK+}$ represents the operating point at which $V_{CLK} = V_{DD} + V_{TP}$ after reaching its minimum value and rising to $V_{DD} + V_{TP}$ (see Fig. 14). Equation (21) represents the fundamentally limiting condition for latching data into a CMOS bistable register.

Table I describes an example circuit which operates just at the latch breakpoint. One parameter, $V_{DATA}$, is varied to exemplify the limiting nature of (21). The other circuit characteristics are kept constant and are listed below:

$$V_{CLK}(\min) = 1.7 \text{ V}$$
$$K_p', K_n' = 4.316 \times 10^{-5} \text{ A/V}^2$$
$$k_{c-}, k_{c+} = 1 \text{ V/ns}$$
$$\text{W/L ratio} = 5.$$

Thus, Table I describes an experiment in which $V_{DATA}$ is perturbed over a small range of voltage, keeping all other conditions constant. For the case where (21) is not satisfied (i.e., $g_{mn} > g_{mp}$), the data signal will not successfully latch into the register. For the case where (21) is satisfied (i.e., $g_{mp} > g_{mn}$), the data signal latches successfully into the register. Finally, for the interesting breakpoint case, where $g_{mp}$ equals $g_{mn}$, the register enters what is effectively a metastable state [3]–[8]. As long as $g_{mn} = g_{mp}$, the register will remain metastable.

## VI. CONCLUSIONS

Closed-form solutions of each of the four regions of operation of a bistable register have been developed. Close agreement with a SPICE generated output response of a CMOS bistable register was shown. Necessary and sufficient conditions for latching data into a bistable register were developed. From these conditions, the limiting requirement for latching, not latching, and becoming metastable in a CMOS bistable register is defined. This result was corroborated by testing (21) at $V_{CLK+} = V_{DD} + V_{TP}$ with breakpoint conditions, and the result fully agreed with expectations. Thus, the limiting requirement for latching provides the minimum latch time (or set-up time) of a CMOS bistable register. With these results, fundamentally limiting conditions for analyzing the latching mechanism in a CMOS bistable register are quantitatively described.

## VII. APPENDIX
## COMPLETE SOLUTION OF $V_1(t)$ IN REGION 3

The output voltage $V_1(t)$ of NAND gate $A$ is given by (7) and repeated below as (A-1). Equation (A-1) is composed of three terms, one due to the initial condition of region 3, $V_{1A}$, one due to the input clock signal, $V_{1C}$, and one due to the input data signal $V_{1D}$:

$$V_1(t) = V_{1A} + V_{1C} + V_{1D}. \quad \text{(A-1)}$$

Each term is described individually below:

$$V_{1A}(t) = V_{23}(0)[R_{1A} + R_{2A} + R_{3A}] \quad \text{(A-2)}$$

$$R_{1A} = \frac{\left(\alpha_1 - \frac{g_{b3}}{C_2}\right)e^{-\alpha_1 t}}{\alpha_1(\alpha_2 - \alpha_1)} \quad \text{(A-3)}$$

$$R_{2A} = \frac{\left(\alpha_2 - \frac{g_{b3}}{C_2}\right)e^{-\alpha_2 t}}{\alpha_2(\alpha_1 - \alpha_2)} \quad \text{(A-4)}$$

$$R_{3A} = \frac{\frac{g_{b3}}{C_2}}{\alpha_1\alpha_2} \quad \text{(A-5)}$$

$$V_{1C}(t) = \frac{-A_2k_c}{C_1}\left[[(R_{1C} + R_{2C} + R_{3C})U(t)] - (R_{1C} + R_{2C} + R_{3C})\big|_{t=E/k_c} U\left(t - \frac{E}{k_c}\right)\right] \quad \text{(A-6)}$$

$$R_{1C} = \frac{\left(\frac{g_{b3}}{C_2} - \alpha_1\right)e^{-\alpha_1 t}}{\alpha_1^2(\alpha_2 - \alpha_1)} \quad \text{(A-7)}$$

$$R_{2C} = \frac{\left(\frac{g_{b3}}{C_2} - \alpha_2\right)e^{-\alpha_2 t}}{\alpha_2^2(\alpha_1 - \alpha_2)} \quad \text{(A-8)}$$

$$R_{3C} = \frac{\alpha_1\alpha_2\left(1 + \frac{g_{b3}}{C_2}t\right) - \frac{g_{b3}}{C_2}(\alpha_1 + \alpha_2)}{\alpha_1^2\alpha_2^2} \quad \text{(A-9)}$$

$$V_{1D}(t) = \frac{-A_1B_1k_D}{C_1C_2}\left[[(R_{1D} + R_{2D} + R_{3D})U(t)] - (R_{1D} + R_{2D} + R_{3D})\big|_{t=E/k_D} U\left(t - \frac{E}{k_D}\right)\right] \quad \text{(A-10)}$$

$$R_{1D} = \frac{e^{-\alpha_1 t}}{\alpha_1^2(\alpha_2 - \alpha_1)} \tag{A-11}$$

$$R_{2D} = \frac{e^{-\alpha_2 t}}{\alpha_2^2(\alpha_1 - \alpha_2)} \tag{A-12}$$

$$R_{3D} = \frac{\alpha_1\alpha_2 t - (\alpha_1 + \alpha_2)}{\alpha_1^2\alpha_2^2} \tag{A-13}$$

$$\alpha_1 = \frac{-\left(\frac{g_{a3}}{C_1} + \frac{g_{b3}}{C_2}\right) + \sqrt{\left(\frac{g_{a3}}{C_1}\right)^2 + \left(\frac{g_{b3}}{C_2}\right)^2 - 2\frac{g_{a3}g_{b3}}{C_1C_2} + 4\frac{A_1B_1}{C_1C_2}}}{2} \tag{A-14}$$

$$\alpha_2 = \frac{-\left(\frac{g_{a3}}{C_1} + \frac{g_{b3}}{C_2}\right) - \sqrt{\left(\frac{g_{a3}}{C_1}\right)^2 + \left(\frac{g_{b3}}{C_2}\right)^2 - 2\frac{g_{a3}g_{b3}}{C_1C_2} + 4\frac{A_1B_1}{C_1C_2}}}{2} \tag{A-15}$$

where $V_{23}(0)$ is the initial condition of region 3 and is equal to $V_{\mathrm{TN}}$, $k_c$ is the decreasing rate of change of the input clock signal, and $k_D$ is the increasing rate of change of the input data signal.

Thus, (A-1)–(A-15) describe the output voltage across $C_1$, $V_1(t)$, when the bistable register operates in the closed loop regenerative mode of region 3. Fig. 8 depicts the $V_1(t)$ waveform in region 3.

In region 3 all of the ON transistors in NAND gate A are saturated. Assuming channel length modulation is zero, $g_{a3}$ is equal to zero. Therefore, with this assumption, (A-14) and (A-15), which describe the two time constants of the bistable register system, become (A-16) and (A-17), respectively.

$$\alpha_1 = \frac{-\left(\frac{g_{b3}}{C_2}\right) + \sqrt{\left(\frac{g_{b3}}{C_2}\right)^2 + 4\frac{A_1B_1}{C_1C_2}}}{2} \tag{A-16}$$

$$\alpha_2 = \frac{-\left(\frac{g_{b3}}{C_2}\right) - \sqrt{\left(\frac{g_{b3}}{C_2}\right)^2 + 4\frac{A_1B_1}{C_1C_2}}}{2}. \tag{A-17}$$

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