Introduction to the Special Issue on Low Power Wireless Communications

THE WIRELESS communication explosion is upon us. This new technology enables global communication ranging from multimedia capable of video and audio, to cellular systems, one-way paging, and the new emerging PCS (personal communication system). The future of wireless communication is seemingly beyond imagination, whereby using an integrated system of low-orbit satellites, individuals will have access to a very large database of information, communication, and computation anywhere on the globe.

The complexity and portability of wireless systems places a stringent requirement on the total power consumption of signal processing and communication systems. The objective of this special issue of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: ANALOG AND DIGITAL SIGNAL PROCESSING is to provide a forum for both low power analog and digital signal processing circuits and systems issues that relate directly to wireless communication.

This wireless revolution started with the two-way radio system in the 1940's and exploded in the 1980's with the introduction of the analog mobile portable system (AMPS) cellular system. The greatest challenge for future wireless systems is two criteria: low power and low cost. With the increasing complexity of these wireless systems, and with carrier frequencies approaching 2–3 GHz for PCS, providing low power while maintaining low cost is the primary challenge.

This Special Issue addresses a variety of system, communication, and analog/digital signal processing aspects of wireless communications. A major focus of this special issue is devoted to wireless design issues, RF signal processing circuits, baseband filtering, and modulation and demodulation circuits and related interfaces. The primary emphasis is on low power approaches to circuits, algorithms, and architectures that apply directly to wireless systems.

In the development of the Special Issue, 32 papers were received and submitted for review. After undergoing a serious and valuable anonymous review process, 11 papers originating from a variety of academic and industrial institutions located around the world, are presented here in this special issue. These papers, while all dealing with low power wireless communications, are focused on two highly integrated subthemes of this increasingly important topic. These two subthemes are low power wireless communication circuits and systems and low power design methodologies for wireless communications.

I. LOW POWER WIRELESS COMMUNICATION CIRCUITS AND SYSTEMS

Six papers are presented in the low power wireless communication circuits and systems subtheme which deal with topics such as transceiver architectures, RF/IF filters, and direct sequence spread spectrum systems. Additional topics include the effects of IF filters on bit-error rate (BER) and adaptive multiuser detectors for spread spectrum systems.

Razavi presents in his paper, "Design Considerations for Direct-Conversion Receivers," an overview of design methods for direct-conversion zero-IF receivers. Direct conversion of RF signal into base-band signal offers many advantages. However, dc offset, I/Q mismatch, even-order distortion, flicker noise, and oscillator leakage can cause major design challenges. This paper describes these effects and proposes solutions to combat these problems. Related design techniques for amplification and mixing, quadrature phase calibration, and baseband processing are also described.

Fabre, Saaid, Wiest, and Boucheron discuss in their paper, "Low Power Current-Mode Second-Order Bandpass Cell Suitable for IF Stages," an efficient BiCMOS current-mode bandpass filter for the IF receiver stage targeted for the GSM cellular telephone. The bandpass topology is implemented using a current-controlled conveyor. In addition to the IF stage, the circuit is composed of a voltage to conversion input cell, a current to voltage output cell, and a programmable gain amplifier. Simulation and prototype results are described for this prototype circuit: less than 38 mW for the entire IF stage with a ± 2.5 V power supply. He, Lo, and Litva present in their paper, "A Spread Spectrum System with a Time Domain Processing Device," a new time domain processing device based on a SAW storage correlator. An analysis of the interference rejection capability of this system is described and quantitative techniques for evaluating the probability of error of the system are presented. These results are validated by an experiment using the SAW storage correlator to demodulate the spread spectrum signal.

Park and Doherty discuss in their paper, "Generalized Project Algorithm for Blind Interference Suppression in DS/CDMA Communications," adaptive interference cancellation algorithms for direct sequence CDMA systems. A new adaptive algorithm is presented to improve the multiuser interference in CDMA systems. The algorithm adaptively adjusts the filter coefficients by iteratively projecting the filter coefficients onto constraint sets. The performance characteristics of the proposed algorithm are demonstrated on simulations of the output signal-to-interference ratio and bit-error rate.

Ai, Daigle, and Petrovic consider in their paper, "Group-Delay Optimized IF Filters for Narrowband PCS" the effects of IF filters on bit-error rate performance of a narrowband PCS device. Design tradeoffs for IF filters and the group delay effects on the BER for wireless data transmission using FSK

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modulation are also discussed. Dutta and Kiaei present in their paper, "Adaptive Multiuser Detector for Asynchronous DS-CDMA in Rayleigh Fading," an adaptive multiuser interference cancellation method for base-station receivers.

II. Low Power Design Methodologies for Wireless Communications

Five papers are presented in the low power design methodologies for wireless communications subtheme. These papers consider topics such as estimating and bounding the power of digital multipliers, the design of low power RF power amplifiers, and developing algorithms for low power FIR digital filters. Additional topics include the effects of analog versus digital low power matched filter design and power management techniques in concert with new low energy register structures.

Satyanarayana and Parhi present in their paper, "A Theoretical Approach to Estimation of Bounds on Power Consumption in Digital Multipliers," a systematic strategy for bounding the power consumption in digital multipliers. This circuit structure is common to all forms of digital communication devices and therefore these power bounds are directly applicable to wireless systems, permitting predictions of battery life. The analysis is presented for both nonpipelined and bit level pipelined multipliers. Simulations of example multipliers are presented that verify the predicted theoretical bounds.

Izadpanah, Malkemes, Chukurov, and Cordell present in their paper, "Low Power Transmitter Experimental Prototype and Simulation for Personal Access Communications System (PACS)," both simulated and prototype results describing a PACS subscriber unit transmitter RF power amplifier. Transmitter spectral spreading and adjacent channel power ratio variations using both experimental and simulation based on GaAs FET, GaAs HBT, and InP HBT technologies are described. This paper presents an interesting comparison of the performance characteristics of different relevant technologies validated by physical results specific to the wireless communications problem.

Sankarayya, Roy, and Bhattacharya present in their paper, "Algorithms for Low Power and High Speed FIR Filter Realization Using Differential Coefficients," new algorithms for computing the convolution with the input data that is particularly amenable to both low power and high speed realizations of FIR filters. These algorithms use differences between the coefficients for computing the convolution, resulting in a reduction in the necessary computations per convolution as compared to a direct use of coefficients. Net energy savings of up to 50% with a two times speedup is achievable with this filter design technique.

Hahm, Friedman, and Titlebaum present in their paper, "A Comparison of Analog and Digital Circuit Implementations of Low Power Matched Filters for Use in Portable Wireless Communication Terminals," analog and digital circuit realizations of a parallel programmable matched filter in which minimum power dissipation is investigated as a function of data precision, filter length, operating frequency, and technology. A multidimensional design space is described in which an appropriate implementation strategy is determined based on specific technological and systems parameters.

Lang, Musoll, and Cortadella present in their paper, "Individual Flip-Flops with Gated Clocks for Low Power Datapaths," techniques to reduce energy consumption in registers by individually deactivating the clock signal when the state of the register is not being changed. New register structures are proposed and relevant energy minimization criteria are presented in terms of additional timing constraints and their effects on overall performance. The evaluations utilize structure-specific energy models and are validated by switch-level simulations and, for the applications considered, demonstrate significant reductions in energy.

This Special Issue presents a number of interesting strategies for designing and building low power wireless communications systems. Many aspects of the systems, circuits, and design methodologies presented in these articles are being developed and applied today in next generation wireless communications systems. As the wireless industry develops and matures, aggressive strategies will be required to provide practical low cost and low power solutions for the expanding wireless user community.

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It is our sincere hope that this Special Issue will help augment and enhance the growing research and development efforts in low power wireless communications systems.

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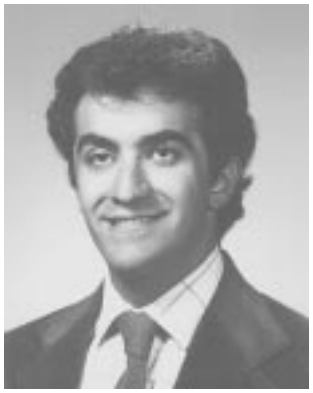

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