Effective Capacitance of Inductive Interconnects for Short-Circuit Power Analysis

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***Abstract*—Interconnect resistance and inductance shield part of the load capacitance, resulting in a faster voltage transition at the output of the driver. Ignoring this shielding effect may induce significant error when estimating short-circuit power. In order to capture this shielding effect, an effective capacitance of a distributed RLC load is presented for accurately estimating the short-circuit power. The proposed method has been verified with Cadence Spectre simulations. The average error of the short-circuit power obtained with the effective capacitance is less than 7% for the example circuits as compared with an RLC π model. This effective capacitance can be used in look-up tables or in empirical k-factor expressions to estimate short-circuit power.**

***Index Terms*—Interconnect, RLC, shielding effect, short-circuit power.**

I. Introduction

SINCE power has become an important design criterion in integrated circuits, accurate and efficient power estimation is required in the circuit design process. As compared with dynamic power which is well characterized, short-circuit power is more difficult to model due to the complicated transient behavior of the short-circuit current [1].

The short-circuit power dissipation in a gate is primarily determined by three factors: input signal transition time, load capacitance, and size of the transistors in the gate. In [2], Veendrick developed a closed-form expression for short-circuit power dissipation in an unloaded CMOS inverter. More accurate device models have recently been adopted to analyze short-circuit power [3], [4]. It is shown in [4] that short-circuit power can be as high as 20% of the total active power in high speed, low voltage circuits. As interconnect coupling becomes more significant in advanced technologies, the impact of crosstalk noise on the short-circuit power is analyzed in [5] by introducing an effective input slew. In these analyses, a lumped capacitor is assumed as the load. With CMOS technology scaling, the interconnect resistance can be comparable to the gate resistance and should be included in the load model. In [6], a π shaped RC model is adopted as the load. An effective capacitance of the RC π structure for short-circuit power estimation is described in [7] and [8] to maintain compatibility with popular look-up table or k-factor based power models. With increasing on-chip frequencies and longer interconnects, the interconnect inductance can also no longer be ignored. As described in [9], the interconnect inductance also exhibits a shielding effect on the load capacitance, increasing the short-circuit power dissipated by the driver.

In [10], an effective capacitance of an RLC load is developed to accurately estimate short-circuit power. This effective capacitance model is extended in this paper. The importance of the inductive shielding effect is identified and the model is further verified for gates with unaligned multiple inputs. The rest of this paper is organized as follows. In Section II, a distributed RLC network is reduced into a π model. From this π model, the effective capacitance is determined. In Section III, the proposed effective capacitance model is verified by Cadence Spectre simulations for gates with single and multiple inputs. Finally, some conclusions are offered in Section IV.

II. Effective Capacitance of an Inductive Load

Model order reduction techniques are commonly used to analyze the timing and power of interconnects to improve simulation efficiency. In Section II-A, a π model is generated from a distributed RLC tree through a typical model order reduction method—moment matching. In Section II-B, this π model is further reduced into an effective capacitance by matching the average charging/discharging current.

A. π Model Representation of RLC Interconnects

In [11], an RC network is reduced to an RC π model by matching the first three moments (y_1, y_2, and y_3) of the admittance at the driving point. Similarly, an RLC network can be reduced to an RLC π model by matching the first four moments, as shown in Fig. 1. This reduction, however, can be unrealizable (the value of the circuit element is not positive real). In order to obtain a realizable RLC π model, a coefficient y_3^* is introduced in [12], which is the third order admittance moment without considering the inductance. By matching y_1, y_2, y_3, and y_3^*, the π model parameters can be obtained as [12]

$$C_f = y_2^2/y_3^* \tag{1}$$

$$C_n = y_1 - C_f \tag{2}$$

$$R_\pi = -y_2/C_f^2 \tag{3}$$

$$L_\pi = (y_3^* - y_3)/C_f^2 \tag{4}$$

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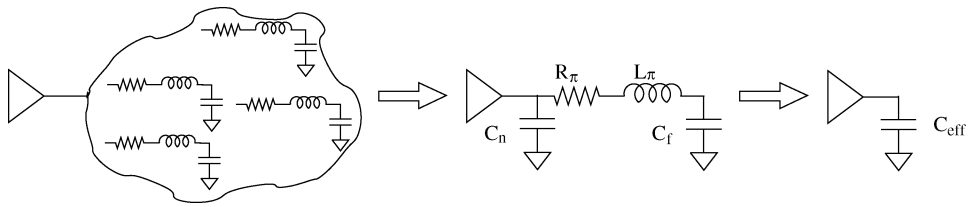

Fig. 1. Reduction of an RLC interconnect network.

where C_n and C_f denote the near end and far end capacitance, respectively.

The input admittance of a distributed RLC interconnect with a load admittance Y_l is [13]

$$Y(s) = \frac{Z_c Y_l + \tanh\theta}{Z_c(1 + Z_c Y_l \tanh\theta)} \tag{5}$$

where $\theta = \sqrt{(R_t + sL_t)sC_t}$ and $Z_c = \theta/(C_t s)$. R_t, C_t, and L_t are the total resistance, capacitance, and inductance of the interconnect, respectively. By expanding $Y(s)$ into a Taylor series of s around zero, the moments at the input of the RLC interconnect can be obtained as

$$y_1 = y_{l,1} + C_t \tag{6}$$

$$y_2 = y_{l,2} - R_t\left(y_{l,1}^2 + y_{l,1}C_t + \frac{1}{3}C_t^2\right) \tag{7}$$

$$\begin{aligned} y_3 = {} & y_{l,3} - R_t(2y_{l,1}y_{l,2} + y_{l,2}C_t) \\ & + R_t^2\left(y_{l,1}^3 + \frac{4}{3}y_{l,1}^2 C_t + \frac{2}{3}y_{l,1}C_t^2 + \frac{2}{15}C_t^3\right) \\ & - L_t\left(y_{l,1}^2 + y_{l,1}C_t + \frac{1}{3}C_t^2\right) \end{aligned} \tag{8}$$

$$\begin{aligned} y_3^* = {} & y_{l,3}^* - R_t(2y_{l,1}y_{l,2} + y_{l,2}C_t) \\ & + R_t^2\left(y_{l,1}^3 + \frac{4}{3}y_{l,1}^2 C_t + \frac{2}{3}y_{l,1}C_t^2 + \frac{2}{15}C_t^3\right). \end{aligned} \tag{9}$$

The input admittance moments of a distributed RLC tree can be determined by recursively applying (6)–(9). From these moments and (1)–(4), the corresponding π structure can be obtained.

B. Effective Capacitance for Short-Circuit Power

Although a π model is highly accurate, four coefficients are required in this model, making it incompatible with k-factor expressions or look-up table based power models. An effective capacitance greatly simplifies the model with little penalty in accuracy, as shown in Fig. 1.

The shielding effect of the interconnect resistance is well known and the effective capacitance of RC interconnects has been developed for estimating delay and short-circuit power in [7], [14]. The interconnect inductance however also exhibits a shielding effect [9]. This inductive shielding effect is illustrated with an example, as shown in Fig. 2. In Fig. 2, a distributed RLC tree is driven by a 0.18-μm CMOS inverter. Since the shielding effect of the interconnect is only significant in interconnect loads with a high impedance which are generally driven by large gates, a large inverter is considered with transistor sizes, $W_n = 10\,\mu$m

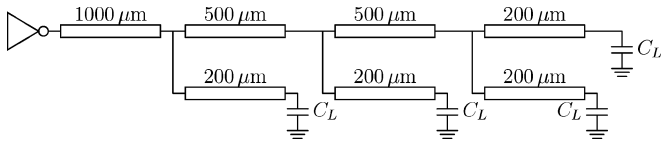

Fig. 2. Example of a distributed RLC tree.

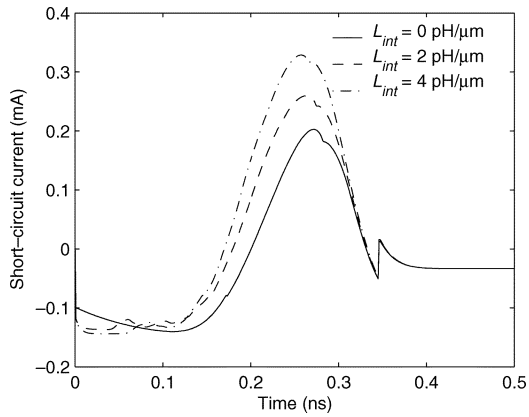

Fig. 3. Effect of inductance on short-circuit current. $t_r = 0.5$ ns.

and $W_p = 25\,\mu$m. The impedance parameters of the interconnect are $R_{\rm int} = 12.23\ \Omega/\mu$m and $C_{\rm int} = 0.245$ fF/μm. These impedance values are extracted from a typical top layer wire structure in a 0.18-μm CMOS technology. The wire width is 2 μm and wire thickness is 1 μm. The load capacitance is $C_L = 0.1$ pF. The short-circuit current in the inverter is illustrated in Fig. 3 for different values of interconnect inductance. When the interconnect inductance becomes larger, a greater far end capacitance is shielded. Less effective capacitance is therefore seen at the inverter output, permitting the output voltage to change faster at the beginning of the signal transition, thereby producing a larger short-circuit current. The currents are measured at the source of the pMOS transistor with a rising edge input as shown in Fig. 4. The discontinuity of the waveform is due to the discontinuity of the transistor capacitance model used in the simulation. Strictly speaking, the currents shown in Fig. 3 include two non-short-circuit current components. The first component is the current flowing through the capacitance C_{gs}, as shown in Fig. 4. This component can be determined as $I_{gs} = C_{gs}V_{\rm dd}/t_r$ and is independent of the load. The second component is the current $I_{\rm ov}$ flowing from the output to $V_{\rm dd}$ due to the overshoot at the output at the beginning of the signal transition. $I_{\rm ov}$ returns a small amount of charge stored in the output node back to $V_{\rm dd}$, slightly reducing the dynamic power.

In [14], the output waveform of a CMOS gate is approximated by a quadratic function followed by a linear function. In this

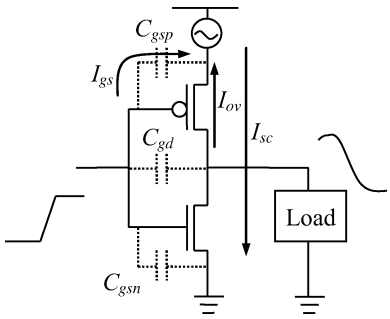

Fig. 4. Current components in a CMOS inverter.

paper, the output waveform of a gate is modeled as a quadratic function during the input transition. Assuming the output waveform is $v(t) = at^2$ for a rising edge, the current drawn from the gate by an RLC π structure is

$$I_\pi(s) = \frac{2a}{s^3}\left(\frac{C_f s}{1 + R_\pi C_f s + L_\pi C_f s^2} + C_n s\right). \quad (10)$$

Applying an inverse Laplace transformation to (10), the current in the time domain is

$$i_\pi = 2aC_f(-R_\pi C_f + t + k_1 e^{s_1 t} + k_2 e^{s_2 t}) + 2aC_n t \quad (11)$$

where

$$s_{1,2} = \frac{-R_\pi \pm \sqrt{R_\pi^2 - \frac{4L_\pi}{C_f}}}{2L_\pi} \quad (12)$$

$$k_1 = \frac{1}{s_1^2(s_1 - s_2)L_\pi C_f} \quad (13)$$

$$k_2 = \frac{1}{s_2^2(s_2 - s_1)L_\pi C_f}. \quad (14)$$

The current drawn from the gate by an effective capacitance is

$$i_{\text{ceff}} = 2aC_{\text{eff}}t. \quad (15)$$

Equating the average of i_π and i_{ceff} during a period from 0 to an evaluation time t_{ev}, C_{eff} can be obtained as

$$C_{\text{eff}} = C_n + C_f\left[1 - \frac{2R_\pi C_f}{t_{\text{ev}}} + \frac{2k_1}{t_{\text{ev}}^2 s_1}(e^{s_1 t_{\text{ev}}} - 1) + \frac{2k_2}{t_{\text{ev}}^2 s_2}(e^{s_2 t_{\text{ev}}} - 1)\right]. \quad (16)$$

Similarly, C_{eff} for an RC π structure is

$$C_{\text{eff}} = C_n + C_f\left[1 - \frac{2R_\pi C_f}{t_{\text{ev}}} + \frac{2R_\pi^2 C_f^2}{t_{\text{ev}}^2}\left(1 - e^{-\frac{t_{\text{ev}}}{R_\pi C_f}}\right)\right]. \quad (17)$$

As expected, C_{eff} is between C_n and $C_n + C_f$. From (16), C_{eff} is a function of t_{ev} as shown in Fig. 5. The π model parameters are obtained from the tree structure as shown in Fig. 2 with an inductance per unit length $L_{\text{int}} = 0.74\,\text{pH}/\mu\text{m}$. With increasing

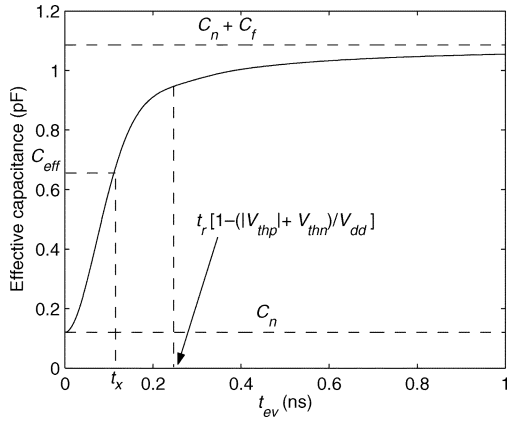

Fig. 5. Effective capacitance as a function of t_{ev}. $C_n = 120.1$ fF, $C_f = 965.9$ fF, $R_\pi = 15.9\ \Omega$, and $L_\pi = 0.96$ nH.

t_{ev}, C_{eff} increases from C_n and approaches $C_n + C_f$. In [14], t_{ev} is the time when the driver output achieves 50% of V_{dd}, which is the objective and is not known *a priori*. Several iterations are therefore required to determine C_{eff}. In [7], t_{ev} is determined as the end point of the short-circuit period. Since the short-circuit current exists when the input is between V_{thn} and $V_{\text{dd}} + V_{\text{thp}}$, the appropriate evaluation time t_x is in the range from 0 to $t_r(1 - (|V_{\text{thp}}|/V_{\text{dd}}) - (V_{\text{thn}}/V_{\text{dd}}))$. Note that $t = 0$ corresponds to the time when the input reaches V_{thn} for a rising edge ($V_{\text{dd}} + V_{\text{thp}}$ for a falling edge). As shown in Fig. 5, for the time period $0 < t < t_x$, the effective capacitance is overestimated and the short-circuit current is underestimated. For the period $t_x < t < t_r(1 - (|V_{\text{thp}}|/V_{\text{dd}}) - (V_{\text{thn}}/V_{\text{dd}}))$, the effective capacitance is underestimated and the short-circuit current is overestimated. By properly adjusting t_x, the estimation error of the short-circuit current in different time regions can be canceled. By comparing Spectre simulations, a fitting parameter is adopted to determine t_x

$$t_x = 0.46t_r\left(1 - \frac{|V_{\text{thp}}|}{V_{\text{dd}}} - \frac{V_{\text{thn}}}{V_{\text{dd}}}\right). \quad (18)$$

The short-circuit current waveforms in an inverter with different load models are compared in Fig. 6. For this inverter, $V_{\text{thn}} = 0.5$ V and $V_{\text{thp}} = -0.5$ V. As shown in Fig. 6, the π model can accurately characterize a tree structure. The waveform obtained with a π model is indistinguishable from the waveform with the original RLC tree (shown in Fig. 2). Using the total capacitance $C_{\text{tot}} = C_n + C_f$ as the load, however, significantly underestimates the short-circuit current. As previously mentioned, the short-circuit current with the effective capacitance is first underestimated and then overestimated. No iterations are required to determine C_{eff}. Since an RLC π model is commonly required in timing analysis, the additional computational expense required to determine C_{eff} is small. Note that unlike C_{eff} for estimating the delay [14], C_{eff} for short-circuit power estimation is independent of the transistor size.

III. Model Verification

The proposed effective capacitance model is verified with gates with a single input (inverter), multiple inputs, and unaligned multiple inputs in Section III-A–C, respectively.

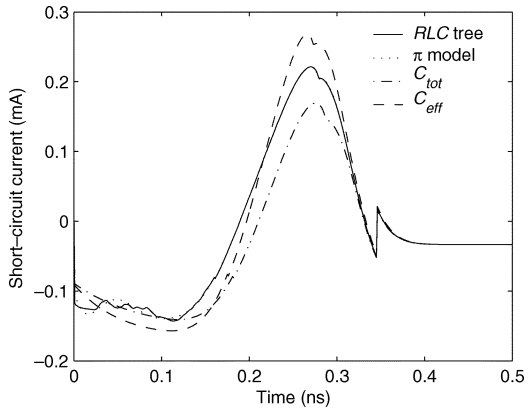

Fig. 6. Short-circuit current with different output loads.

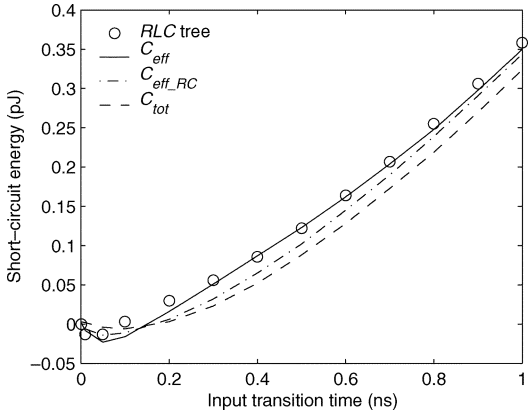

Fig. 7. Short-circuit energy with different loads. $L_{\rm int} = 0.74$ pH/μm.

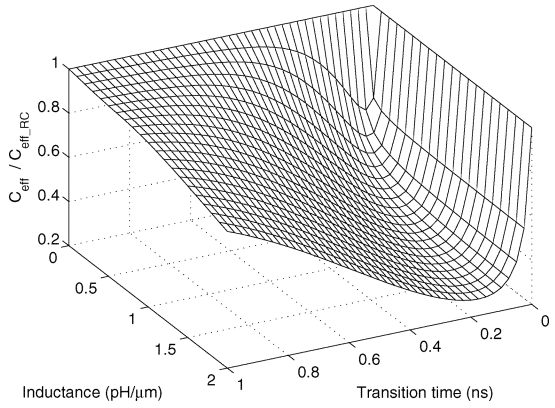

Fig. 8. Effect of inductance on the effective capacitance.

TABLE I
SHORT-CIRCUIT ENERGY DISSIPATION DURING A FULL SIGNAL SWITCH IN A NAND GATE

t_r (ns)	R_π/L_π /C_n/C_f (Ω/nH/pF/pF)	C_{eff} (pF)	Short-circuit energy (pJ)								
			Upper			Lower			Both		
			π	C_{eff}	C_{tot}	π	C_{eff}	C_{tot}	π	C_{eff}	C_{tot}
0.5	100/2/0.2/0.6	0.37	0.12	0.12	0.08	0.11	0.10	0.07	0.06	0.05	0.02
1	100/2/0.2/0.6	0.52	0.35	0.35	0.30	0.36	0.35	0.29	0.30	0.29	0.24
2	100/2/0.2/0.6	0.64	0.93	0.93	0.87	0.98	0.97	0.91	0.88	0.86	0.81
0.5	200/3/0.1/0.8	0.21	0.15	0.15	0.08	0.14	0.13	0.06	0.09	0.07	0.02
1	200/3/0.1/0.8	0.32	0.41	0.41	0.28	0.41	0.41	0.28	0.35	0.34	0.23
2	200/3/0.1/0.8	0.48	0.99	1.00	0.83	1.05	1.05	0.87	0.94	0.93	0.78
0.5	300/4/0.1/0.3	0.17	0.16	0.16	0.12	0.15	0.14	0.10	0.09	0.08	0.05
1	300/4/0.1/0.3	0.23	0.45	0.45	0.38	0.45	0.45	0.38	0.38	0.37	0.32
2	300/4/0.1/0.3	0.29	1.11	1.11	1.04	1.16	1.16	1.09	1.03	1.02	0.96
*0.2	200/3/0.1/0.8	0.12	0.03	0.03	0.01	0.03	0.03	0.01	0.02	0.02	0.01
*0.5	200/3/0.1/0.8	0.19	0.11	0.13	0.06	0.13	0.14	0.07	0.11	0.12	0.06
*1	200/3/0.1/0.8	0.30	0.27	0.30	0.20	0.31	0.34	0.22	0.28	0.29	0.21
Average % Error			—	3.7	26.7	—	3.5	30.3	—	6.2	36.7

A. Gate With Single Input

For the example circuit shown in Fig. 2, the short-circuit energy dissipated over a full signal transition with different loads is compared in Fig. 7. As shown in Fig. 7, the total capacitance always underestimates the short-circuit energy as compared with a distributed RLC tree. For example, the error for $t_r = 0.5$ ns is 28.1%. More accurate estimations can be obtained with $C_{\rm eff\_RC}$ (only considering the resistive shielding effect) and $C_{\rm eff}$ (considering both resistive and inductive shielding effects).

The inductive shielding effect is most important for this example in the range from $t_r = 0.2$ ns to $t_r = 0.8$ ns. The inductive shielding effect can be evaluated by the ratio of $C_{\rm eff}$ to $C_{\rm eff\_RC}$. In Fig. 8, this ratio is plotted with different input transition times and wire inductances for the example circuit shown in Fig. 2. As shown in Fig. 8, $C_{\rm eff}$ decreases with increasing interconnect inductance. The ratio of $C_{\rm eff}$ to $C_{\rm eff\_RC}$ can be smaller than 0.3. When t_r approaches zero, the driver only sees the near-end capacitance, both $C_{\rm eff}$ and $C_{\rm eff\_RC}$ approach C_n, and the ratio $C_{\rm eff}/C_{\rm eff\_RC}$ approaches one. When t_r is sufficiently large, the driver has sufficient time to charge and discharge the far end capacitance, both $C_{\rm eff}$ and $C_{\rm eff\_RC}$ approach $C_{\rm tot}$, and the ratio also approaches one.

Since the dynamic power is usually determined as $\alpha f V_{\rm dd}^2 C_{\rm load}$ (where α is the switching factor), the reduction in dynamic power $P_{\rm red}$ due to $I_{\rm ov}$ is considered part of the short-circuit power such that the summation of the two power components (dynamic and short-circuit) can represent the total transient power. With fast inputs, $P_{\rm red}$ can dominate the short-circuit power, producing a negative short-circuit power, as shown in Fig. 7. Since $P_{\rm red}$ cannot be characterized by $C_{\rm eff}$, the error of the power estimation is greater for fast inputs. With very slow inputs, although the output voltage waveform deviates from a quadratic behavior, the proposed method remains accurate as shown in Fig. 7. In these cases, the shielding effects are small, and the effective capacitance approaches $C_{\rm tot}$. This behavior is well captured by (16).

B. Gate With Multiple Inputs

The effective capacitance concept can also be applied to other logic gates with multiple inputs, such as NAND and NOR gates. The short-circuit energy consumed by a two input NAND gate during a full signal transition is listed in Table I for different input transition times and interconnect loads. The two inputs of the NAND gate are denoted as the upper input and the lower input according to the relative position of the input terminal. Three switching patterns are considered: only the upper input is switched (the lower input is tied to $V_{\rm dd}$), only the lower input is switched, and both of the two inputs are connected and simultaneously switched. The size of the transistors in the NAND gate is $W_n = 10$ μm and $W_p = 25$ μm. The rows starting with an '$*$' are obtained with a 45-nm [15] CMOS NAND gate, and the transistor sizes are $W_n = 4$ μm and $W_p = 10$ μm. As listed in Table I, the effective capacitance can accurately capture the

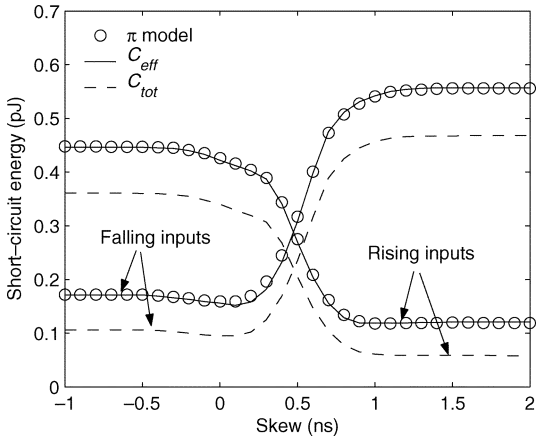

Fig. 9. Short-circuit energy with multiple switching inputs. $C_n = 0.1$ pF, $C_f = 0.8$ pF, $R_\pi = 200\ \Omega$, and $L_\pi = 3$ nH.

shielding effect of the resistance and inductance in determining the short-circuit power. The average error of the short-circuit power is less than 7% as compared with the π model. The average error with the total capacitance, however, is more than 26% for these examples. Note that for a 45-nm CMOS technology, a new fitting parameter can be determined to further improve the accuracy of the model.

C. Gate With Unaligned Multiple Inputs

For multiple switching inputs with offsets in delay (non-simultaneous input signals), an equivalent input signal has been developed in [16] for estimating the short-circuit power. From this equivalent input signal, an effective capacitance can be obtained from (16) and (18). The short-circuit energy dissipated in a NAND gate is shown in Fig. 9 for different skew between the two inputs. The transition time of the upper input and lower input is 1 and 2 ns, respectively. The skew is determined as $t_{\rm upper} - t_{\rm lower}$, where $t_{\rm upper}$ and $t_{\rm lower}$ are the starting time of the transition at the upper input and lower input, respectively. From Fig. 9, it can be seen that the effective capacitance model is also valid for multiple switching inputs with delay offsets.

Look-up tables or k-factor expressions are commonly used to model short-circuit power as a function of t_r and C_L. The total transient power in a CMOS gate driving an interconnect network, therefore, can be represented as

$$P_{\rm total} = P_{sc}(t_r, C_{\rm eff}) + \alpha f C_{\rm load} V_{\rm dd}^2 \qquad (19)$$

where $C_{\rm load}$ includes the total interconnect capacitance and the parasitic capacitance of the transistors. If glitches occur at the output, both dynamic power and short-circuit power depend upon the transient voltage waveform at the output. Expression (19) is no longer valid in this case and a more complicated analysis is required.

IV. Conclusions

As CMOS technology is scaled, the interconnects not only dominate the overall circuit delay, but also greatly affect the power dissipation. The dynamic switching power of a circuit is directly related to the total interconnect capacitance. Using the total interconnect capacitance to estimate the short-circuit power, however, can lead to significant error due to the shielding effect of the interconnect impedance. In this paper, an effective capacitance of a distributed RLC load is developed to accurately estimate the short-circuit power. The average error of the short-circuit power obtained with $C_{\rm eff}$ is less than 7% as compared with an RLC π model. This effective capacitance can be used in look-up tables or in empirical k-factor expressions to estimate short-circuit power as well as in analytic models to simplify the interconnect analysis process.

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