Energy-Efficient Nonvolatile Flip-Flop With Subnanosecond Data Backup Time for Fine-Grain Power Gating

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Abstract—**A nonvolatile flip-flop (NVFF) is proposed, where magnetic tunnel junctions (MTJs) are incorporated into a CMOS flip-flop (FF) to enable nonvolatility. The voltage-controlled magnetic anisotropy (VCMA) effect is utilized to back up the latched data into MTJs before the power supply is turned off. Switching an MTJ through the VCMA effect does not require a dedicated write circuit for data backup, resulting in reduced area as compared with NVFFs exploiting the spin transfer torque (STT) switching mechanism. In a VCMA-based NVFF, the MTJs are coherently switched, enabling ultra-energy efficient data backup with subnanosecond backup time. Simulation results exhibit more than a $342\times$ ($33.7\times$) improvement in data backup energy per bit, and more than $35.5\times$ ($7.7\times$) improvement in data backup delay per bit as compared with the most efficient STT-based NVFFs (spin Hall effect-based NVFF). The energy efficiency of the VCMA-based NVFF results in sufficiently short breakeven times, enabling effective fine-grain power gating.**

Index Terms—**Breakeven time (BET), fine-grain power gating, magnetic tunnel junction (MTJ), nonvolatile flip-flop (NVFF), voltage-controlled magnetic anisotropy (VCMA).**

I. INTRODUCTION

LEAKAGE current in high-performance CMOS logic circuits has drastically increased, becoming the dominant component of power dissipation [1]. Power gating (PG) architectures have emerged as an effective method to reduce leakage current [2] by disconnecting a circuit block from the power supply during sleep mode [2]. To save energy, therefore, the sleep mode has to be sufficiently long to compensate for the energy overhead used during processing. The minimum duration of the sleep mode to produce a gain in energy is referred to here as the breakeven time (BET) [3]. The BET is the time during which the energy saved by PG equals the energy lost by the overhead. To support fine-grain PG, which requires short BETs, the PG energy overhead should be significantly reduced.

Nonvolatile flip-flops (NVFFs) in a PG domain is a promising technique to preserve data when the domain is turned off [4]–[8]. During active mode, an NVFF operates as a conventional flip-flop (FF). An NVFF stores the current logic state within nonvolatile storage devices once the backup mode is initiated. During sleep mode, where the PG domain is disconnected from the power supply, an NVFF retains the logic state in a nonvolatile storage element. When the active mode is initiated, the stored logic state is retrieved from the NVFF, and the PG domain resumes normal operation.

A magnetic tunnel junction (MTJ) [9]–[11] is a device whose electrical resistance can be switched between two stable states. One bit of information may therefore be retained within an MTJ. Owing to high retention time and compatibility with CMOS process technologies, an MTJ can be used to introduce nonvolatility into a CMOS FF [4]–[8]. A bit can be written either magnetically or electrically into an MTJ. Electrical writing mechanisms offer opportunities to introduce MTJs into high-performance applications requiring low power consumption. An MTJ may be electrically written through: 1) the spin transfer torque (STT) effect [12]; and/or 2) the voltage-controlled magnetic anisotropy (VCMA) effect [13]–[15].

The STT mechanism writes an MTJ using current pulses that transport spin angular momentum. A current pulse may be injected into an MTJ either directly [12] or through a spin Hall effect (SHE) metallic layer [16]. For a specific duration of the injected current pulse, the operation of the STT mechanism is maintained as long as the amplitude of the current pulse is larger than a threshold current. Since the current threshold grows significantly as the duration of the pulse decreases, fast operation through the STT mechanism compromises the power efficiency. Hence, an STT-based NVFF suffers from a large energy overhead, making STT-based NVFFs unable to support fine-grain PG schemes where short BETs are required [2], [3], [6]. Furthermore, the STT effect causes an MTJ to switch stochastically over a widely distributed switching time [12]. The VCMA mechanism has therefore attracted considerable attention for spintronic applications operating at ultralow power levels [13]–[15]. The VCMA method is an electric field-driven mechanism that switches an MTJ through a voltage pulse applied across an MTJ device. Theoretical [10], [18] and experimental [15] results demonstrate that the required energy for switching (writing a bit into) an MTJ through the VCMA mechanism may be potentially less than 1 fJ for a subnanosecond switching time.
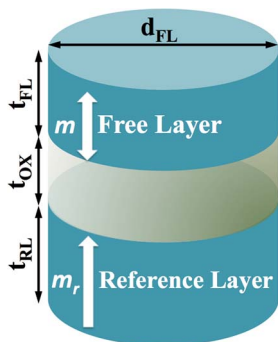
Fig. 1. PMTJ. The magnetic easy axes of the FM layers are perpendicular to the plane of the layers.

TABLE I
DESIGN PARAMETERS OF PMTJ IN VCMA-BASED NVFF

Parameter	Numerical value
Free layer diameter (d_{FL})	70 nm
Free layer thickness (t_{FL})	0.9 nm
Barrier thickness (t_{OX})	1.4 nm
Reference layer thickness (t_{RL})	1.8 nm
Magnetization saturation	1.4 Tesla
Gilbert damping factor (α)	0.02
Resistance-area product	130 Ω μm^2
Tunneling magnetoresistance (TMR)	150%

In this brief, a VCMA-based NVFF is introduced for ultraenergy-efficient storage and fast backup operations. The backup operation with the proposed VCMA-based NVFF is achieved by applying a voltage pulse across the device. No dedicated writing circuit is therefore incorporated within the circuit, resulting in small area overhead. Data backup operation in the VCMA-based NVFF is achieved through coherent switching of an MTJ [10], [14]. Fast backup operation is therefore performed by properly signaling the MTJs and not by dissipating additional energy. The energy efficiency permits the VCMA-based NVFF to support fine-grain PG architectures, where short BETs are required. Furthermore, no detectable incubation time [10] associated with the coherent switching mechanism is necessary. Therefore, in contrast to STT-based NVFFs, the data backup operation with the VCMA-based NVFF is a deterministic process.

The rest of this brief is organized as follows. The VCMA-based NVFF is described in Section II. Validation of the VCMA-based NVFF through simulation and experimental data of PMTJs is discussed in Section III. A comparison between the VCMA-based NVFF and previously proposed NVFFs is provided in Section IV. This brief is concluded in Section V.

II. VCMA Switching Mechanism

An MTJ is composed of two ferromagnetic (FM) nanolayers separated by a tunneling barrier. The magnetization of an FM layer, which is referred to as the reference layer, is fixed, whereas the magnetization of the other FM layer, referred to as the free layer, can be aligned either parallel (P) or antiparallel (AP) to the magnetization of the reference layer. The electrical resistance of an MTJ is high (low) for an AP (P) configuration of the FM layers.

MTJs with perpendicular-to-the-plane anisotropy (PMTJs) [11] are used in the VCMA-based NVFF, where the magnetic easy axis of the FM layers, as shown in Fig. 1, is perpendicular to the plane of the layers. The parameters of the PMTJ [14] used to evaluate the proposed VCMA-based NVFF are listed in Table I. A PMTJ exhibits higher thermal stability than MTJs with in-plane anisotropy (IMTJs), where the magnetic easy axis of the FM layers is in the plane of the layers. A PMTJ is therefore more scalable than an IMTJ.

The VCMA mechanism reverses the magnetization of the free layer by a temporal change in the direction of the magnetic easy axis through a voltage pulse V_p applied across the device [10], [13]–[15]. A change of the easy axis direction temporarily modulates the perpendicular magnetic anisotropy (PMA) field ($H_{s,\mathrm{perp}}$), inducing precessional motion of the magnetization of the free layer ($\mathbf{m}$) around the effective magnetic field $\mathbf{H}_{\mathrm{eff}}$ experienced by the free layer. Magnetization switching occurs through the motion when the duration of the applied voltage pulse t_p is in the range of half an integer of the precession period [13]–[15], [18].

For an PMTJ, the effective magnetic field $\mathbf{H}_{\mathrm{eff}}$ experienced by the free layer is characterized as [10]

$$\mathbf{H}_{\mathrm{eff}} = -\frac{1}{2} \bigtriangledown_{\mathbf{m}} \left[\left(H_c m_y^2 + H_{s,\mathrm{perp}}(V_p) m_z^2 \right) - \mathbf{m} \cdot \mathbf{H}_{\mathrm{d}} \right]$$

where $\mathbf{m} = (m_x, m_y, m_z)$ is a unit vector characterizing the orientation of the magnetization of the free layer, H_c is the in-plane coercive field, $H_{s,\mathrm{perp}}(V_p)$ is the PMA field modulated by the voltage V_p applied across the device, and $\mathbf{H}_{\mathrm{d}}$ represents the resultant of the fields exerted on the free layer. The period of the precessional motion is determined by the in-plane component of $\mathbf{H}_{\mathrm{eff}}$ and is proportional to the Larmor frequency [10], [14]. No external magnetic field is required to maintain the VCMA mechanism [10], [15], and the strength of the in-plane component of $\mathbf{H}_{\mathrm{eff}}$ is tuned to the device [10], [15].

III. VCMA-Based NVFF

Here, the structure of the VCMA-based NVFF and different modes of operation are explained. The modes of operation that occur sequentially within an VCMA-based NVFF are active mode, data backup mode, sleep mode, data restore mode, and bit reset mode. Bit reset is a novel mode of operation that permits the FF to write only one MTJ while backing up the data bit. In previously proposed NVFFs [4]–[8], all MTJs are over written during the backup mode even if the MTJs are already at the correct magnetic configuration (P or AP) corresponding to the new bit of information.

A. Structure of VCMA-Based NVFF

As shown in Fig. 2, the VCMA-based NVFF is composed of a volatile master latch followed by a nonvolatile slave latch. The nonvolatile latch includes two PMTJs (PMTJ1 and PMTJ2), which retain the latched bit when the circuit is power gated off. The PMTJs are accessible through two transmission gates,
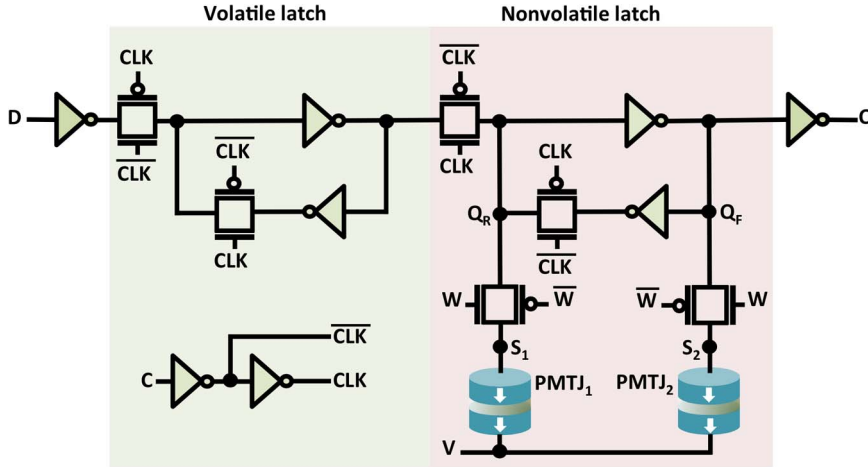
Fig. 2. VCMA-based NVFF composed of a volatile master latch followed by a nonvolatile slave latch.
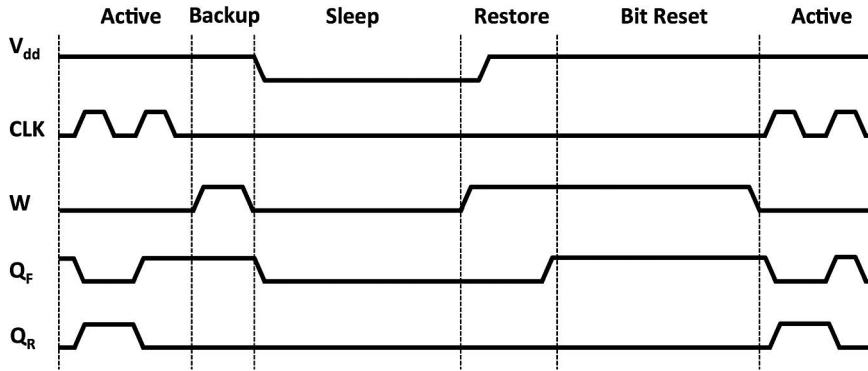

Fig. 3. Timing diagram of the VCMA-based NVFF.

which determine the different modes of operation. The timing diagram depicted in Fig. 3 shows the process in which signal W is sequenced during the active, backup, restore, and bit reset modes of operation. A VCMA-based NVFF behaves as a conventional FF during the active mode of operation, where V and W are held low to make the PMTJs inaccessible. Both PMTJs are therefore preserved from switching and remain in the P configuration during the active mode of operation.

B. Data Backup Mode in VCMA-Based NVFF

To perform a backup operation, depending upon the latched bit, one of the two PMTJs switches from P to AP, whereas the other PMTJ remains in the P configuration. During the backup operation, CLK and V are held low, whereas W is asserted high for duration t_p. Depending upon the latched bit, a voltage pulse V_p is applied across one of the PMTJs, whereas the other PMTJ is biased to zero. As shown in Fig. 4(a), when the latched bit is 0, Q_F is high and Q_R is low. By setting W to high for duration t_p, a voltage pulse of duration t_p and amplitude V_p is applied across the PMTJ$_2$. PMTJ$_2$ therefore switches from P to AP, whereas PMTJ$_1$ is zero biased and remains in P. As shown in Fig. 4(b), when the latched bit is 1, Q_F is low, and Q_R is high. By setting W to high for t_p, a voltage pulse of duration t_p and amplitude V_p is applied across the PMTJ$_1$. Hence, PMTJ$_1$ switches from P to AP, whereas PMTJ$_2$ is zero biased and remains in P.

C. Sleep Mode in VCMA-Based NVFF

The sleep mode of operation follows the backup mode of operation. During the sleep mode, where the FF is disconnected from power and ground, PMTJ$_1$ and PMTJ$_2$ retain a bit due to the nonvolatile nature of the MTJs. If the stored bit is 1, PMTJ$_1$ is AP, and PMTJ$_2$ is P. If the stored bit is 0, PMTJ$_1$ is P, and PMTJ$_2$ is AP.

D. Data Restore Mode in VCMA-Based NVFF

The data restore operation is performed when the FF is enabled to resume conventional operation. The data restore operation relies on the different current drive capabilities of PMTJ$_1$ and PMTJ$_2$. More specifically, during the data restore operation, PMTJ$_1$ and PMTJ$_2$ are at different magnetization configurations, exhibiting different electrical resistances. To perform the restore operation, as illustrated in Fig. 4(c), the power lines for both inverters I$_1$ and I$_2$ are pulled high, W is set high, and V is held low. Sweeping the power from 0 to V_{dd} charges the parasitic capacitance at storage nodes Q_R and Q_F through the P channel path of inverters I$_1$ and I$_2$. Q_R and Q_F simultaneously discharges, respectively, through PMTJ$_1$ and PMTJ$_2$.

If, for instance, the stored bit is 1, PMTJ$_1$ is AP, and PMTJ$_2$ is P. The current drive of PMTJ$_1$ is therefore weaker than PMTJ$_2$, resulting in Q_R more slowly discharging than Q_F, establishing $V_{Q_R} > V_{Q_F}$. Due to the positive feedback, the
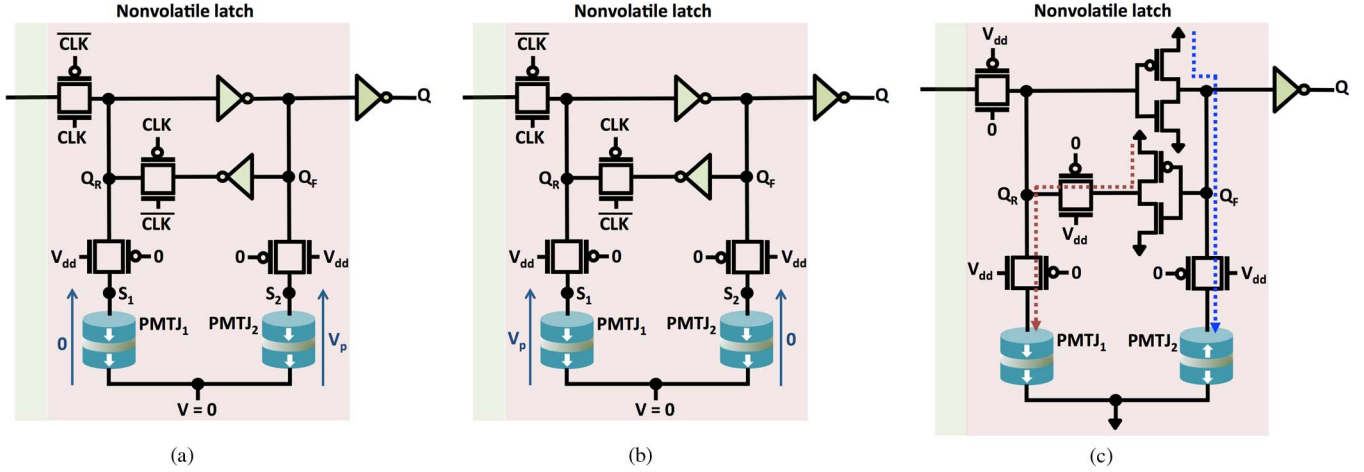
Fig. 4. Backup operations in the slave latch (a) at Q = '0', (b) at Q = '1', and (c) restore operation when $PMTJ_1$ ($PMTJ_2$) is P (AP).

regenerative action is enabled through the cross-coupled inverters [see Fig. 4(c)], settling V_{Q_R}, V_{Q_F}, and V_Q to, respectively, V_{dd}, 0, and V_{dd}.

E. Bit Reset Mode in VCMA-Based NVFF

During the active mode of operation, both PMTJs are in P. This situation is required because, as explained in Section III-B, the backup operation switches only one of the P configured PMTJs to AP. The AP configured PMTJ switches to the P configuration through the bit reset operation once the data are restored. As explained in Section III-D, at the completion of the restore mode of operation, if $PMTJ_1$ ($PMTJ_2$) is at AP, Q_R (Q_F) is at V_{dd}, and Q_F (Q_R) is at zero. The W signal, set to high during the restore operation, is held high for t_p after the restore operation is completed. As shown in Fig. 3, a voltage pulse of amplitude V_p and duration t_p is applied across the AP configured PMTJ, switching the device to P and completing the bit reset operation.

IV. SIMULATION RESULTS

Here, the operation of the VCMA-NVFF is compared with STT-NVFF [6] and SHE-NVFF [7]. Simulations use the Cadence/Spectre simulator and are based on the adaptive compact MTJ (ACM) model [17] for PMTJs, and the predictive transistor model (65-nm PTM) for CMOS transistors. The ACM model is a compact model of an MTJ switched by the STT mechanism, VCMA mechanism, or a hybrid STT-VCMA mechanism [17]. Furthermore, the ACM model considers the dynamic behavior of a self-heating junction and the effects of temperature on the behavior of an MTJ device [17]. The ACM model dynamically determines the resistance of an MTJ as a function of temperature, applied voltage, and orientation of the magnetization of the free layer with respect to the magnetization of the reference layer. The ACM parameters, as listed in Table I, are set according to the experimental parameters recently reported in [14], [15]. The gate length of the transistors is the minimum value specified by the technology models, i.e., 65 nm. Furthermore, the gate width of the N—and P-channel

TABLE II
COMPARISON AMONG NVFFS

		VCMA-NVFF	SHE-NVFF [7]	STT-NVFF [7]
Area		1.3x	1.28x	2.09x
Energy (fJ)	Backup	14.6	492.8	5004
	Restore	97.9	196.8	348.6
	Bit reset	14.6	N/A	N/A
Delay (ns)	Backup	0.83	6.43	29.45
	Restore	2	2	2
	Bit reset	0.83	N/A	N/A

transistors is, respectively, 260 and 500 nm. The supply voltage V_{dd} is 1.1 V.

The VCMA mechanism coherently switches an MTJ by temporal modulation of the magnetic anisotropy through a voltage pulse applied across the device [13]–[15]. Hence, the switching energy consumption is associated with only charging and discharging the parasitic capacitance of the MTJ [10], [13]–[15], [18]. The VCMA mechanism therefore has the potential to achieve sub-fJ switching energy consumption [18]. Certain physical impedances, however, impose some ohmic energy consumption by the device [14], [15].

Due to the high tunneling magnetoresistance (TMR), the current drive capability of a P-configured PMTJ is sufficiently higher than an AP-configured PMTJ, producing a fast restore operation (∼2 ns). Furthermore, to be driven by the VCMA mechanism, the PMTJs within an VCMA-NVFF need to exhibit a high resistance–area product (∼130 Ω μm^2 − ∼240 Ω μm^2), lowering the energy consumption during the restore mode of operation.

A comparison among different NVFFs is listed in Table II. The circuits include the VCMA-NVFF, the SST-NVFF [6], [7], and SHE-NVFF [7]. The bit reset operation makes the VCMA-NVFF able to write only one MTJ while backing up the data. In the previously proposed NVFFs [4]–[8], both MTJs are over written during the backup mode, despite being placed in the correct configuration (P or AP). Therefore, to provide a fair comparison between the VCMA-NVFF and the previously proposed most efficient STT-based and SHE-NVFFs, the energy consumption and delay of the bit-reset operation are added, respectively, to the energy consumption and delay of the data backup operation. Considering the data backup energy

TABLE III
TIMING CHARACTERISTICS OF THE VCMA-NVFF AND STANDARD D FF

		Temperature (°C)			Process				
		−55	27	85	SS	SF	TT	FS	FF
τ_{CQH}, τ_{CQL} (ps)	D FF	33.1, 36.5	51.0, 51.3	68.4, 67.9	64.1, 64.3	46.9, 47.4	51.0, 51.3	53.3, 55.3	40.1, 41.2
	NVFF	34.4, 37.2	53.9, 53.5	73.1, 70.6	67.3, 67.5	50.2, 49.4	53.9, 53.5	56.9, 57.5	42.4, 42.6
τ_{STH}, τ_{STL} (ps)	D FF	10.6, 5.6	15.1, 14.2	20.6, 23.0	18.3, 19.6	14.9, 12.6	15.1, 14.2	15.5, 17.0	12.6, 10.9
	NVFF	10.8, 5.8	15.5, 14.6	20.9, 23.5	18.6, 20.0	15.0, 13.1	15.5, 14.6	15.6, 17.2	12.8, 11.7
τ_{HTH}, τ_{HTL} (ps)	D FF	0.0, -8.2	-7.0, -9.4	-10.6, -6.5	-9.5, -8.8	-3.5, -9.8	-7.0, -9.4	-10.1, -8.1	-4.5, -8.6
	NVFF	0.0, -8.1	-6.6, -9.1	-10.2, -6.2	-9.0, -8.7	-3.0, -9.6	-6.6, -9.1	-9.7, -8.0	-4.2, -8.3

TABLE IV
ENERGY OF THE VCMA-NVFF

	Temperature (°C)			Process				
	−55	27	85	SS	SF	TT	FS	FF
Backup energy (fJ)	13.8	14.6	15.4	15.7	15.1	14.6	14.0	13.7
Restore energy (fJ)	86.4	97.9	105.1	103.9	101.5	97.9	93.8	91.9
Bit reset energy (fJ)	13.8	14.6	15.4	15.7	15.1	14.6	14.0	13.7

penalty imposed by the bit reset operation, the VCMA-NVFF offers more than a $171\times$ ($17\times$) improvement in data backup energy as compared with the most efficient STT-based NVFF (SHE-NVFF) [7]. Furthermore, considering the data backup delay penalty imposed by the bit reset operation, the VCMA-NVFF offers $\sim 17.5\times$ ($\sim 4\times$) improvement in backup delay as compared with the most efficient STT-based NVFF (SHE-NVFF) [7]. The area overhead of different NVFFs with respect to the reference D FF is also listed in Table II. The area overhead of the VCMA-NVFF is almost the same as the SHE-NVFF, increasing the cell area by up to $\sim 1.3\times$ of the area of a standard D FF.

The timing characteristics of the VCMA-NVFF as compared with the standard D FF is listed in Table III. τ_{CQH} and τ_{CQL} are the clock-to-output (Q) delay, τ_{STH} and τ_{STL} are the minimum setup time, and τ_{HTH} and τ_{HTL} are the minimum hold time. The last subscript in each index (L and H) denotes the logic level transferred to the Q node by switching the FF through the positive edge trigger of the clock. The degradation (increase) in the timing characteristics of the VCMA-NVFF as compared with the standard D FF is within 7%. The timing characteristics of the STT-NVFF have been reported only at room temperature and typical process conditions (TT) [6]. Furthermore, the timing characteristics of the SHE-NVFF have not been reported for any temperature or process corner conditions [7]. The degradation (increase) in timing characteristics for the VCMA-NVFF at TT process conditions is within 5.7%, smaller than the STT-NVFF (6%) [6].

V. CONCLUSION

A novel NVFF has been proposed where the latched data bit is backed up through the VCMA mechanism within an MTJ before the FF is disconnected from the power supply. Depending upon the polarity of the bit being backed up, one MTJ is coherently switched, enabling an ultra-energy-efficient data backup with subnanosecond backup time. Simulation results exhibit more than $342\times$ ($33.7\times$) improvement in data backup energy per bit, and more than $35.5\times$ ($7.7\times$) improvement in data backup delay per bit as compared with the most efficient STT-based NVFFs (SHE-based NVFF). Due to the high energy

efficiency (see Table IV), the proposed VCMA-based NVFF requires sufficiently short BETs, enabling effective fine-grain PG.

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