Dynamic and Short-Circuit Power of CMOS Gates Driving Lossless Transmission Lines

Yehea I. Ismail, Eby G. Friedman, *Senior Member, IEEE*, and Jose Luis Neves

***Abstract*—The dynamic and short-circuit power consumption of a complementary metal–oxide–semidconductor (CMOS) gate driving an inductance–capacitance (*LC*) transmission line as a limiting case of an *RLC* transmission line is investigated in this paper. Closed-form solutions for the output voltage and short-circuit power of a CMOS gate driving an *LC* transmission line are presented. A closed form solution for the short-circuit power is also presented. These solutions agree with circuit simulations within 11% error for a wide range of transistor widths and line impedances for a 0.25-μm CMOS technology. The ratio of the short circuit to dynamic power is shown to be less than 7% for CMOS gates driving *LC* transmission lines where the line is matched or underdriven. The total power consumption is expected to decrease as inductance effects becomes more significant as compared to a resistance–capacitance (*RC*)-dominated interconnect line.**

***Index Terms*—CMOS, dynamic, interconnect, LC, power dissipation, RC, RLC, short-circuit, transmission lines.**

I. Introduction

HISTORICALLY, interconnect has been modeled as a single lumped capacitance in the performance analysis of on-chip interconnects [1]–[6]. With the scaling of technology and increasing chip size, the crosssectional area of wires has scaled down while interconnect length has increased. The resistance of the interconnect has therefore become significant, requiring more accurate resistance–capacitance (RC) delay models [7]. Initially, the interconnect was modeled as a lumped RC circuit. To further improve accuracy, the interconnect is often modeled as a distributed RC circuit (as multiple T or Π sections) for those nets requiring increased accuracy [8], [9].

Currently, inductance is becoming more important with decreasing on-chip rise times and longer wire lengths [10]–[17]. Wide wires are frequently encountered in clock distribution networks and in data busses. These wires, often at the upper metal layers, are low resistance wires that can exhibit significant inductive effects [16], [17]. Furthermore, performance requirements are pushing the introduction of new materials, such as low resistivity copper interconnect [18]. In the limiting case, high temperature superconductors may possibly become commercially available [19]. More accurate *RLC* transmission line models are therefore becoming necessary in the analysis of VLSI-based interconnect.

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The *RC* model can be viewed as a limiting case of the *RLC* transmission line model where the inductance is considered to be negligible. This case has been thoroughly investigated and is well represented in the literature, e.g., [20]–[26]. The other limiting case is an inductance–capacitance (*LC*) transmission line where the resistance is negligible. This case approximates the low-loss lines encountered in multichip modules (MCM's) and printed circuit boards (PCB's). Although it is highly improbable that the resistance of an on-chip interconnect will become negligible in the near term, this *LC* analysis provides an upper limit for analyzing inductive effects in VLSI circuits. The behavior of an *RLC* transmission line case can therefore be bounded by analyzing the behavior of the *RC* and the *LC* cases.

The focus of this paper is the investigation of dynamic and short-circuit power in CMOS gates driving *LC* transmission lines. A closed-form solution for the output voltage of a CMOS gate driving an *LC* transmission line is presented in Section II. This solution is based on the alpha power law for deep submicrometer (DSM) CMOS technologies [27]. This solution is compared to the output voltage of a CMOS gate driving a lumped capacitive representation of a line. It is also shown in Section II that these two solutions become equivalent as the transition time of the signal at the input of the CMOS gate driving a transmission line becomes greater than twice the time of flight of the waves across the transmission line. The dynamic and short-circuit power consumption of a CMOS gate driving an *LC* transmission line is presented in Section III. The analysis in Section III is performed for the case where the transition time of the signal at the input of the CMOS gate driving a transmission line is smaller than twice the time of flight of the waves propagating across the transmission line. Finally, some conclusions are offered in Section IV.

II. Capacitive Approximation of a Lossless Transmission Line

A transmission line can be replaced by its characteristic impedance Z_0 for the period of time $0 < t < 2T_0$ where T_0 is the time of flight of the signals across the line [28]. An equivalent circuit of a CMOS inverter driving a lossless transmission line with a characteristic impedance $Z_0 = \sqrt{L_t/C_t}$ is shown in Fig. 1. For this equivalent circuit, the output voltage is given by the inverter output current multiplied by the characteristic impedance of the line. Ignoring the effect of the NMOS transistor for a falling input and assuming the PMOS transistor is saturated, the output current of the transistor does not depend on the output voltage (neglecting channel length

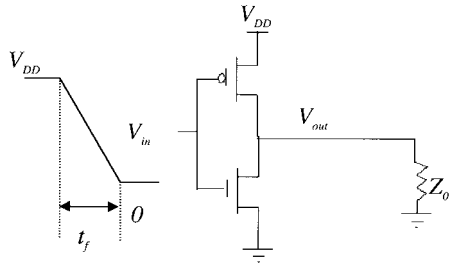

Fig. 1. Equivalent circuit of a CMOS inverter driving a lossless transmission line for a period of time $0 < t < 2T_0$.

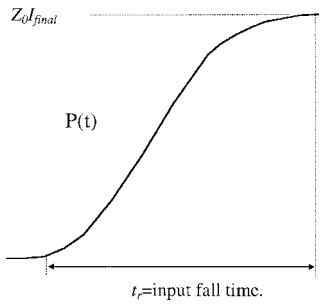

Fig. 2. The initial output voltage pulse generated by the inverter for the period of time $0 < t < 2T_0$.

modulation). Thus, the output voltage is

$$V_{\text{out}} = Z_0 I_{p\text{sat}} = P(t) \tag{1}$$

for the period of time $0 < t < 2T_0$. $I_{p\text{sat}}$ is the saturation current of the PMOS transistor and is

$$I_{p\text{sat}} = P_{Cp}\frac{W_p}{L_p}\left(V_{\text{DD}} - V_{\text{in}} - |V_{Tp}|\right)^{\alpha_p} \tag{2}$$

assuming the alpha power law is used to model the saturation current of a MOSFET [27] where P_C is a constant that characterizes the drive current of the transistor in saturation, W and L are the geometric width and length, respectively, of the transistor, and α is a constant between one (strong velocity saturation) and two (weak velocity saturation) [27]. V_{Tp} is the threshold voltage of the P-channel device and is negative for an enhancement mode device. p indicates the PMOS transistor and n indicates the NMOS transistor.

This current depends on the input voltage and has a final value of

$$I_{\text{final}} = P_{Cp}\frac{W_p}{L_p}(V_{\text{DD}} - |V_{Tp}|)^{\alpha_p} \tag{3}$$

which is reached when the input voltage reaches its final value of zero volts. This initial output voltage pulse is shown in Fig. 2. This pulse propagates across the line, reaches the open circuit (or small capacitor [29]), and reflects a signal of the same magnitude and sign back toward the CMOS inverter. Since the PMOS transistor is assumed to be in saturation, the transistor maintains an almost constant current which requires a current reflection coefficient of negative one. Therefore, the voltage reflection coefficient is one. Thus, after a time $2T_0$, the original signal that is launched at time zero is multiplied by three (the initial signal, the signal reflected at the load, and the signal reflected at the transistor). Under the above conditions, the output voltage is

$$V_{\text{out}} = P(t) + \sum_{i=1}^{n} 2P(t - 2iT_0) \quad \text{for } 2nT_0 < t < 2(n+1)T_0 \tag{4}$$

where $n = 1, 2, \ldots m$. m is the time at which the transistor is no longer saturated and enters the linear region. This behavior is illustrated in Fig. 3. The horizontal parts of the curve have voltage values given by

$$V_{\text{out}} = (2n+1)Z_0 I_{\text{final}}. \tag{5}$$

At the times $(2n+1)T_0$, the output voltage has the values given by (5) since these times fall in the middle of the periods $2nT_0 < t < 2(n+1)T_0$.

A transistor driving a lossless transmission line in the matched or underdriven case has an output voltage that follows the response of a transistor driving a capacitance C_L, as shown in Fig. 4. A CMOS gate is matched to a transmission line if the geometric widths of the transistors are finely adjusted to avoid reflections such that the output impedance of the CMOS gate is equal to the characteristic impedance of the line. The line is said to be underdriven if the widths of the transistors of the CMOS gate driving the transmission line are smaller than the transistor widths in the matched case such that the output impedance of the CMOS gate is greater than the characteristic impedance of the line. Since $T_0 = \sqrt{C_t L_t}$ and $Z_0 = \sqrt{L_t/C_t}$ [28] where L_t and C_t are the total inductance and capacitance of the line, respectively, the value T_0/Z_0 is equal to C_t. Thus, equating C_L to T_0/Z_0 or the total capacitance of the line, V_{out} becomes

$$V_{\text{out}} = I_{\text{final}}\frac{Z_0}{T_0}t \tag{6}$$

after the input voltage reaches its final value. If V_{out} is sampled at times $(2n+1)T_0$, the resulting expression for V_{out} is

$$V_{\text{out}} = (2n+1)Z_0 I_{\text{final}}. \tag{7}$$

This expression is exactly the same as (5). The equivalence of (7) and (5) demonstrates that the output voltage of a CMOS gate driving a capacitor equal to the total capacitance of a transmission line intersects the output voltage of the CMOS gate driving the transmission line at times $(2n+1)T_0$. Results from the IBM developed circuit simulator AS/X [30] based on a 0.25-μm CMOS technology are shown in Fig. 5. As the fall (rise) time of the signal at the input of the inverter increases, the slope of the rising (falling) portions of the transmission line response decreases, while the intersection points determined by the capacitance approximation remain the same. Thus, while the rise (fall) time of the input signal increases with respect to T_0, the capacitive approximation more accurately matches the transmission line model, as shown in Fig. 5. Once t_r becomes greater than $2T_0$, the horizontal portions of the response are no longer apparent and the two responses coincide. It can be shown that the assumption made here (a lossless transmission line behaves as a single lumped

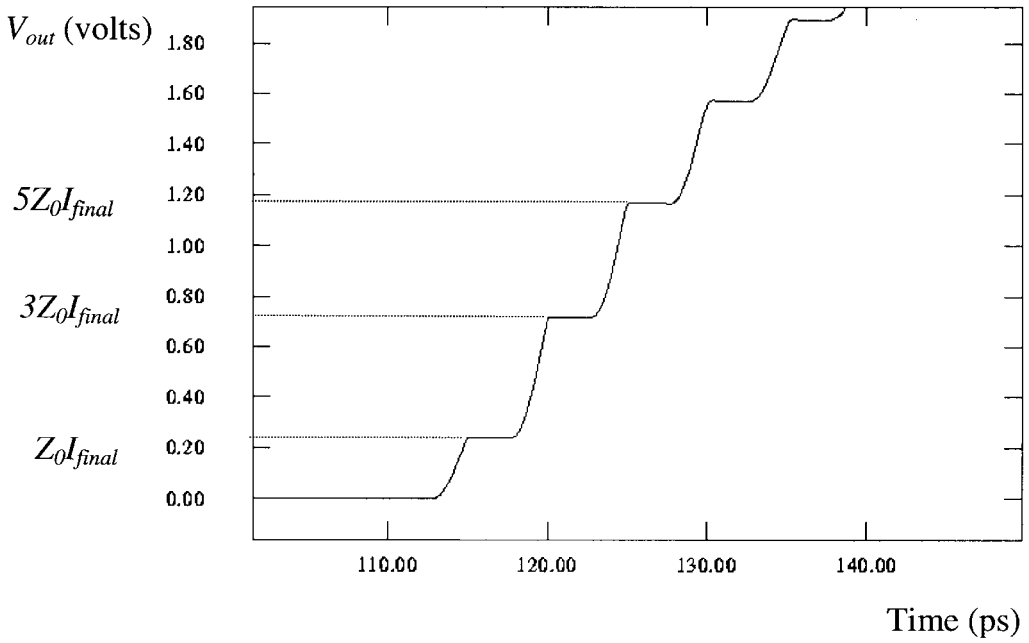

Fig. 3. Voltage at the output of a saturated transistor connected to an open circuit transmission line.

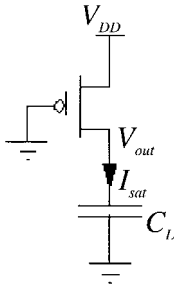

Fig. 4. A PMOS transistor driving a capacitive approximation of a lossless transmission line.

capacitor when $t_r > 2T_0$) for a saturated transistor holds when the transistor also operates in the linear region. This behavior can be seen in Fig. 5 at the exponential tail of the response at the end of the logical transition where the transistor enters the linear region. When the lumped capacitor response approaches the transmission line response when the transistor is saturated, the two responses also approach each other in the linear region. This behavior can be qualitatively interpreted by noting that the inductive impedance is given by $j\omega L$ and the capacitive impedance is given by $1/j\omega C$ where ω is the radial frequency. When the frequency decreases (the rise time increases), the capacitive impedance becomes large compared to the inductive impedance which make the inductance negligible, permitting the line to be treated as a single lumped capacitor.

This behavior makes the study of a CMOS gate driving a lossless transmission line unnecessary when $t_r > 2T_0$ because the transmission line model can be simply replaced by a capacitor equal to the total capacitance of the line. In addition, on-chip signal transition times are decreasing in next-generation VLSI circuits, while wires are becoming longer (which increases T_0). Therefore, the more important regime of interest when analyzing the effects of on-chip inductances occurs when $t_r < 2T_0$ [31]. Thus, it is assumed that $t_r < 2T_0$ in the remaining analysis presented in this paper.

III. Dynamic and Short-Circuit Power

The dynamic power consumption can be derived from analyzing the behavior of a transmission line interacting with a CMOS gate. This topic is discussed in Section III-A. It is shown that the dynamic power consumption of a CMOS gate driving a transmission line is the same as the dynamic power consumption of a gate driving a capacitor equal to the total capacitance of the transmission line. In Section III-B the short-circuit power consumption of a CMOS gate driving a lossless transmission line is investigated for the regime where $t_r < 2T_0$. The short-circuit to dynamic power ratio is examined in Section III-C and compared to the same ratio when the load is a simple capacitor or an *RC* line.

A. Dynamic Power

A MOS transistor driving a lossless transmission line launches an initial voltage wave with a value $V_1 = I_{\rm sat}Z_0$. This initial voltage signal propagates toward the load and reaches the load at time T_0. Assuming the load is open or is a small capacitor, a voltage wave propagates back toward the transistor with a magnitude V_1 and a current wave $-I_{\rm sat}$. This wave returns to the MOS transistor at time $2T_0$. At that moment, the current of the two waves cancels and the voltage adds to $2V_1$. For this period of time (from zero to $2T_0$), a current of V_1/Z_0 is drawn from the power supply. At $t = 2T_0$, a new voltage wave is initiated with a value $V_2 = I(V_{\rm DD} - 2V_1 - V_2)Z_0$ where $I(V_{\rm DD} - 2V_1 - V_2)$ is the current of the transistor with $V_{\rm out} = 2V_1 + V_2$. The cycle is repeated and a current V_2/Z_0 is drawn from the supply for the period of time from $2T_0$ to $4T_0$. This cycle repeats until the voltage at the output of the transistor reaches $V_{\rm DD}$. The last voltage wave is assumed to be V_n where n is the number of traversals of the line required to reach a steady state. The number of iterations can, in general, be infinite or only one in the perfectly matched case. The output current $I_{\rm DS}$ of a

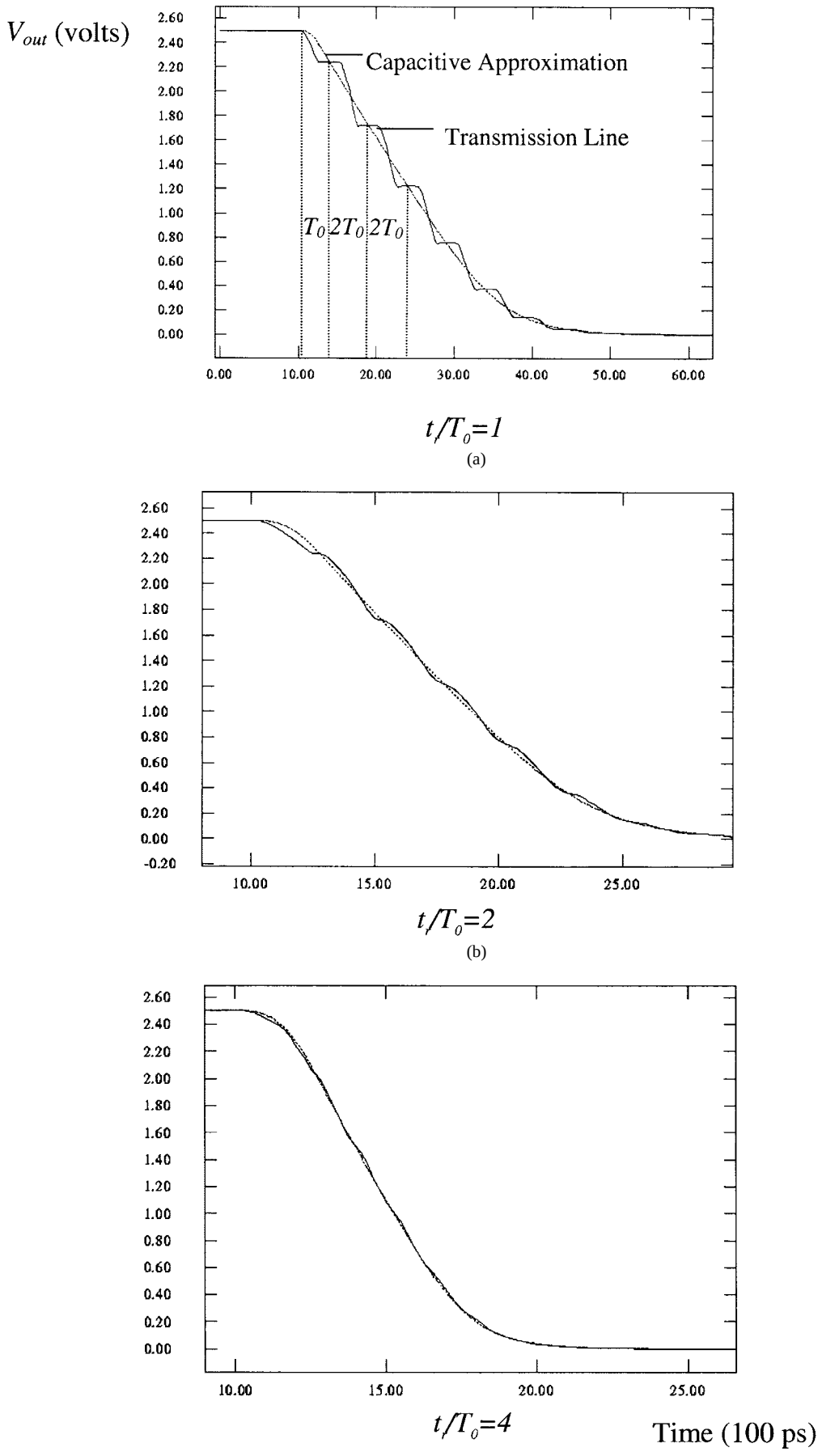

Fig. 5. Effect of rise time on the capacitive approximation of a transmission line. Ratios of t_r/T_0 of 1, 2, and 4 are shown in (a), (b), and (c), respectively.

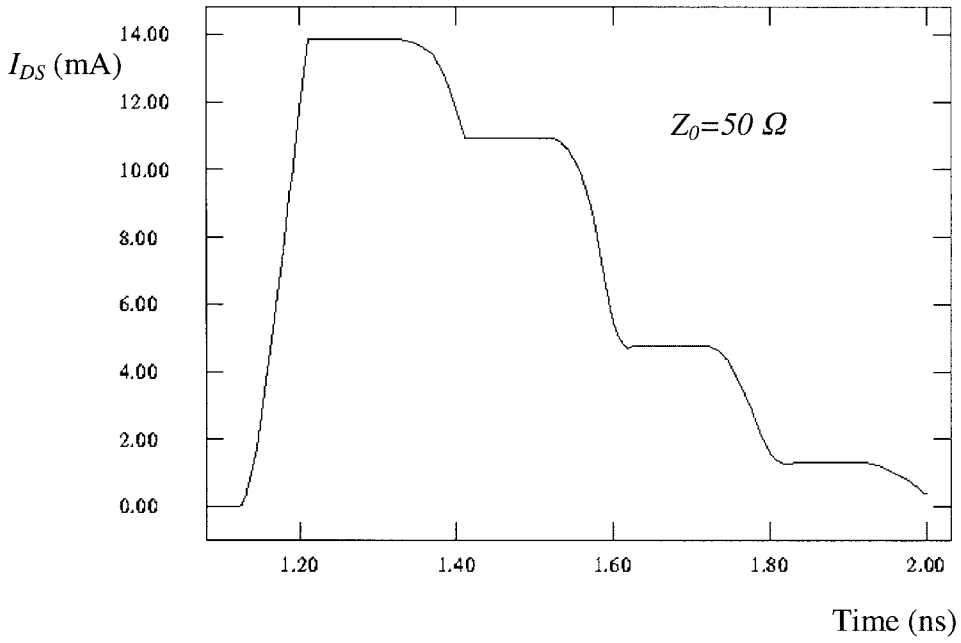

Fig. 6. Source-to-drain current of a PMOS transistor driving a lossless transmission line.

PMOS transistor as a function of time pulling up the output voltage is shown in Fig. 6.

Summing these voltages, the following condition is satisfied:

$$V_1 + V_2 + \cdots + V_n = \frac{V_{\rm DD}}{2} \tag{8}$$

since the final voltage is $V_{\rm DD}$ once the transient response reaches the steady state value. From this description, the energy taken from the power supply for a low to high transition is

$$E_{\rm dyn}/{\rm Cycle} = V_{\rm DD} \cdot \frac{2T_0}{Z_0} \cdot (V_1 + V_2 + \cdots + V_n). \tag{9}$$

Using (8) and noting that T_0/Z_0 is equal to C_t, the total capacitance of the line (9) evaluates to

$$E_{\rm dyn}/{\rm Cycle} = C_t \cdot V_{\rm DD}^2. \tag{10}$$

This energy is stored in the capacitance of the line and is passed to ground in the next high-to-low transition as the line is discharged. Thus, (10) represents the energy per cycle of the output. The dynamic power is therefore

$$P_{\rm dyn} = C_t \cdot V_{\rm DD}^2 f \tag{11}$$

where f is the frequency of the signal at the output of the CMOS gate. This formula is the same as the dynamic power for a capacitor of the same value as the total capacitance of the line [31].

B. Short-Circuit Power

The other component of switching transient power in CMOS circuits is the short-circuit power that occurs when both the NMOS and PMOS transistors conduct current at the same time. This power is consumed during the rise (fall) time of the input signal when the input signal is between V_{Tn} and $V_{\rm DD} + V_{Tp}$ (where V_{Tn} is the threshold voltage of the N-channel device). The case considered here is when the rise time is less than twice the propagation delay across the line ($t_r < 2T_0$), as discussed in Section II. In this case, the reflections do not affect the short-circuit power because the signal returns to the driver after the input signal has reached its final value. Under this condition, the transmission line appears as a resistance with a value Z_0. The equivalent circuit of a CMOS inverter driving a lossless transmission line for the period of time zero to T_0 is shown in Fig. 7 where C_0 is the intrinsic drain capacitance of a CMOS inverter.

The differential equation describing the Kirchoff's current law (KCL) for the output node is

$$(I_n - I_p) = C_0 \cdot \frac{d(V_{\rm DD} - V_{\rm out})}{dt} + \frac{(V_{\rm DD} - V_{\rm out})}{Z_0} \tag{12}$$

where I_n and I_p are the currents of the NMOS transistor and the PMOS transistor, respectively. Note that the resistance Z_0 representing the transmission line is connected between $V_{\rm DD}$ and $V_{\rm out}$ because the line is assumed to be charged to $V_{\rm DD}$ and that $d(V_{\rm DD} - V_{\rm out})/dt = -d(V_{\rm out})/dt$. The NMOS transistor is assumed to be in the saturation region during the rise time of the input signal. This assumption is justified because the output is initially $V_{\rm DD}$, which makes $V_{{\rm DS}n}$ large where $V_{{\rm DS}n}$ is the drain-to-source voltage of the NMOS transistor. Also, since the input is still rising, $V_{{\rm GS}n}$ is smaller than $V_{\rm DD}$ where $V_{{\rm GS}n}$ is the gate-to-source voltage of the NMOS transistor. Thus, the saturation condition in [27], $V_{{\rm DS}n} > P_{Vn}(V_{{\rm GS}n} - V_{Tn})^{\alpha_n/2}$, is satisfied during the rise time of the input signal. P_{Vn} is a constant that characterizes the current drive capability of the NMOS transistor when operating within the linear region [27]. This assumption is further accurate in deep submicrometer technologies because of the early saturation phenomenon [27]. This aspect can be understood by noting that α decreases for deep submicrometer devices and approaches one, which satisfies the aforementioned saturation condition for a larger range of the output voltage. On the other hand,

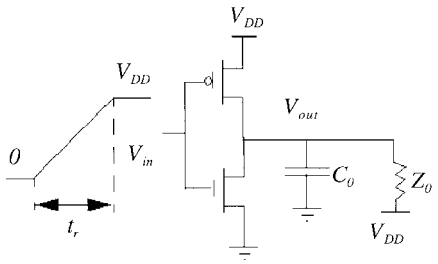

Fig. 7. Equivalent circuit of a CMOS driver driving a lossless transmission line for $0 < t < 2T_0$.

the PMOS transistor starts in the linear region and then enters the saturation region. The short-circuit current describes the current through the PMOS transistor during a rising input. The signal at the input of the CMOS driver is

$$V_{\text{in}} = kt = \frac{V_{\text{DD}}}{t_r}t \tag{13}$$

before the input signal reaches V_{DD} (i.e., $t < V_{\text{DD}}/k$).

Based on the alpha power law, when the PMOS transistor is in saturation, the short-circuit current is

$$I_{\text{SC}} = P_{Cp} \cdot \frac{W_p}{L_p} \cdot (V_{\text{DD}} - kt - |V_{Tp}|)^{\alpha_p}. \tag{14}$$

When the PMOS transistor operates in the linear region, the solution of (12) appears intractable because $V_{\text{DS}p}$ (the drain-to-source voltage of the PMOS transistor) is a function of V_{out}. Therefore, the current from the output capacitor C_0 is assumed to be small compared to the current from the transmission line. This assumption is accurate in deep submicrometer technologies because the transistors have small parasitic capacitances and high current levels. Also, Z_0 is typically in the range of 30 to 60 Ω, see, e.g., [14], [17], which results in large currents as compared to the current sourced by the parasitic capacitance C_0. Under this assumption and using the alpha power law model, the output voltage is

$$V_{\text{out}} = V_{\text{DD}} - \frac{Z_0 \cdot P_{Cn} \cdot \frac{W_n}{L_n} \cdot (kt - V_{Tn})^{\alpha_n}}{1 + \frac{P_{Cp}}{P_{Vp}} \cdot \frac{W_p}{L_p} \cdot (V_{\text{DD}} - kt - |V_{Tp}|)^{\frac{\alpha_p}{2}} \cdot Z_0} \tag{15}$$

for the time $0 < t < t_r$ where $t_r < 2T_0$ according to the assumption made in Section II. Noting that $V_{\text{DD}} - V_{\text{out}}$ is V_{SD} of the PMOS transistor, the short-circuit current of a CMOS inverter loaded by an *LC* transmission line is

$$I_{\text{SC}} = \frac{Z_0 \cdot P_{Cn} \cdot \frac{W_n}{L_n} \cdot (kt - V_{Tn})^{\alpha_n}}{\frac{P_{Vp}}{P_{Cp}} \cdot \frac{L_p}{W_p} \cdot (V_{\text{DD}} - kt - |V_{Tp}|)^{-\frac{\alpha_p}{2}} + Z_0}. \tag{16}$$

A CMOS gate driving a transmission line can be most efficiently characterized by the matching factor λ, where

$$\lambda = \frac{2S_pW_pZ_0}{V_{\text{DD}}} \tag{17}$$

and S_p is a technology-dependent constant. A detailed derivation of λ is given in the Appendix. When $\lambda = 1$, the transistor is optimally matched to the transmission line. If λ is less than one, the transmission line is underdriven and the response suffers from a slow output rise time. If λ is greater than one, the transmission line is overdriven and the response suffers from overshoots and undershoots that can cause reliability problems. If the overshoots and undershoots are sufficiently large, logical errors can occur. Voltages higher than the supply voltage and lower than ground create large electric fields that can deteriorate the oxide and increase hot electron effects. In addition, out-of-rail voltages can forward bias the junctions between the drain and source and the substrate, the n well, or the p well. When these junctions are forward biased, current flows directly into the wells or the substrate. This behavior is undesirable because it wastes current, dissipating extra power, and can induce other reliability problems within the substrate. Thus, the range defined by $0.3 < \lambda < 1.6$ is arbitrarily chosen to represent the range of interest characterizing practical matching conditions. The analytical solutions of (14) and (16) are compared to AS/X simulations in Fig. 8, assuming $t_r = 100$ ps and using λ as a design parameter. The characteristic impedance of the line Z_0 is kept constant while the PMOS transistor width W_p is varied to change λ. The analytical solution shows good agreement with the circuit simulations for a wide range of λ.

The short-circuit energy per transition can be calculated from

$$E_{\text{SC}}/\text{Transition} = \text{Area}_{\text{SC}} \cdot V_{\text{DD}} \tag{18}$$

where Area_{SC} (in coulombs) is the area under the short-circuit current curve. This area can be approximated by a triangle [22] whose base is given by $(V_{\text{DD}} - V_{Tn} + V_{Tp})t_r/V_{\text{DD}}$ and height is given by I_{peak} (the maximum point on the short-circuit current curve). Thus, the short-circuit energy per transition is

$$E_{\text{SC}}/\text{Transition} = \frac{I_{\text{peak}}}{2}(V_{\text{DD}} - V_{Tn} - |V_{Tp}|)t_rK_c \tag{19}$$

where K_c is a correction factor. Note in Fig. 8 that the analytical solution deviates from the simulated results in a consistent way at the point of intersection of the saturated curve and the linear curve. This deviation is due to the nonmonotonic nature of the alpha power law model used to characterize the devices. Due to this consistent error at the saturation/linear break point, a constant correction factor K_c is used and calibrated at $\lambda = 1$.

I_{peak} can be calculated by equating (14) and (16). Alternatively, I_{peak} can be calculated as

$$I_{\text{peak}} - K(\lambda)W_p \tag{20}$$

where $K(\lambda)$ is determined from varying λ and calculating $I_{\text{peak}}/W_p \cdot K(\lambda)$ for a specific 0.25-μm CMOS technology is plotted in Fig. 9.

$K(\lambda)$ quantifies in I_{peak} the effect of the output waveform shape on the short-circuit current. Note that $K(\lambda)$ saturates to an asymptotic value. This behavior can be explained by observing how the shape of the output signal varies with λ in Fig. 10. Note that the shape of the output voltage waveform depends heavily on λ for small λ, and this dependence saturates as λ increases. The short-circuit current depends upon the output voltage waveform because the drain-to-source voltage across the PMOS transistor is dependent on V_{out}. The gate-to-source voltage of the PMOS transistor depends only on

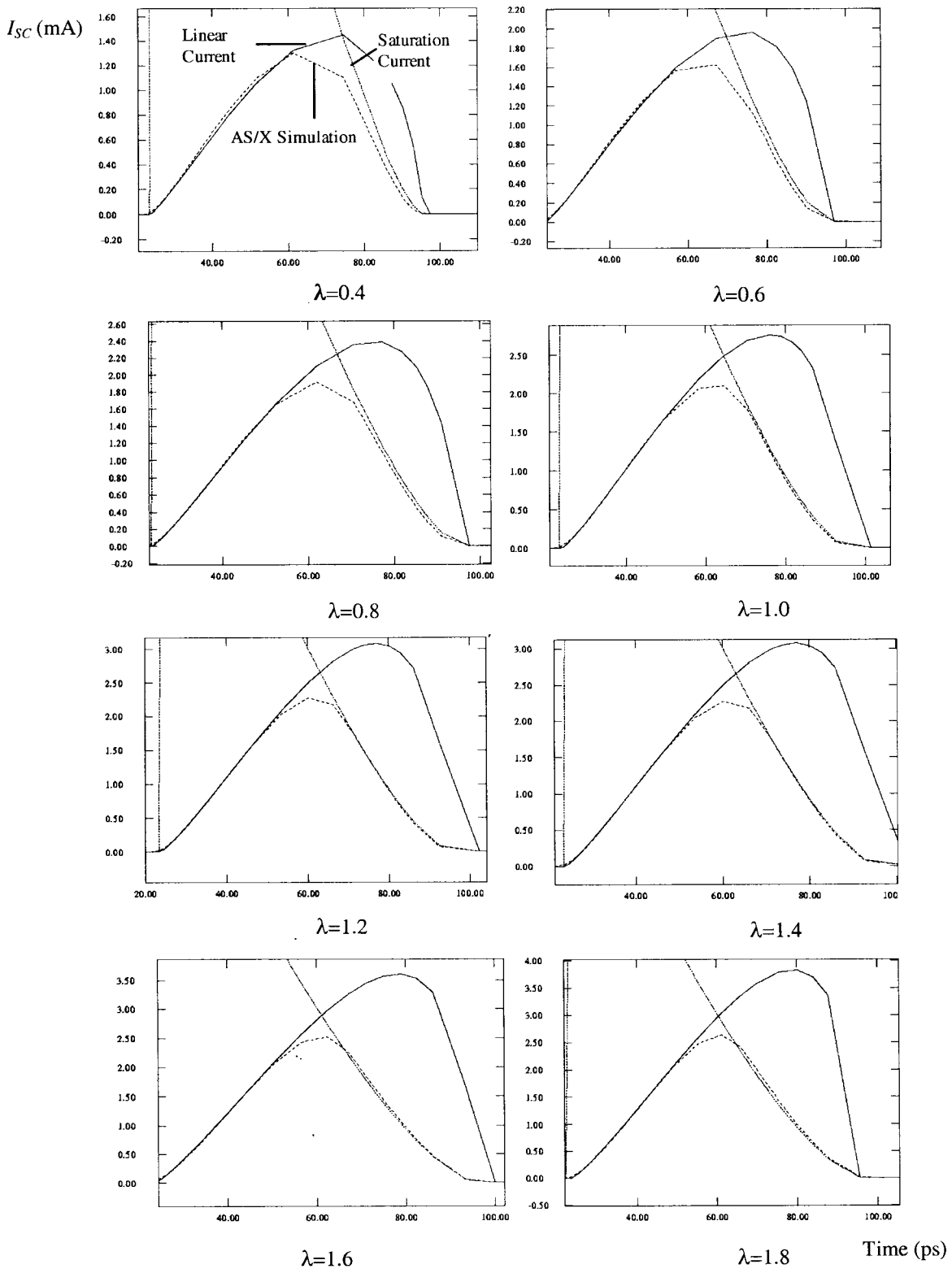

Fig. 8. Analytical solutions of the short-circuit current in (14) and (16) compared to AS/X simulations for $\lambda = 0.4, 0.6, 1.0, 1.2, 1.4, 1.6$, and 1.8. The AS/X curve is denoted by dashes, (14) is denoted by dots, and (16) is solid.

the input signal of the transistor (since the source is connected to the power supply). The output voltage with respect to the input voltage is determined by λ, as shown in Fig. 10. The peak current of the PMOS transistor is completely determined by λ and the geometric width of the PMOS transistor W_p, as given by (20). The transition time of the input signal results only in a shift of the time at which the peak current occurs without changing the magnitude of the peak current. The AS/X circuit simulator is used to quantify the accuracy of these analytic equations, such as the comparison of (19) with AS/X in Table I. The analytical solution shows good agreement (less than 1% error for $\lambda \geq 1$) with the circuit simulations for a wide

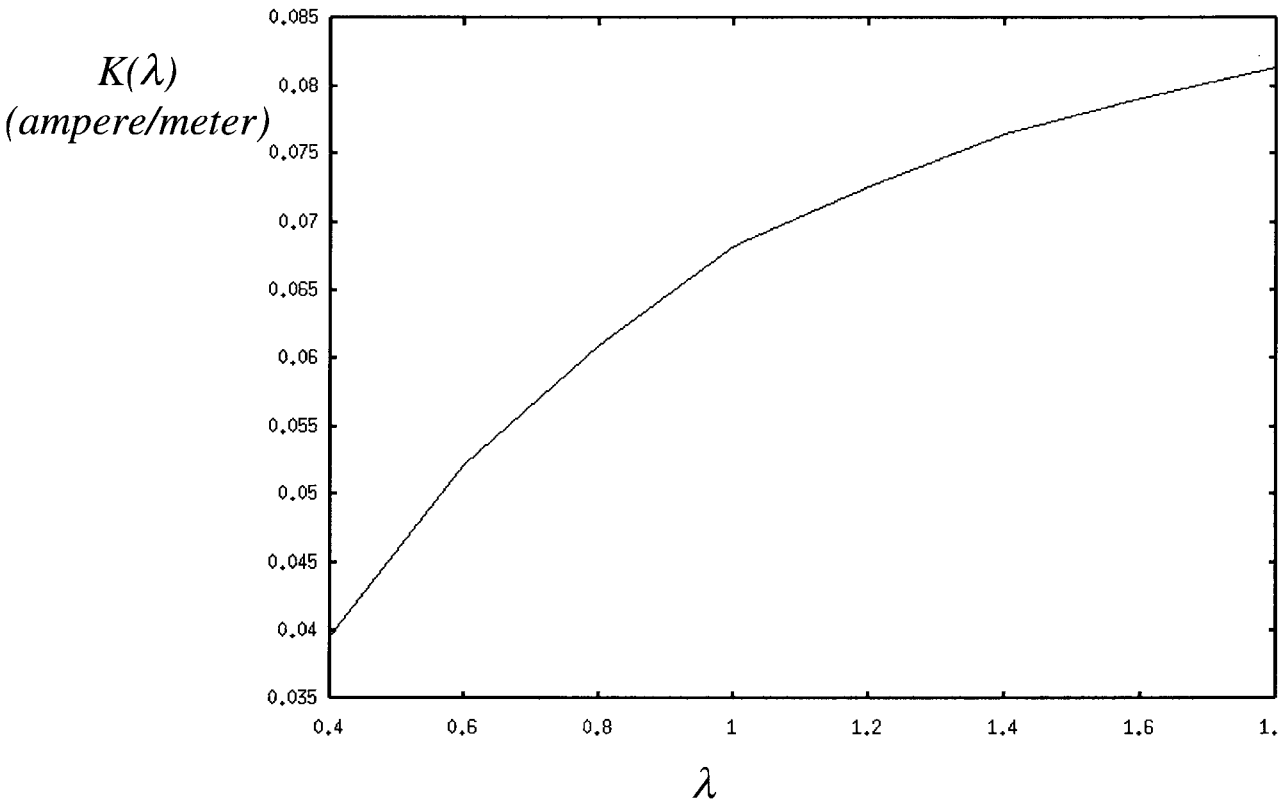

Fig. 9. $K(\lambda)$ versus λ.

TABLE I
AS/X SIMULATIONS COMPARED TO ANALYTICAL SOLUTION FOR E_{SC}/TRANSITION (IN JOULES)

λ	AS/X Simulation x10^{-15}	Analytical x10^{-15}	% Error
0.4	131.20	116.00	11.00
0.6	161.45	152.50	5.50
0.8	182.77	178.95	2.09
1.0	199.60	199.60	0.00
1.2	212.55	212.30	0.12
1.4	224.55	223.20	0.60
1.6	231.93	231.37	0.24
1.8	239.68	238.20	0.62

range of λ and exhibits a maximum error of 11% for small λ [31].

C. Short-Circuit to Dynamic Power Ratio

Assuming a symmetric CMOS gate, the short-circuit power is

$$P_{\mathrm{SC}} = I_{\mathrm{peak}}(V_{\mathrm{DD}} - V_{Tn} - |V_{Tp}|)t_r f. \tag{21}$$

As described previously, the dynamic power is

$$P_{\mathrm{dyn}} = \frac{T_0}{Z_0} \cdot V_{\mathrm{DD}}^2 f. \tag{22}$$

Dividing (21) by (22), the magnitude of the dynamic power can be compared to the magnitude of the short-circuit power. The resulting ratio is

$$\frac{P_{\mathrm{SC}}}{P_{\mathrm{dyn}}} = K(\lambda)\lambda \cdot \frac{(V_{\mathrm{DD}} - V_{Tn} - |V_{Tp}|)}{V_{\mathrm{DD}}} \frac{t_r}{T_0} \cdot \frac{K_c}{2S_p}. \tag{23}$$

The ratio between the short-circuit power and the dynamic power depends upon the matching condition λ of the transmission line impedance to the output impedance of the CMOS gate and the ratio between the rise time of the input signal to the time of flight of the waves propagating across the transmission line (t_r/T_0). The dependence on the supply voltage is fairly weak. The dependence only exists if the supply voltage and the threshold voltages scale differently. The dependence of the short-circuit to dynamic power ratio on λ is shown in Fig. 11. As the matching condition moves from underdriven to matched to overdriven, the short-circuit to dynamic power ratio increases. This ratio is less than 7% for the matched $(\lambda = 1)$ and underdriven cases $(\lambda < 1)$. This low ratio is due to the small voltage step in the output voltage while the input signal is still changing, as can be seen from Fig. 10. In the matched case, the input signal transitions approximately twice as fast as the output signal transitions since the input signal transitions from zero to V_{DD} at the same time as the output signal transitions from zero to $V_{\mathrm{DD}}/2$. This characteristic explains the low short-circuit to dynamic power ratio in a matched or underdriven circuit. Therefore, it is preferable to not overdrive the line (i.e., make $\lambda > 1$) in order to decrease the short-circuit power. The classical design criterion for driving a capacitive load is to maintain equal input and output transition times, which gives rise to a short-circuit power of approximately 20% of the dynamic power [3]. For *RC* loads, the $P_{\mathrm{SC}}/P_{\mathrm{Dyn}}$ ratio is even greater because the voltage drop across the load resistance makes the source-to-drain voltage large once the transistor begins to switch.

The maximum value of t_r/T_0 to exhibit nontrivial inductance effects is two. If t_r/T_0 is larger than two, the

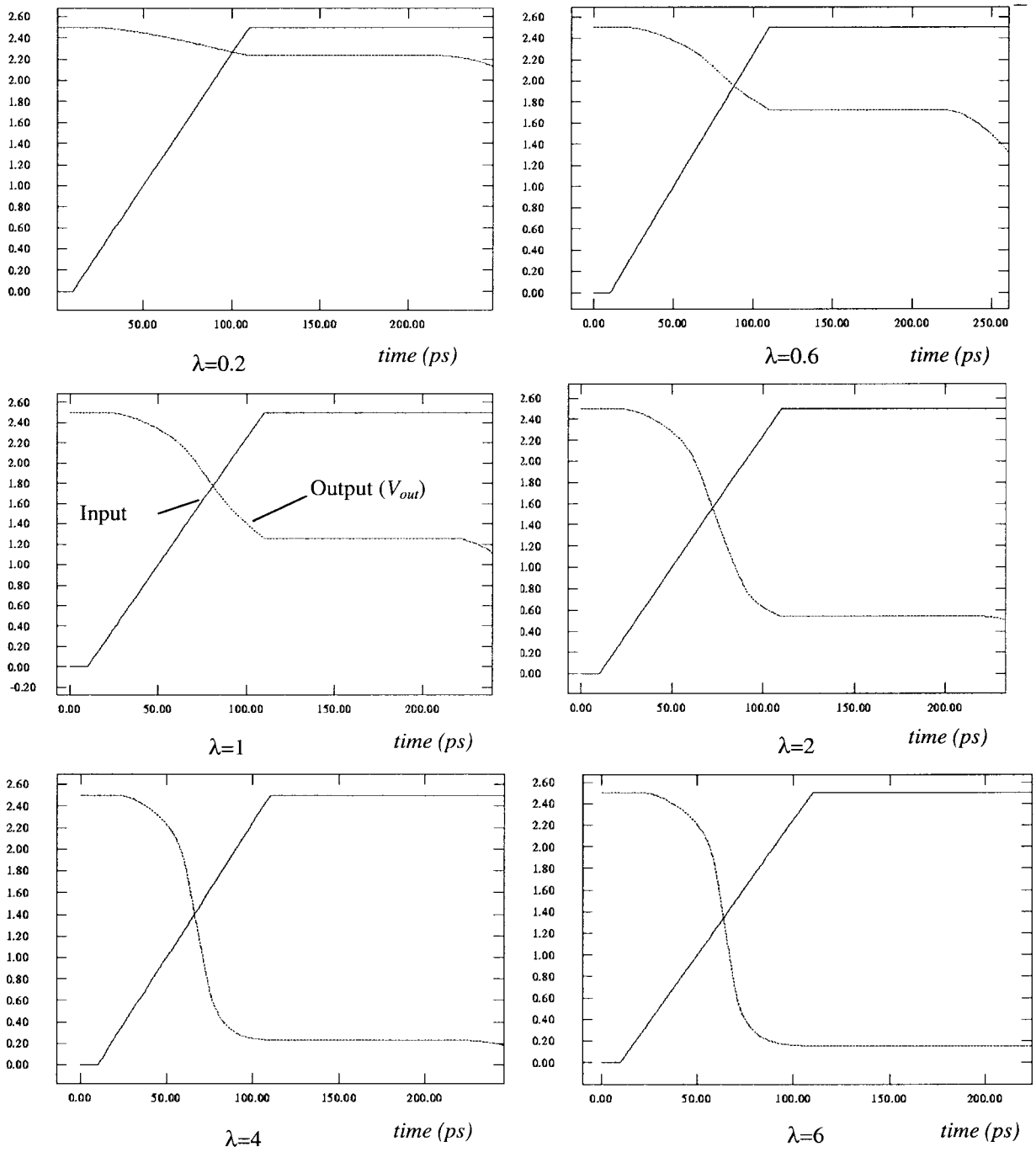

Fig. 10. The dependence of the output voltage on λ for $\lambda = 0.2, 0.6, 1.0, 2.0, 4.0,$ and 6.0.

transmission line can be approximated by a capacitor, as is illustrated in Section II. As the rise time of the input signal t_r increases, the short-circuit power increases since there is more time for the short-circuit current to flow. The rise time t_r does not affect the dynamic power and thus increasing t_r increases the ratio of the short-circuit power to the dynamic power. Dynamic power increases with increasing T_0 because the total capacitance of the line is T_0/Z_0. Thus, as T_0 increases, the capacitance of the line increases linearly, which increases the dynamic power linearly. The short-circuit power is not affected by T_0 as long as T_0 is greater than half the input rise time, making the ratio of the short-circuit power to the dynamic power decrease as T_0 is increased.

Finally, note that the dynamic power depends only on the total capacitance of the line and does not depend on the interconnect model. Therefore, the following statement canbe made: "The total power consumption of CMOS gates decreases as inductance affects increase." This is physically understandable since, unlike resistance, inductance stores and releases the energy without dissipating energy.

IV. Conclusion

A closed-form solution for the output voltage of a CMOS gate driving a lossless transmission line is presented. Transmission line effects are shown to be insignificant when the

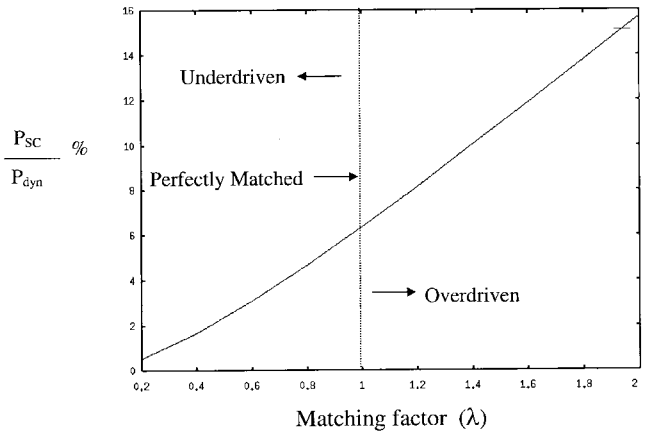

Fig. 11. Dependence of the short-circuit to the dynamic power ratio on λ.

transition time of the input signal at the CMOS gate driving a transmission line is greater than twice the time of flight of the signals across the line. The dynamic and short-circuit power consumed by a CMOS gate driving a lossless transmission line is investigated. The dynamic power of a CMOS gate driving a lossless transmission line is shown to be the same as that of a CMOS gate driving a capacitor equal to the total capacitance of the line. A closed-form solution for the short-circuit power is presented that agrees with circuit simulations within 11% error for a wide range of the matching factor λ. An expression for the short-circuit to dynamic power ratio is presented that shows that the short-circuit power is below 7% of the dynamic power for $\lambda \leq 1$. Thus, the short-circuit power for the case of an *LC* load is much less than that of the case of an *RC* load. In the case of an *RLC* load, the short-circuit power is in the middle, greater than the case of an *LC* load, but less than the case of an *RC* load.

Appendix
Matching Conditions of a CMOS Gate Driving a Lossless Transmission Line

To calculate the transistor widths for the matched condition, an understanding of the nature of the signal propagation across a lossless transmission line is necessary. When the transistor is first turned on, the transmission line appears as a resistor with a value Z_0. This situation is shown in Fig. 12. The initial voltage wave that is launched into the transmission line (V_{initial}) can be determined by equating the current from the transistor with the current through Z_0. The gate-to-source voltage of the PMOS transistor is $-V_{\text{DD}}$ and the drain-to-source voltage is $V_{\text{initial}} - V_{\text{DD}}$. Thus, the current of the transistor is a function of V_{DD} and V_{initial}. V_{initial} can be calculated from

$$I_{\text{ds}}[V_{\text{DD}}, V_{\text{initial}}] = \frac{V_{\text{initial}}}{Z_0} \tag{24}$$

where $I_{\text{ds}}[V_{\text{DD}}, V_{\text{initial}}]$ is the transistor output current and is a function of V_{DD} and V_{initial}.

The signal at the input of the transmission line does not reach the value V_{initial} directly since the output capacitor in parallel with Z_0 requires some time to charge to V_{initial}. This time is dependent on the intrinsic delay of the technology and is typically smaller than twice the time of flight of the signals

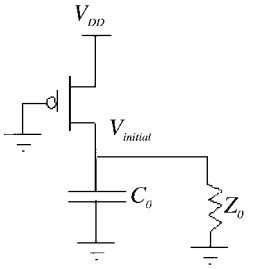

Fig. 12. A PMOS transistor driving a lossless transmission line. This circuit is the equivalent circuit of a CMOS inverter driving a lossless transmission line for the period of time $0 < t < 2T_0$.

propagating across the transmission line, thereby permitting the effect of the output capacitance to be neglected. The signal propagates along the transmission line and takes a time T_0 to reach the load impedance. At the load the signal reaches a steady-state value of two times V_{initial} due to the reflection at the load capacitance [29]. This voltage doubling occurs since the capacitor appears as an open circuit at steady state. Assuming that the incident wave V_{initial} is a step input, the voltage across the load capacitor is [29]

$$V_c = 2V_{\text{initial}}\left[1 - e^{\left(\frac{-t}{Z_0 C_L}\right)}\right]. \tag{25}$$

Thus, the time required to reach the steady-state value of $2V_{\text{initial}}$ depends on the time constant Z_0C_L. If this time constant is much less than $2T_0$, the effect of the load capacitance is negligible. Typically, this time constant is in the order of a few picoseconds and is sufficiently small to neglect the effects of the load capacitance [17].

The required condition for matching is launching an initial voltage $V_{\text{initial}} = V_{\text{DD}}/2$. This voltage wave propagates across the line and is totally reflected at the load after a period of time T_0. The reflected wave of magnitude $V_{\text{DD}}/2$ propagates from the load back toward the transistor. As this wave propagates back toward the source, the signal adds to the initial voltage wave, charging the line to V_{DD}. When this reflected wave reaches the transistor at time $2T_0$, the drain voltage of the PMOS transistor reaches V_{DD} and $V_{\text{DS}p}$ reaches zero volts. Thus, the transistor no longer conducts any current and the system becomes stable. This condition is illustrated in Fig. 13 for a CMOS inverter driving a lossless transmission line with $V_{\text{DD}} = 5$ V.

To determine the widths of the transistors required to satisfy the matching condition, (24) is solved with $V_{\text{initial}} = V_{\text{DD}}/2$. Using the alpha power law model to characterize the MOS transistors in the saturation region, (24) evaluates to

$$P_{Cp}\frac{W_p}{L_p}(V_{\text{DD}} - |V_{Tp}|)^{\alpha_p} = \frac{V_{\text{DD}}}{2Z_0}. \tag{26}$$

The geometric widths of the transistors of a CMOS inverter that satisfy the matched condition are

$$W_p = \frac{V_{\text{DD}}}{2Z_0 S_p}, \tag{27}$$

$$W_n = \frac{V_{\text{DD}}}{2Z_0 S_n} \tag{28}$$

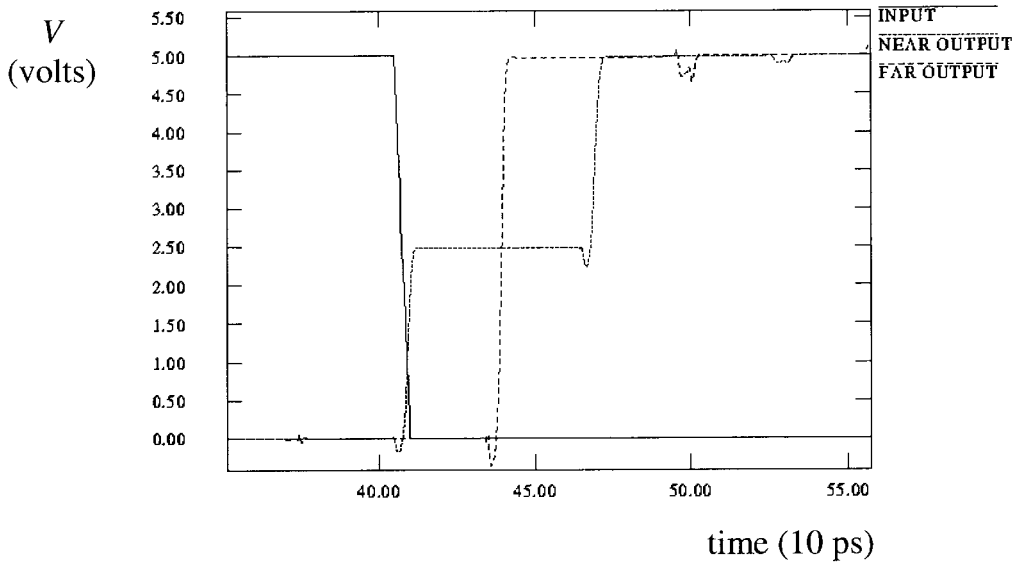

Fig. 13. AS/X simulations of a matched inverter driving an ideal transmission line.

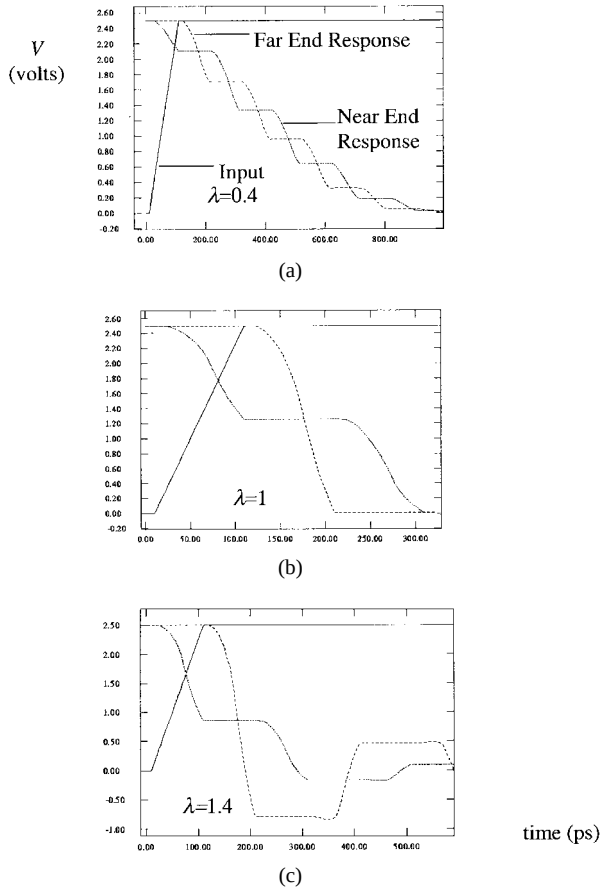

Fig. 14. AS/X simulations of a CMOS inverter driving an ideal transmission line for several values of λ, depicting the (a) underdriven, (b) matched, and (c) overdriven cases.

where S_p and S_n are technology-dependent parameters given by

$$S_p = \frac{P_{Cp}}{L_p}(V_{\rm DD} - |V_{Tp}|)^{\alpha_p}, \tag{29}$$

$$S_n = \frac{P_{Cn}}{L_n}(V_{\rm DD} - V_{Tn})^{\alpha_n}. \tag{30}$$

The assumption that the transistors operate in the saturation region is correct for deep submicrometer technologies because of the early saturation phenomenon [27]. The AS/X simulations shown in Fig. 13 demonstrate the accuracy of these equations and exhibit near-perfect matching between the MOS transistors and the lossless (or low-loss) transmission lines.

A useful parameter that characterizes the input/output relationship of a CMOS gate driving a lossless transmission line can be defined based on (27) as

$$\lambda_p = \frac{2S_pW_pZ_0}{V_{\rm DD}} \tag{31}$$

$$\lambda_n = \frac{2S_nW_nZ_0}{V_{\rm DD}}. \tag{32}$$

λ_p characterizes the response to a low-to-high output transition and λ_n characterizes the response to a high-to-low output transition. For a symmetric gate $\lambda_p = \lambda_n$, the CMOS inverter is simply characterized by one parameter λ. It can be seen that $\lambda = 1$ is the matched condition defined by (27). If λ is greater than one, wider transistors are used as compared to the matched widths and the output response is overdriven with overshoots and undershoots. If λ is less than one, smaller transistor widths are used as compared to the matched widths and the output response is underdriven or a sluggish response occurs. AS/X simulations are shown in Fig. 14 for several values of λ, depicting the underdriven, matched, and overdriven cases. The widths of the transistors are varied and λ is calculated according to (17). Note that λ accurately characterizes the output response as described above.

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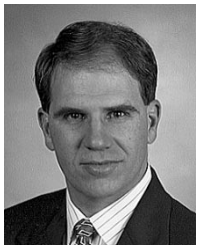

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