# EMI Suppression With Distributed *LLC* Resonant Converter for High-Voltage VR-on-Package

Kan Xu, Boris Vaisband, Gregory Sizikov, Xin Li, and Eby G. Friedman, *Fellow, IEEE*

***Abstract*— Higher on-chip current demand leads to lower power efficiency of the power delivery network due to distribution losses within the current path. A high-voltage power architecture and voltage regulator (VR)-on-package topology can increase system power efficiency by reducing distribution losses. Electromagnetic interference (EMI) can, however, be a significant challenge due to the high-voltage injection and close proximity to sensitive electronics. A novel transformer-based inductor, inductor, capacitor (*LLC*) resonant converter with a distributed topology for point-of-load dc-to-dc conversion is presented here. The distributed topology exhibits more than 3× lower EMI as compared with a single-branch *LLC* resonant converter with the same step-down ratio. A prototype of the VR-on-package has been developed. Experimental results demonstrate good correlation with the EMI analysis. Application to systems-in-package, wireless devices, and Internet of Things is targeted due to the low EMI of this distributed converter system.**

***Index Terms*— Electromagnetic interference (EMI), high-voltage power architecture, inductor, inductor, capacitor (*LLC*) resonant converter, system-in-package (SiP), voltage regulator (VR)-on-package.**

## I. Introduction

A CENTRALIZED power architecture (CPA) is widely used in computer systems, where two-stage voltage conversion is typically required [1]. A high dc voltage (ranging from 48 to 60 V), generated from an ac-to-dc converter, is initially converted to a medium-level dc voltage (for instance, 12 V) [2]. A point-of-load (PoL) converter subsequently transfers the medium-level voltage to an on-chip voltage (for instance, 0.8 V). Due to increasing current demand in high-performance computing (HPC) systems, a CPA suffers from significant distribution losses. A distributed power architecture (DPA) has therefore become a widely used power distribution topology [3], [4]. In DPA systems, the high dc voltage is directly converted into the load voltage using a PoL converter to eliminate local distribution losses caused by transmitting low voltages. With on-chip voltages as low as 0.8 V [5], high step-down ratio converters for DPA systems are required [3]. Although a DPA system can reduce distribution losses between the ac-to-dc converter and the PoL converter, the power loss due to the parasitic resistance between the PoL converter and the on-chip load can be substantial, particularly in HPC systems. This loss is referred to as the *last inch power loss* [6].

A voltage regulator (VR)-on-package is a promising technology to mitigate this last inch power loss. A VR module is traditionally board mounted, supporting voltage conversion and regulation for the on-chip load through the power distribution network of the printed circuit board (PCB) and the package. By placing a PoL converter within the package [6], the resistive path is shorter and only within the package. Power losses due to the resistive path are, therefore, lower as compared with a VR-on-PCB topology. Moreover, a VR-on-package topology requires less ball grid array (BGA) resources for the power distribution network due to high-voltage transmission between the PCB to package interface, supporting a higher on-chip signal bandwidth.

The close distance between the VR and on-chip load due to the VR-on-package topology and high-voltage injection due to the high-voltage DPA system lead to significant electromagnetic interference (EMI) [7]–[9]. Moreover, the higher operating frequency of the VR makes EMI more of a challenge [10]–[12]. Not only may EMI affect the proper function of the digital circuits but EMI can also pollute the surrounding EM environment, which is crucial for wireless devices and Internet of Things (IoT). EMI is particularly difficult to eliminate because EMI is often coupled through the package, where traditional shielding techniques cannot be applied. Suppression at the source of EMI is, therefore, important.

EMI is affected by the waveform profile and magnitude of the current flowing through the converter. The harmonic behavior associated with the high-frequency current and voltage waveforms is a major aspect of EMI. A sinusoidal current waveform exhibits few harmonics (ideally, only the primary harmonic), significantly mitigating EMI [13], [14]. A resonant converter is, therefore, advantageous due to the characteristics of high efficiency, high power density, and sinusoidal-shaped waveforms [15], [16]. Based on this concept, a novel high step-down ratio, low EMI inductor, inductor, capacitor (*LLC*) resonant converter with a distributed topology is proposed here.

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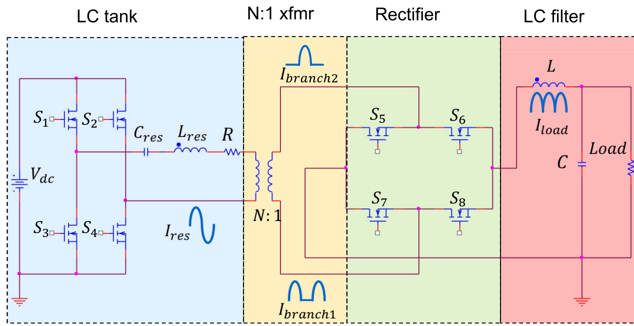


Fig. 1. Full-bridge isolated $LLC$ resonant converter.

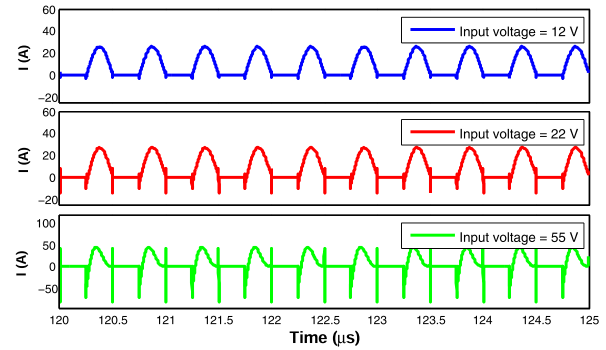


Fig. 2. Performance degradation of a high-turns-ratio converter.

The rest of this article is organized as follows. The performance degradation of an $LLC$ resonant converter caused by a high turns ratio is discussed in Section II. In Section III, a distributed $LLC$ resonant converter is introduced. The performance and power efficiency of this converter are also presented. In Section IV, near-field simulations of the EMI of the proposed distributed resonant converter are described. Experimental near-field scans of a VR-on-package prototype are also discussed. Some conclusions are offered in Section V.

## II. Performance Degradation Due to High Turns Ratio

As illustrated in Fig. 1, an $LLC$ resonant converter consists of four parts: 1) a primary stage $LC$ tank; 2) a transformer; 3) a rectifier in the secondary stage; and 4) an $LC$ filter. The primary stage $LC$ tank generates sinusoidal current from the input dc voltage of the $LLC$ resonant converter $V_{\mathrm{dc}}$. In this work, $V_{\mathrm{dc}}$ is assumed to be 55 V, a typical voltage within the telecommunications ecosystem. Voltage conversion and isolation are achieved by a step-down transformer. The step-down ratio determines the turns ratio of the transformer. A full-wave rectifier in the secondary stage of the converter transforms the ac current from the transformer into a dc current flowing into the load. Switches within the resonant converter utilize power MOSFETs, as illustrated in Fig. 1. An $LC$ filter removes any high-frequency harmonics originating from the imperfect sinusoidal current as well as stabilizes the output voltage.

The operating frequency of a resonant converter can range from a few hundreds of kilohertz up to a few megahertz. To limit the area of the magnetic component, a higher frequency is preferred, leading to a larger power density. The tradeoff, however, is greater switching loss. In the VR-on-package topology in this work, a smaller area is preferred. The target frequency of the $LLC$ resonant converter is, therefore, 2 MHz. The higher switching power loss is alleviated by the reduced distribution loss due to the VR-on-package topology.

The step-down transformer transfers the sinusoidal current from the primary stage ($I_{\mathrm{res}}$) to the branches of the secondary stage ($I_{\mathrm{branch1/2}}$). The magnitude of $I_{\mathrm{branch1/2}}$ is determined from both the load and turns ratio of the transformer. Two current paths control the switches, $S_5$, $S_6$, $S_7$, and $S_8$, in the rectifier stage, as illustrated in Fig. 1. When switches, $S_6$ and $S_7$, turn on, the first half-cycle of the sinusoidal current enters branch 1, flows through the load, and returns to the transformer in branch 2. When switches, $S_5$ and $S_8$, turn on, the second half-cycle of the sinusoidal current enters branch 2, flows through the load, and returns to the transformer in branch 2. Switching pairs, $S_6$ and $S_7$ and $S_5$ and $S_8$, intermittently turn on and off two current paths at the resonant frequency of the primary $LC$ tank stage. The load current ($I_{\mathrm{load}}$) is, therefore, a positive half-cycle sinusoidal current at twice the resonant frequency, as illustrated in Fig. 1. Due to the output capacitor $C_{\mathrm{out}}$, the voltage across the load exhibits less ripple, proportional to the current flowing through the load.

A transformer with a high turns ratio is required for high step-down ratio conversion in DPA systems (e.g., from 55 to 0.8 V). Parasitic impedances exist between the secondary stage of the resonant converter and the on-chip load. For example, the power delivery network within the package connecting the VR to the on-chip power delivery network can contribute hundreds of micro-ohms of parasitic resistance. The effects of the parasitic impedance within the secondary stage, however, become significant with a higher turns ratio, producing a distorted current waveform within the converter. As compared with a sinusoidal current waveform, a distorted current waveform produces greater EMI. Two case studies with large input voltages and a high step-down ratio have been evaluated. 22 and 55 V are the input voltages in these two case studies. The output voltage in both cases is 0.8 V. The turns ratio of each transformer is selected to match the step-down ratio of the converters. Simulation results of the two case studies are illustrated in Fig. 2. Performance degradation due to the high turns ratio is demonstrated as compared with the low turns ratio in the 12 V to 18 V conversion.

The current flowing through branch 1 $I_{\mathrm{branch1}}$ in each of the converters is illustrated in Fig. 2. Current spikes are observed in both cases when the current waveform within the branch crosses zero. The magnitude of the current spikes increases with a higher turns ratio of the transformer, as illustrated in Fig. 2. In the case of the 55-V input, the current waveform is significantly distorted, no longer maintaining a sinusoidal shape. Large current spikes of 90 A produce greater EMI, resulting in a less robust, noisy system. Moreover, a high voltage across the circuit elements is induced by these current spikes, potentially causing device failure.

The effect of the turns ratio of a transformer on the behavior of a converter is illustrated in Fig. 3. An ideal transformer is

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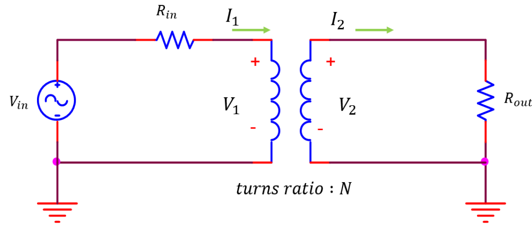


Fig. 3. Working principle of basic transformer.

assumed, where

$$\frac{V_1}{V_2} = \frac{I_2}{I_1} \tag{1}$$

is maintained. The voltage across the primary winding is

$$V_1 = \frac{N^2 R_{\text{out}}}{N^2 R_{\text{out}} + R_{\text{in}}} V_{\text{in}}. \tag{2}$$

The current through the primary winding is

$$I_1 = \frac{V_{\text{in}}}{N^2 R_{\text{out}} + R_{\text{in}}}. \tag{3}$$

The output resistance and parasitic impedance of the rectifier stage degrade the operation of the primary $LC$ tank. The resistance in the secondary stage contributes to the total parasitic resistance within the $LC$ tank in the sinusoidal current generation stage. From (2) and (3), the parasitic impedance seen by the primary stage is $N^2$ times larger than the actual resistance. The output impedance, therefore, has a greater effect on the $LC$ tank than the parasitic impedance of the primary stage. With increasing $N$, the effect of the parasitic impedance on the secondary stage grows exponentially, leading to a distorted current waveform within the $LC$ tank. An $LLC$ resonant converter with a high turns ratio is, therefore, a challenging requirement. Nonetheless, a high step-down ratio is required for DPA PoL converters due to the high input and low on-chip output voltage levels. A converter with a small turns ratio transformer and high step-down ratio is, therefore, highly desirable.

## III. *LLC* Resonant Converter With Distributed Topology

To provide high step-down ratio conversion, a scalable distributed topology for the $LLC$ resonant converter is proposed. As illustrated in Fig. 4, a distributed topology is achieved by cascading multiple primary stages in parallel with multiple secondary stages. A lower voltage drop is exhibited in this configuration across the primary winding of each branch. The secondary stage of each branch is connected to the load without contention from the other branches. The output of the secondary stage of each branch is connected to the power/ground pins of the resonant converter. Current flows from the power pins to the power delivery network within the package. The secondary stage voltage of the distributed topology is similar to the voltage of a single branch $LLC$ resonant converter. The primary stage voltage in the distributed topology is, however, reduced due to the voltage divider across all of the serially connected primary stages. Increasing the

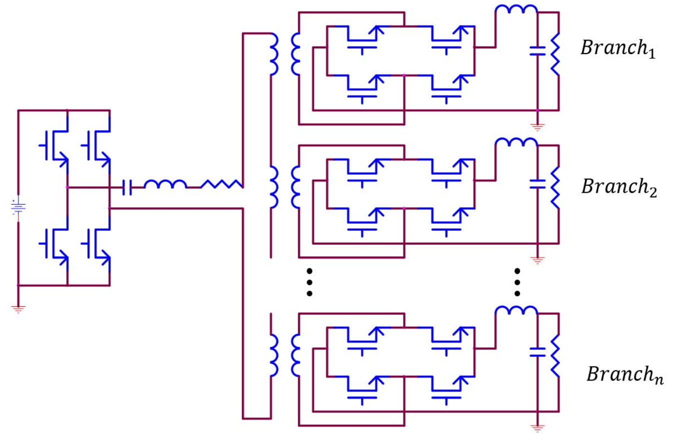


Fig. 4. *LLC* resonant converter with distributed topology.

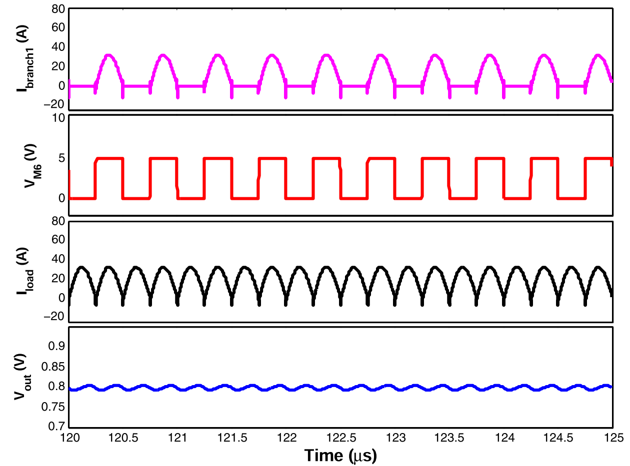


Fig. 5. Waveforms characterizing performance of distributed $LLC$ resonant converter.

number of branches within the distributed topology further reduces the turns ratio of the transformer within the $LLC$ resonant converter. High step-down ratio conversion is, therefore, achieved using multiple transformers with a low turns ratio.

The topology of the distributed $LLC$ resonant converter is evaluated for high step-down ratio PoL conversion. The distributed topology consists of eight branches. Each branch exhibits a turns ratio of 8.5. An input voltage of 55 V is converted to an output voltage of 0.8 V. The passive $LC$ elements, parasitic impedances, switches, and load behavior are identical for each branch. Simulation results describing the performance of the distributed $LLC$ resonant converter are illustrated in Fig. 5. The output voltage is stable around 0.8 V with less than 3% ripple. Improved sinusoidal distortion and smaller current spikes are achieved as compared to a single-branch, high-turns-ratio converter. A reduction of 90% in the magnitude of the current spikes is achieved by the distributed topology. Reductions in EMI levels are discussed in Section IV.

Power loss breakdown models of converters have been well researched [17]–[20]. Four components are considered to quantify the loss breakdown process: 1) primary side power MOSFETs; 2) transformer; 3) secondary side power

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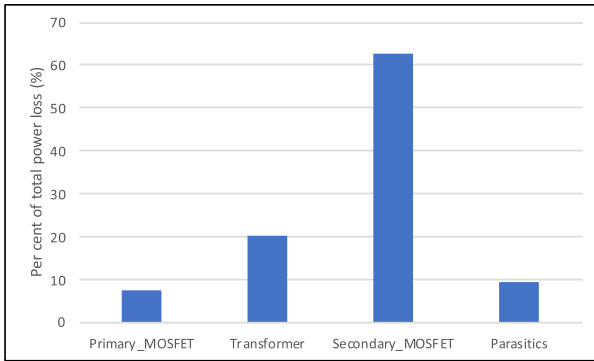


Fig. 6. Power loss components for an eight-branch distributed $LLC$ resonant converter.

MOSFETs; and 4) parasitic impedances. Note that a low output resistance reduces the loss within the MOSFET. PSPICE is used to evaluate both the switching and static power loss. The transformer loss, typically composed of core and winding losses, is a significant component of the total power loss of a converter [20]. The transformer loss varies significantly with different design specifications such as the core size, winding size, and winding material. One objective of this article is to evaluate the effects of EMI on the proposed resonant converter. Since the design of the transformer is out of the scope of this article, a 97% transformer efficiency is assumed for the power loss breakdown analysis.

A distribution of the power loss of each component in the eight branch distributed $LLC$ resonant converter is illustrated in Fig. 6. The transformers and MOSFETs within each of the branches are included. The secondary-side MOSFETs contribute most of the total power loss due to the high currents flowing through the secondary stage and the large number of MOSFETs to support the eight branches. The maximum power efficiency of the distributed $LLC$ resonant converter is 89.8%, as compared to a 91.7% maximum power efficiency in a single-branch $LLC$ resonant converter with the same step-down ratio. The distributed converter, therefore, exhibits a greater total power loss as compared with the single-branch resonant converter. Due to the low turns ratio, the energy loss of each branch in the distributed topology is less than the energy loss of the single-branch resonant converter. The degradation in power efficiency in the distributed topology is small. The slightly reduced power efficiency is compensated by the high step-down ratio conversion in DPA systems, leading to comparable or greater system-level power efficiency. Due to the lower turns ratio, the current waveform is also less distorted, producing lower EMI.

Because of the additional transformers and switches in the secondary stage, the area of the distributed $LLC$ resonant converter increases linearly with the number of branches. The increase in area is dependent on the type of transformer and switch. Due to the lower current flowing through each branch within the distributed resonant converter, a smaller switch is utilized. A smaller transformer is also used due to the lower turns ratio. The area of each branch within the distributed $LLC$ resonant converter is, therefore, less than the single-branch resonant converter. In one case study, the area of an eight-branch distributed $LLC$ resonant converter is 84.1% larger than a single-branch $LLC$ resonant converter.

Note that the distributed converter topology is highly scalable. The number of branches is dependent on the circuit area, specific voltages, and performance requirements. This distributed topology is particularly advantageous when high step-down ratio conversion is required, as in DPA systems. Due to the EMI mitigation characteristics, as described in Section IV, the distributed topology is highly applicable to noisy environments, such as systems-in-package, IoT, and wireless applications.

## IV. Near-Field EMI Evaluation in VR-on-Package Environment

Although a high step-down ratio PoL converter-in-package is a promising technology, high EMI levels have become significant, degrading the system-level signals and compromising power integrity. Due to the close proximity in a VR-on-package environment between the source and victims of EMI, and the high voltages in a high step-down ratio converter-in-package, EMI within a package has become a significant issue. Full-wave EM simulations are, therefore, described in this section to evaluate the EMI characteristics of the proposed distributed $LLC$ resonant converter. EMI fundamentals are briefly summarized in Section IV-A. The VR-on-package environment used to evaluate the EMI characteristics of the proposed distributed $LLC$ resonant converter is described in Section IV-B, followed by the simulation setup. Experimental and simulation results are discussed in Section IV-C.

### A. EMI Background

EMI is the phenomenon where an EM disturbance is generated by surrounding electronic devices that affect the proper function of the electrical circuits through a conducted or radiated path. Conducted EMI, also called coupling noise, consists of inductive and capacitive coupling through an electrical path. Conducted EMI filters are widely used to reduce the conducted EMI [21], [22]. Since the primary focus in this article is to evaluate how the resonant converter affects the EM environment within a system-on-package (SoP), conducted EMI, albeit important, is not the focus of this article. Radiated EMI is the undesired EM radiation generated by high-frequency electronic devices without an electrical path. Due to the high operating frequency of the proposed distributed $LLC$ resonant converter, radiated EMI is the primary noise issue in this converter.

The effects of EMI can be evaluated as two parts, the aggressor and the victim. Any electrical device or passive element can behave as an antenna, radiating an EM wave to the surrounding environment. This structure is considered to be an EMI aggressor. The higher the frequency and the larger the antenna size, the stronger the EM radiation. Due to the high frequency, high power characteristics, and large metal traces transferring high voltages, the PoL converter-in-package is considered here as an EMI aggressor. The entire system, including the digital ICs and PoL converters, is treated as an EMI victim. The surrounding environment

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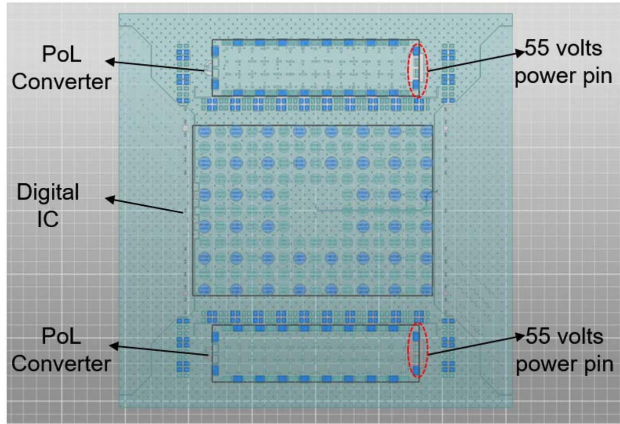
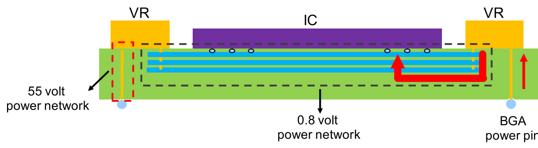



(a)




(b)

Fig. 7. Package with a digital IC and two PoL converters. (a) Top view. (b) Side view.

outside the package is not considered; the near-field range is the focus of this article.

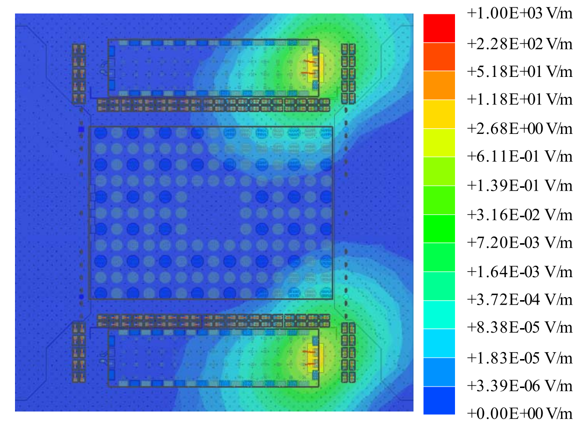
### B. EMI Evaluation Setup

The evaluation of package-level EMI has recently drawn significant attention from the research community [7]–[9], [11], [23], [24]. In [9], a thin micro-electromechanical system (MEMS) package is used to evaluate different EMI suppression methods. By redesigning the microbumps, adding ground vias, and applying a metal coating on the input–output ports, lower EMI is achieved. In [7], a near-field EMI evaluation methodology has been developed for mobile DRAM applications. In [8], cavity resonance, as an EMI contributor, has been evaluated with a full-wave solver. The effects on EMI within individual elements and possible EMI vulnerable spots within a package are also discussed. To the authors' best knowledge, no work has been published on evaluating EMI in a VR-on-package environment where the PoL converters are treated as EMI aggressors.

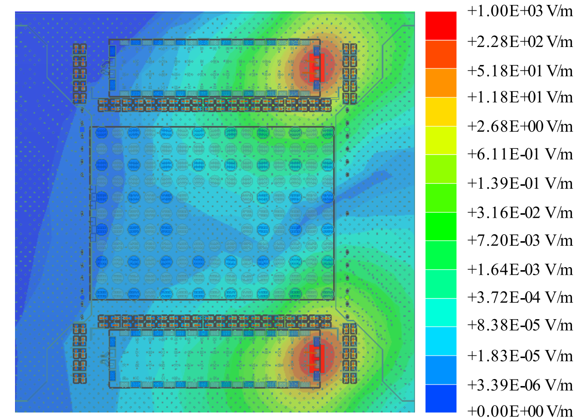
The package utilized to evaluate EMI has been designed within a VR-on-package environment based on the design specification listed in Table I. All of the power planes and via connections for the power distribution network exist within the package. No signal routing, however, exists within the package. As illustrated in Fig. 7(a), three components, a digital IC and two PoL converters, are placed on the top side of the package, highlighted by the solid rectangles. The area of the IC and PoL converter components is, respectively, 900 and 250 mm$^2$. Since the intended application of the VR-on-package is HPC, the rectangle representing the digital IC can include a silicon interposer and high bandwidth memory. Alternatively, the rectangle representing a PoL converter represents the proposed resonant converter, including

TABLE I
DESIGN SPECIFICATIONS OF PACKAGES SUPPORTING VR-ON-PACKAGE ENVIRONMENT

| *Package parameter* | *Value* |
|---|---|
| Total metal layers | 28 |
| Package core layers | 14 |
| Package thickness (um) | 2,025 |
| Package size (mm) | 62 x 62 |
| Decoupling capacitance (uF) | 2,892 |
| 12 volt power plane footprint (mm$^2$) | 4 |
| Number of BGA pins | 2,780 |




(a)




(b)

Fig. 8. Intensity of electric field across package. (a) Distributed *LLC* resonant converter. (b) Single-branch *LLC* resonant converter.

the switching devices, transformer, and power/ground pinout. Note that planar magnetics technology is utilized by the power transformer within the converter, reducing the thickness of the converter in the VR-on-package system. The winding is based on etched copper traces on a PCB with the planar magnetic core passing through the PCB. The active and passive components are assembled on the surface of the PCB. The entire converter is assembled on the package next to the digital IC, as illustrated in Fig. 7(a). The circular pads shown in the figure are connection pins between the package and digital

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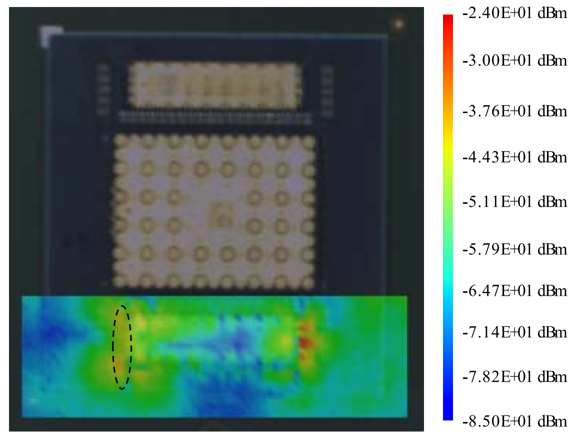
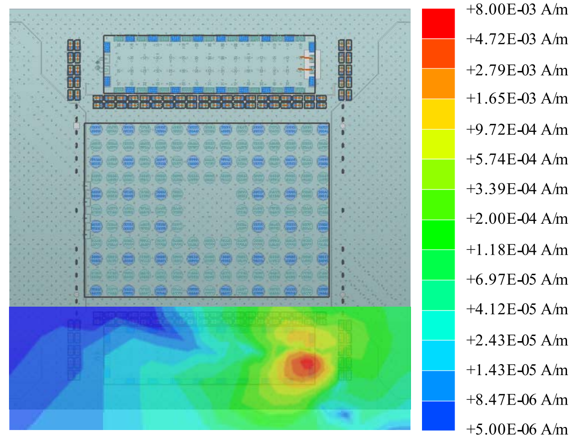
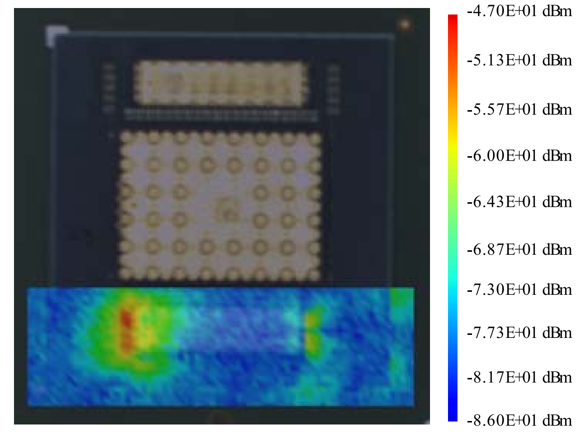



(a)

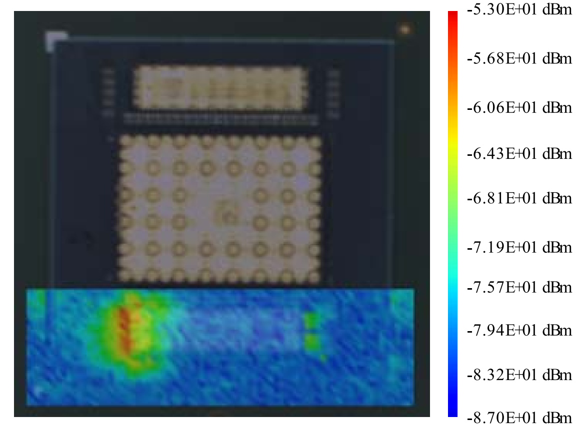



(b)

Fig. 9. Validation of near-field EMI of distributed topology of $LLC$ resonant converter. (a) Experimental near-field scan. (b) EMI simulation of the $Y$-component of the magnetic field at 120 MHz.




(a)




(b)

Fig. 10. Near-field EMI scan of the $Y$-component of the magnetic field. (a) 500 MHz. (b) 800 MHz.

IC and the PoL converters. The dashed circles illustrate the location of the via stack, which transfers 55 V from the PCB to the PoL converter.

A side view of the system is depicted in Fig. 7(b). Two voltage domains exist within the power network of the package. One domain is a high-voltage power network (55 V), as illustrated by the dash box. The high-voltage power network connects the BGA power pins and the VRs, where low current is transferred from the BGA power pins to the VRs, as the thin arrow indicates. The other power domain is a low-voltage power network (0.8 V), as illustrated by the double dash box. The low-voltage power network connects the VRs and IC, where high current is transferred from the VRs to the on-chip power network through the 0.8-V power network, as the thick arrow indicates. Note that the decoupling capacitance listed in Table I is connected to the 0.8-V power network. Dedicated power planes transfer current from the PoL converters to the digital IC after 55 V are converted into 0.8 V.

As previously mentioned, radiated EMI behaves as an antenna. A large metal trace passing a high-frequency, high-voltage signal is a strong EMI aggressor. In the following case study, the via stack, which transfers 55 V to the PoL converter, is treated as an EMI aggressor. Note that EMI from the via stack passing through the package is difficult to eliminate since it is difficult to shield the system. The metal trace within the PoL converter is not considered an EMI aggressor since the voltage on the metal trace within the PoL converter is only 0.8 V after the conversion process. A metal coating can also be used to reduce EMI radiation around the PoL converter [9]. The EMI intensity is also related to the characteristics of the signal passing through the EMI aggressor (the EMI source) [25]. To compare the EMI levels of the proposed distributed $LLC$ resonant converter with the single branch $LLC$ resonant converter, the current and voltage characteristics are extracted from Cadence Virtuoso simulations, as described in Section III. A near-field EMI simulation (using ANSYS SIwave [26]) is subsequently conducted for the entire package. The far-field radiation of the PoL converter is also provided, comparing the EMI level with the International Special Committee on Radio Interference (CISPR) 22 standard, which is widely used for radiated and conducted EMI.

### *C. EMI Validation of Distributed LLC Resonant Converter*

As previously mentioned, simulation of the near-field EMI is conducted in ANSYS SIwave, where the near field is

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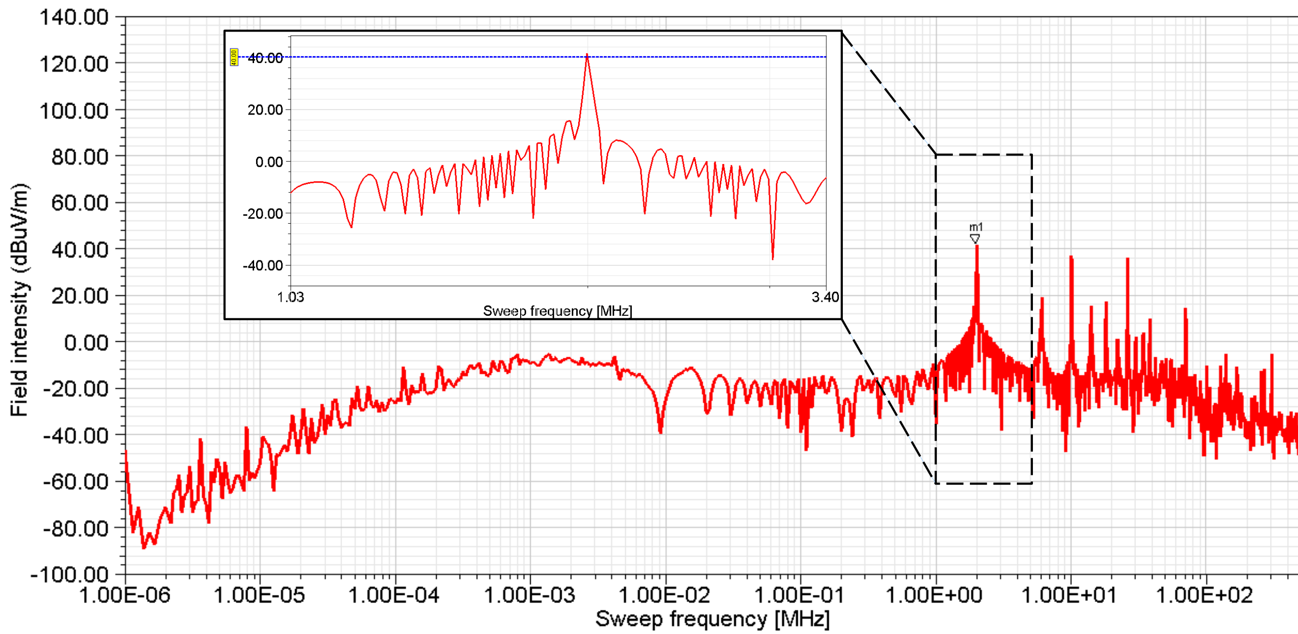


Fig. 11. Comparison between far-field radiation of distributed $LLC$ resonant converter at 3 m and the CISPR 22 standard.

TABLE II
COMPARISON OF SINGLE-BRANCH AND DISTRIBUTED $LLC$ RESONANT CONVERTERS

| | (i) $V_{in}$ | (ii) $V_{out}$ | $\frac{(ii)}{(i)}$ Step down ratio | Turns ratio | Branch # | Ripple | Power efficiency |
|---|---|---|---|---|---|---|---|
| Single branch | 12 V | 0.8 V | 15 | 15 | 1 | 4% | 91.7% |
| Distributed topology | 55 V | 0.8 V | 68.75 | 8.5 | 8 | 3% | 89.8% |

evaluated on the surface of a cuboid that completely encloses the system. The offset of the $x$-, $y$-, and $z$-axes of the cuboid is 4 mm. The observation surface illustrated in Fig. 8 is the top surface of the cuboid.

The EMI levels across the entire package, characterized as electronic field intensity, are illustrated in Fig. 8. A layout of the metal layer and components of the package are also illustrated in Fig. 8, where the near-field distribution within the package is depicted. A darker color implies a higher EMI level. The closer to the EMI aggressor, the higher the EMI. The highest electric field intensity is observed around the via stack, where the high voltage is injected into the VR-on-package system. The highest EMI level from the single-branch and distributed $LLC$ resonant converters is, respectively, 740 and 210 V/m, as illustrated in Fig. 8. The distributed $LLC$ resonant converter, therefore, exhibits more than 3× lower EMI than the single-branch $LLC$ resonant converter.

A prototype of the VR-on-package topology has also been developed. Near-field scans have been conducted, spanning from 120 MHz to 14 GHz. The near field is scanned using the API 3-D scanning system with a printed circuit magnetic field probe [27]. An experimental magnetic field scan above the bottom side of the PoL VR at 120 MHz is illustrated in Fig. 9(a). These experimental results agree with the EMI simulations in ANSYS SIwave, depicting the magnitude and location of the peak EMI in the VR-on-package system.

TABLE III
EMI CHARACTERISTICS OF DISTRIBUTED $LLC$ RESONANT CONVERTER WITH DIFFERENT NUMBER OF BRANCHES

| Branch number | 1 | 2 | 4 | 8 |
|---|---|---|---|---|
| EMI level | 740 V/m | 560 V/m | 384 V/m | 210 V/m |

The $Y$-component of the peak magnetic field is $6.85 \times 10^{-3}$ A/m, as illustrated in Fig. 9(b). The highest radiated power in the experimental near-field scan is −24 dBm, as illustrated in Fig. 9(a). As previously mentioned, the evaluation surface is 4 mm above the package, leading to a magnetic field strength of $7.25 \times 10^{-3}$ A/m. The simulation of the peak EMI matches the experimental near-field scan within a 5.5% error. The experimental field distribution pattern illustrated in Fig. 9(a) is different from the EMI simulation in Fig. 9(b) since no signal routing is included in the simulation. The location of the high-speed signal is illustrated by the dashed circle in Fig. 9(a). The experimental results also demonstrate that EMI from the high-speed signal begins to dominate with increasing frequency, as illustrated in Fig. 10.

The far-field radiation of the proposed distributed $LLC$ resonant converter at a distance of 3 m is illustrated in Fig. 11. The frequency ranges from 0 to 500 MHz. A zoomed-in view around the resolution frequency of 2 MHz is also illustrated in Fig. 11 to provide sufficient resolution. The highest field

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intensity at 3 m, 42 dBuV/m, is observed at 2 MHz due to the resonant frequency of the converter. CISPR 22 for class B 3-m radiated EMI limit (40 dBuV/m) is also illustrated in Fig. 11 as the dashed line. The far-field EMI is below 40 dBuV/m across the entire spectrum except for the resonant frequency at 2 MHz. Note that the far-field EMI is not the focus of this article. Shielding techniques can reduce far-field EMI [9]. Near-field EMI is, however, difficult to eliminate due to the compact nature of a system-in-package.

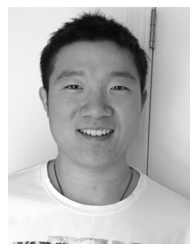
A comparison of the near-field EMI among distributed resonant converters with different branch numbers is listed in Table III. Although the power efficiency of the distributed $LLC$ resonant converter is lower than the single-branch $LLC$ resonant converter, the distributed $LLC$ resonant converter utilizes a much higher step-down ratio. Importantly, the distributed $LLC$ resonant converter exhibits significantly lower EMI as compared with the single-branch $LLC$ resonant converter (see Table II). The high step-down ratio and low EMI characteristics of the proposed distributed $LLC$ resonant converter make the distributed $LLC$ resonant converter a promising candidate for PoL conversion in a VR-on-package environment.

## V. Conclusion

An $LLC$ resonant converter operating at high frequencies to provide PoL dc–dc conversion is described in this article. Distortion of the sinusoidal waveform produces a 90-A current spike due to the high turns ratio of the transformer. A distributed $LLC$ resonant converter that supports high step-down conversion is, therefore, proposed. A stable voltage with less than 3% ripple is achieved. A reduction of nearly 90% in the magnitude of the current spikes as compared to a single-branch $LLC$ resonant converter with a similar step-down ratio is also achieved. A VR-on-package platform, supporting EMI evaluation of the VR, is demonstrated. More than 3× lower EMI in the distributed $LLC$ resonant converter is achieved as compared with the single-branch $LLC$ resonant converter utilizing the same step-down ratio. Experimental results show good correlation with the EMI simulations in terms of the magnitude and location of the peak EMI. The distributed converter topology is also highly scalable and compatible with standard power conversion architectures.

## References

[1] K. I. Hwu, W. Z. Jiang, and Y. T. Yau, "Ultrahigh step-down converter," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3262–3274, Jun. 2015.
[2] I. P. Vaisband, R. Jakushokas, M. Popovich, A. V. Mezhiba, S. Kose, and E. G. Friedman, *On-Chip Power Delivery and Management*. Cham, Switzerland: Springer, 2016.
[3] L. Brush, "Distributed power architecture demand characteristics," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, vol. 1, Feb. 2004, pp. 342–345.
[4] H. Huang, "Coordination of design issues in the intermediate bus architecture," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, vol. 1, Mar. 2005, pp. 169–175.
[5] K. Xu, R. Patel, P. Raghavan, and E. G. Friedman, "Exploratory design of on-chip power delivery for 14, 10, and 7 nm and beyond FinFET ICs," *Integration*, vol. 61, pp. 11–19, Mar. 2018.
[6] K. Xu, B. Vaisband, G. Sizikov, X. Li, and E. G. Friedman, "Power noise and near-field EMI of high-current system-in-package with VR top and bottom placements," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 9, no. 4, pp. 712–718, Apr. 2019.
[7] J. S. Youn *et al.*, "Chip and package-level wideband EMI analysis for mobile dram devices," in *Proc. DesignCon*, Jan. 2016, pp. 1–14.
[8] N. Kim, L. H. Li, S. Karikalan, R. Sharifi, and H. Kim, "Package-level electromagnetic interference analysis," in *Proc. IEEE Electron. Compon. Technol. Conf.*, May 2014, pp. 2119–2123.
[9] C.-H. Ko, H.-L. Lee, and C.-H. Wang, "The EMI suppression of ultra thin MEMS microphone package," in *Proc. IEEE Int. Microsyst. Packag. Assembly Circuits Technol. Conf.*, Oct. 2010, pp. 1–3.
[10] D. J. Perreault *et al.*, "Opportunities and challenges in very high frequency power conversion," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2009, pp. 1–14.
[11] D. Shin, N. Kim, J. Lee, Y. Park, and J. Kim, "Quantified design guides for the reduction of radiated emissions in package-level power distribution networks," *IEEE Trans. Electromagn. Compat.*, vol. 59, no. 2, pp. 468–480, Apr. 2017.
[12] S. Kose, E. G. Friedman, R. M. Secareanu, and O. Hartin, "Current profile of a microcontroller to determine electromagnetic emissions," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2013, pp. 2650–2653.
[13] Y.-S. Lee and G.-T. Cheng, "Quasi-resonant zero-current-switching bidirectional converter for battery equalization applications," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1213–1224, Sep. 2006.
[14] R. L. Steigerwald, "A comparison of half-bridge resonant converter topologies," in *Proc. IEEE Appl. Power Electron.*, Mar. 1987, pp. 135–144.
[15] P. Clarke, "Self-commutated thyristor DC-to-DC converter," *IEEE Trans. Magn.*, vol. MAG-6, no. 1, pp. 10–15, Mar. 1970.
[16] K. Xu, B. Vaisband, G. Sizikov, X. Li, and E. G. Friedman, "Distributed sinusoidal resonant converter with high step-down ratio," in *Proc. IEEE Elect. Perform. Electron. Packag. Syst.*, Oct. 2017, pp. 1–3.
[17] F. Krismer and J. Kolar, "Accurate power loss model derivation of a high-current dual active bridge converter for an automotive application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 881–891, Mar. 2010.
[18] K. Venkatachalam, C. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters," in *Proc. IEEE Comput. Power Electron.*, Jun. 2002, pp. 36–41.
[19] R. Yu, G. K. Y. Ho, B. M. H. Pong, B. W.-K. Ling, and J. Lam, "Computer-aided design and optimization of high-efficiency LLC series resonant converter," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3243–3256, Jul. 2012.
[20] F. Xue, R. Yu, and A. Q. Huang, "A 98.3% efficient GaN isolated bidirectional DC–DC converter for DC microgrid energy storage system applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9094–9103, Nov. 2017.
[21] X. Huang, J. Feng, F. C. Lee, Q. Li, and Y. Yang, "Conducted EMI analysis and filter design for MHz active clamp flyback front-end converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2016, pp. 1534–1540.
[22] H.-I. Hsieh, J.-S. Li, and D. Chen, "Effects of X capacitors on EMI filter effectiveness," *IEEE Trans. Ind. Electron.*, vol. 55, no. 2, pp. 949–955, Feb. 2008.
[23] Y. Xiong and Z. Yan, "EMI and PI analysis of analog board," in *Proc. IEEE Int. Symp. Microw., Antenna, Propag. EMC Technol. Wireless Commun.*, Oct. 2013, pp. 171–175.
[24] S. Hayashi and M. Yamada, "EMI-noise analysis under ASIC design environment," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 19, no. 11, pp. 1337–1346, Nov. 2000.
[25] T. Sudo, H. Sasaki, N. Masuda, and J. Drewniak, "Electromagnetic interference (EMI) of system-on-package (SOP)," *IEEE Trans. Adv. Packag.*, vol. 27, no. 2, pp. 304–314, May 2004.
[26] (2017). *ANSYS SIwave*. [Online]. Available: http://www.ansys.com/products/electronics/ansys-siwave
[27] (2019). *API*. [Online]. Available: http://www.amberpi.com/productssmartscan550



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