Grid-Based Redistribution Layers Within 3-D Power Networks

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***Abstract*— Although CMOS scaling has slowed, the demand for greater performance and heterogeneous integration has only increased. Three-dimensional integrated circuits (ICs), which exploit the vertical dimension, extend scaling while providing a platform for heterogeneous integration and greater performance. The redistribution layer (RDL) is a critical component in the power delivery system within heterogeneous 3-D systems, where each layer is individually designed, optimized, and fabricated. A circuit model of the power/ground (P/G) RDL is described considering different through-silicon-via (TSV) fabrication methods and stacking topologies. A grid-based RDL is proposed to support higher current and fewer P/G TSVs. By utilizing a grid-based RDL, five times more current is supported without a significant voltage drop as compared with a direct point-to-point (P2P) RDL. The grid-based RDL also supports a nonuniform TSV distribution, alleviating area constraints. In one case study, a grid-based RDL with 20 unevenly distributed TSVs exhibits a 9.8% lower voltage drop than a P2P RDL with 50 uniformly distributed TSVs.**

***Index Terms*— 3-D integrated circuits (ICs), power delivery network, redistribution layer (RDL), through-silicon vias (TSVs).**

I. Introduction

IMPROVEMENTS in microprocessors have slowed and become more costly due to the increasing challenges in scaling CMOS technology [1]. By exploiting the vertical direction, 3-D integrated circuits (ICs) provide a promising solution to extend scaling [2]. Vertical integration in 3-D ICs achieves a smaller die as well as significantly shorter global interconnects, leading to higher system performance and lower power dissipation. Multiple forms of 3-D ICs exist, including monolithic, contactless, and through-silicon-via (TSV) topologies. The TSV is the key technology in TSV-based 3-D ICs, where signal communication and power distribution between layers are achieved with, respectively, signal TSVs and power/ground (P/G) TSVs. The 3-D ICs are also a natural platform for heterogeneous integration, where individual layers can be designed, optimized, and fabricated with different semiconductor technologies [3].

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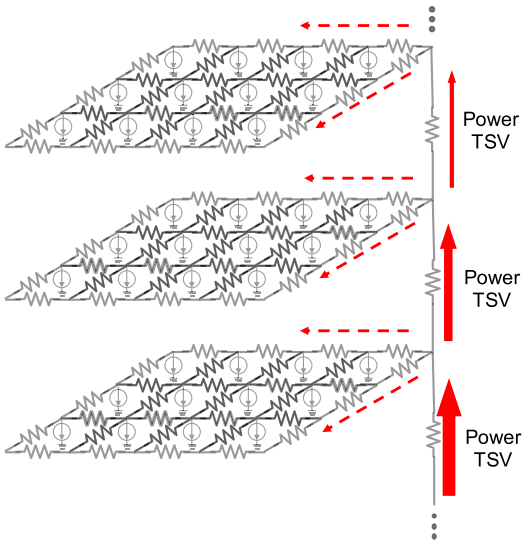

Fig. 1. Current path within a 3-D power distribution network consisting of vertical current paths through the P/G TSVs and horizontal current paths within each 2-D IC.

Despite the successful commercial development of 3-D products such as 3-D DRAM memory, high-bandwidth memory, and field programmable gate arrays (FPGAs) [4]–[7], 3-D ICs suffer from power integrity issues within the 3-D power delivery system [8]–[11]. Due to the introduction of P/G TSVs, the current paths within a complex 3-D system can be highly sophisticated, affecting both the reliability and performance of the 3-D power delivery system. A model of a 3-D power delivery system consists of a conventional 2-D power grid and P/G TSVs, which are serially connected to adjacent 2-D power grids [12], [13]. Two current paths, therefore, exist within a 3-D power delivery system, as shown in Fig. 1. As highlighted by the dashed arrow in Fig. 1, the horizontal current path designates the power network transferring current from a nearby P/G TSV within a 2-D power grid. The magnitude and current path of this current are set by the on-chip current demand of each 2-D layer. Alternatively, the vertical current path transfers current from the bottom P/G TSVs to the upper P/G TSVs, as highlighted by the thick arrow shown in Fig. 1. This vertical current path is achieved by the serially connected P/G TSVs between layers. The magnitude of the vertical current within certain P/G TSV is set by the total current demand of all of the layers receiving current through the TSVs.

The development of a power delivery network within a 3-D IC is highly challenging due to these vertical current paths.

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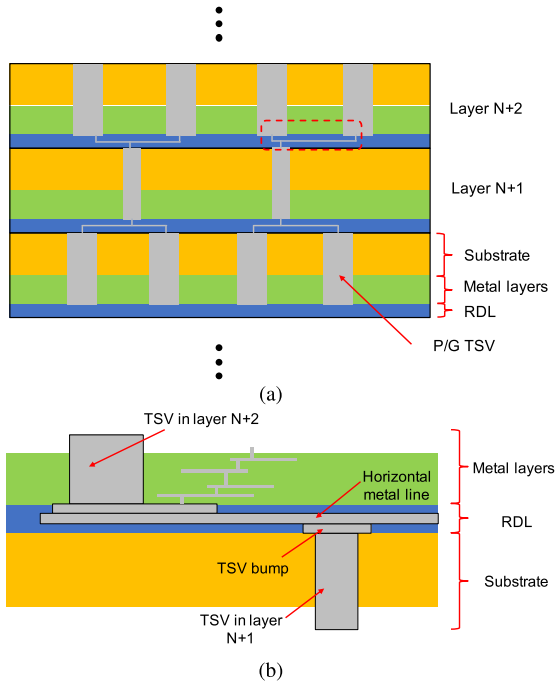

Fig. 2. RDL as an interface between a P/G TSV and an adjacent P/G TSV and between a P/G TSV and a 2-D power grid. (a) Location of the RDL within a 3-D IC between two adjacent layers. (b) Zoomed-in view of the RDL, where the RDL supports both horizontal and vertical current paths.

One of the key factors affecting the current path is the P/G TSVs [10], [14]–[24]. Another key factor is the redistribution layer (RDL) within the 3-D power delivery network. This topic has to date received minimal attention from the research community [25]–[27]. An RDL within a 3-D power delivery system is shown in Fig. 2, where a face-to-back stacked topology is depicted. As shown in Fig. 2(a), the RDL is between the substrate of layer N and the metal layer of layer $N+1$. As shown in Fig. 2(b), the RDL behaves as the interface between the P/G TSVs and adjacent P/G TSVs and between the P/G TSVs and the 2-D power grid, which supports, respectively, the horizontal path and vertical path. The RDL is therefore a critical component in the 3-D power delivery system. An RDL plays an even more impactful role within heterogeneous 3-D systems, where each layer is individually designed, optimized, and fabricated. An evaluation of RDLs with different 3-D manufacturing processes as well as the effects of an RDL on the power delivery system is described in this article. In addition, a grid-based RDL and related design guidelines to tackle power integrity challenges in heterogeneous 3-D systems are provided.

The rest of this article is organized as follows. Prior work related to RDLs in 3-D ICs is discussed in Section II. Technical background characterizing an RDL is also introduced. The effects of different 3-D integration topologies on an RDL are discussed in Section III. In Section IV, the effects of a grid-based RDL on the power integrity of a 3-D system are discussed. Multiple scenarios are introduced to demonstrate the advantages of a grid-based RDL in heterogeneous 3-D systems. Some conclusions are offered in Section V.

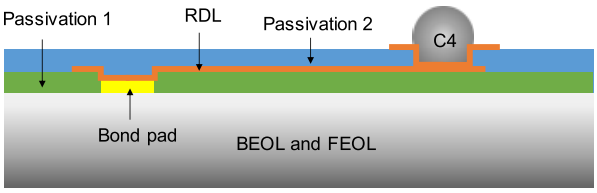

Fig. 3. RDL as an interface between the IC and package.

A discussion of the effects of the TSV manufacturing process on an RDL is provided in Appendixes A and B.

II. Background and Previous Work

In conventional 2-D ICs, the RDL is effectively within the top metal layer, above the back-end-of-line (BEOL) and beneath the controlled collapse chip connection (C4) bumps, as shown in Fig. 3. Note that the RDL is a separate fabrication process, which occurs after the BEOL and prior to the bonding process [28]. The bond pads and C4 bumps are connected by the RDL, and the C4 bumps are connected to the bond pads on the package. The RDL is the interface between the IC and package. Within an industrial design flow, the IC and package are typically designed separately [29], [30]. Any mismatches between the package pinout and on-chip pinout can therefore be corrected by the RDL as a routing layer between the package and IC [28].

As an intermediate step toward 3-D integration, 2.5-D systems have become a viable solution to increase the on-chip bandwidth [31]. In a 2.5-D system, the RDL is the metal lines within the silicon interposer between the IC and package [32]. The vertical connections between the package and ICs are achieved with fine pitch TSVs. The ICs are interconnected through the RDL within the interposer for interchip communication. The RDL is the interface between multiple ICs within a 2.5-D system.

RDLs in 3-D integrated systems have not attracted significant attention in the literature. Discussions of P/G RDLs utilize oversimplified assumptions, such as a perfect TSV-to-TSV match between adjacent layers or simple metal stripe connections between the TSVs and the 2-D power grid [25]–[27], [33]. A 3-D RDL is defined in this work as: 1) the metal lines connecting the TSVs within layer N to the TSVs within layer $N+1$ and 2) the metal lines connecting the TSVs within layer N to the on-chip interconnect within layer N. An RDL is briefly mentioned in a 3-D integrated environment [34]–[36], where the RDL is between the bottom layer and the package, which is effectively a 2-D RDL. In [27] and [37], a novel layer bonding technique is proposed for via-first 3-D integration, where a damascene patterned metal/adhesive RDL is achieved within the bonding layer. In [26], two methods for fabricating an RDL in TSV-based 3-D ICs are introduced. A comparison between these two methods as well as fabrication guidelines are also provided. In [25], the signal integrity of 3-D interconnect is discussed with different TSV fabrication techniques. A physical model of a TSV-RDL-bump interconnect is provided, followed by characterization of the impedances. In [33], the RDL between the C4 and microbumps

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is investigated in a two-layer 3-D system. An IR drop analysis of different RDL schemes and TSV fabrication technologies is also included. Interactions between the interlayer currents due to the RDL are, however, not considered in [25] and [33].

Note that the focus of this article is on RDLs for power delivery systems rather than for signal routing. Optimization and modeling of 3-D power networks have been investigated, but these works [17]–[23], [38]–[40] do not consider power/ground (P/G) RDL networks. The RDL in 3-D power networks is, therefore, the focus of this article. Intralayer and interlayer current transfer within an RDL for 3-D power delivery is discussed here for the first time.

III. RDL With Different 3-D Stacking Topologies

As discussed in Section II, the P/G RDL in a 3-D IC is the interface between the P/G TSVs and adjacent 3-D layers and between the TSVs and the 2-D power grid within the same 3-D layer. The 3-D stacking topologies, therefore, significantly affect the RDL. The effects of different 3-D stacking topologies on the circuit model of the P/G RDL are discussed in this section. The TSVs also play an important role in the RDL. A frontside via-last TSV is assumed in the following discussion due to the characteristics of low resistance and high current capacity. The effects of the TSV fabrication process on the P/G RDL are described in Appendixes A and B.

A back-to-face topology is widely used in 3-D ICs due to the ability to scale multilayer stacks [2], [21]. Other topologies exist in 3-D ICs, including face-to-back, face-to-face, and back-to-back [2]. These stacking topologies can also affect the current paths and P/G RDL in 3-D ICs. Since both the face-to-face and back-to-back topologies can only be applied to a two-layer 3-D IC, these topologies are not considered here. The face-to-back topology, alternatively, is a popular topology utilized in many 3-D ICs [4]–[7].

Consider an example of a frontside via-last TSV. A comparison of the P/G RDL between the back-to-face and face-to-back topology is shown in Fig. 4. Two types of 3-D RDLs, including the connection between the TSVs and 2-D power grid and between the TSVs and adjacent TSVs, are named, respectively, a type one RDL and type two RDL. Both type one and two RDLs are required in these two topologies, where the connection to the RDLs is somewhat different. A type two RDL in both topologies connects the TSV of layer N to the TSV of layer $N+1$. A type one RDL, alternatively, connects the TSV of layer N to the power grid of layer N and layer $N+1$ in, respectively, the back-to-face and face-to-back topologies, as listed in Table I. The current flowing to the loads in layer N is therefore transferred from the P/G TSV within layer N in the back-to-face topology. In contrast, the same current is transferred from the P/G TSV within layer $N-1$ in the face-to-back topology. Note that this difference in current paths leads to different design methodologies and optimization processes for these two types of topologies, a topic which has to date been ignored. For example, the design characteristics of a P/G TSV within layer N, such as the physical size, number, and distribution style, should be chosen based on the power

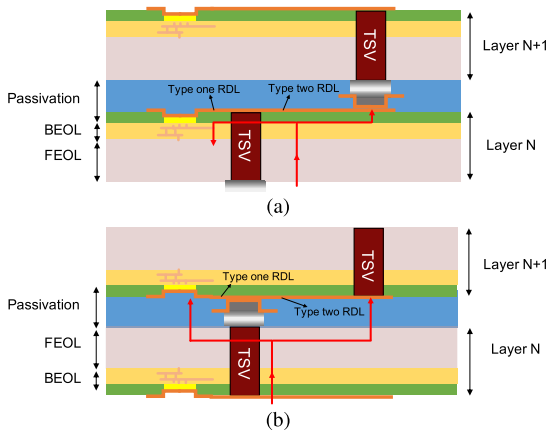

Fig. 4. Cross-sectional view of current path and P/G RDL. (a) Back-to-face stacking topology. (b) Face-to-back stacking topology.

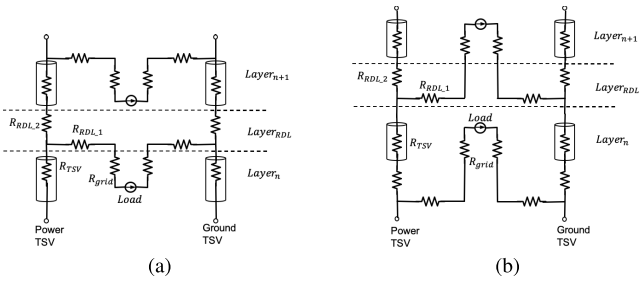

Fig. 5. Circuit model of current path and P/G RDL. (a) Back-to-face stacking topology. (b) Face-to-back stacking topology.

consumption and load distribution in layer $N+1$ in a face-to-back topology.

A circuit model of the current path and P/G RDL within different 3-D stacking topologies is based on the single layer circuit model. A type two RDL, R_{RDL2}, as the interface between layer$_n$ and layer$_{n+1}$, is shown in Fig. 5(a). The dashed lines represent the border between layers, specifically, layer$_n$, layer$_{n+1}$, and layer$_{\mathrm{RDL}}$. Note that a flip-chip technology is assumed in the circuit model, where the current passes from the bottom layer to the top layer. To evaluate the effects of the 3-D stacking topology on the power noise, a seven layer 3-D power network is considered. In both topologies, the bottom layer is connected to a 0.8-V power supply. Circuit parameters, R_{RDL1}, R_{RDL2}, R_{TSV}, R_{grid}, and Load, are the same for the two topologies. The load current is modeled as a dc current source.

The voltage drop in layer three for the two topologies is shown in Fig. 6. The solid and dashed lines represent, respectively, the voltage drop in the back-to-face and face-to-back topologies. Increasing the load current in an adjacent layer, layer three, from 10 to 500 mA, while maintaining a constant load current from the other layers increases the voltage drop, as shown in Fig. 6(a). Note that a higher voltage drop is observed in the back-to-face topology since an additional layer of P/G TSVs is required for the back-to-face topology, as listed in Table I. The back-to-face topology is more sensitive to load variations in the adjacent layer as a greater change in the voltage drop is observed as compared with the face-to-back topology. The effect of the resistance on

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TABLE I
COMPARISON OF FACE-TO-BACK AND BACK-TO-FACE 3-D STACKING TOPOLOGIES

	Back-to-face	Face-to-back
Supported TSV processes	Via-first, via-middle, and via-last	Via-first, via-middle, and via-last
RDL one connection	TSV (layer n) to grid (layer n)	TSV (layer n) to grid (layer n+1)
RDL two connection	TSV (layer n) to TSV (layer n+1)	TSV (layer n) to TSV (layer n+1)
Total layer of TSV in an M layer 3-D IC	M	M-1

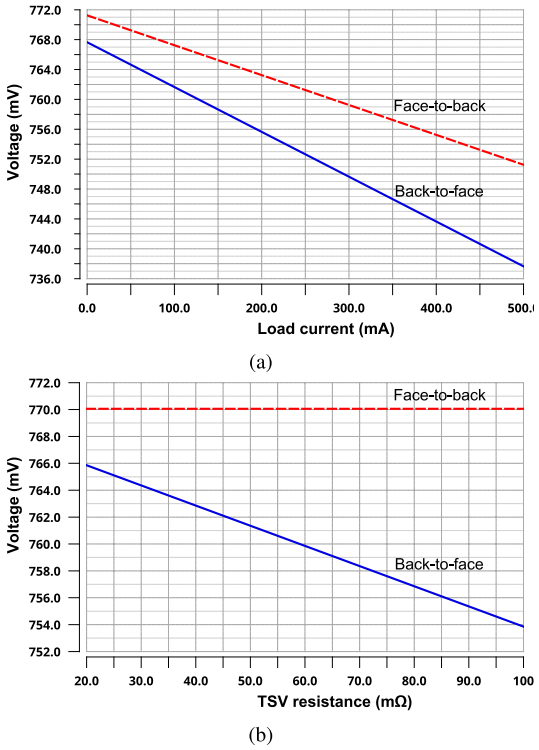

Fig. 6. Comparison of the voltage drop at the current source of layer three within a seven layer 3-D power network with a back-to-face and face-to-back topology. (a) Load increases in the adjacent layer. (b) P/G TSV resistance increases within layer three.

the P/G TSV on the voltage drop of layer three is shown in Fig. 6(b). A 35% increase in voltage drop is observed in the back-to-face topology due to R_{TSV} in layer three. In contrast, the voltage drop does not change in the face-to-back topology. This constant voltage drop is due to the fundamental difference between current paths within these two 3-D stacking topologies. Consider an example of layer$_n$. The current flows to Load$_n$, passing through R_{TSV} in layer n within the back-to-face topology. Alternatively, the current flows to Load$_n$, passing through R_{TSV} in layer $n-1$ rather than R_{TSV} in layer n within the face-to-back topology. In the face-to-back topology, the P/G TSV within a specific layer does not directly affect the voltage drop in this layer, but rather affects the voltage drop in the higher layer. The back-to-face topology, therefore, supports a self-contained design process for each layer.

Both TSV fabrication methods and the 3-D stacking topology significantly affect the current paths and P/G RDL in a 3-D IC. To compare the proposed grid-based RDL with existing RDL structures, frontside via-last TSVs and a back-to-face topology are assumed. Due to the higher conductivity of the fill material and relatively mature fabrication process, the via-last TSV method is preferred for the P/G TSVs in 3-D systems. Within the via-last TSV method, the frontside via-last TSV is assumed here since the type one RDL is not used in the backside via-last TSV method. A more general RDL analysis, including both type one and two RDLs, is appropriate for heterogeneous 3-D systems. A discussion of the interactions between RDLs and TSV manufacturing processes is provided in Appendixes A and B. Although an additional layer of TSVs is required in the back-to-face topology as compared with the face-to-back topology, the back-to-face topology is preferred due to the advantages of separate TSV processes for the different layers.

Existing work has demonstrated fabricated 3-D systems without discussing the function and effect of the P/G RDL [4]–[7]. Oversimplified assumptions regarding the RDL have, however, been made. For example, a perfect match of the P/G TSV distribution between adjacent layers is assumed [4]–[7], where the P/G TSV bumps in layer N perfectly overlap with the TSV bumps in layer $N+1$. The aforementioned type two RDL is, therefore, neglected. In addition, a type one P/G RDL is also neglected by either assuming a via-first or via-middle TSV type or by simplifying the connection as a point-to-point (P2P) metal line [10]. These assumptions are either unrealistic or do not support high-performance heterogeneous 3-D systems.

IV. GRID-BASED RDL IN 3-D ICS

The current path and P/G RDL of a 3-D power network with different TSV fabrication methods and 3-D stacking topologies are reviewed in Section III. The 1-D lumped circuit models are described to demonstrate the effects of the P/G RDL on different 3-D systems. Although a lumped model is sufficient to provide insight into the P/G RDL, the distributed nature of the power network is not considered.

A 2-D distributed circuit model of a 3-D power network is, therefore, preferred to characterize a P/G RDL [41]. A resistive grid-based 3-D power network as a platform to evaluate different P/G RDL topologies is described in Section IV-A. A grid-based RDL is also introduced in this section. A comparison between the proposed RDL and existing RDLs is provided in Section IV-B. The advantages of a grid-based RDL in different scenarios, such as a nonuniform P/G TSV distribution and high-current demand, are also discussed in this section.

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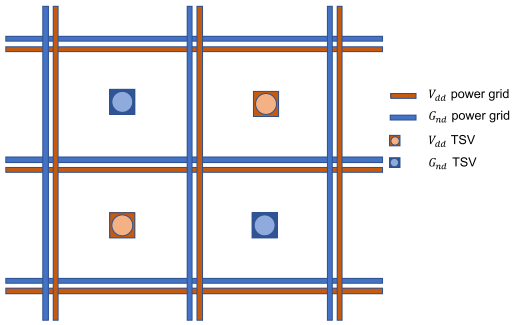

Fig. 7. Power grid with a two-layer mesh structure.

TABLE II
2-D POWER GRID SPECIFICATIONS [1]

Characteristic	Value
2-D IC size (μm)	1,000 x 1,000
P/G pitch (μm)	2
P/G pair pitch (μm)	50
Metal line width (μm)	1
Metal line depth (μm)	2.5
Metal layer number	2
Cu conductivity (S/m)	5.88 x 10^7
Average power consumption (W)	2
V_{dd} (V)	0.8

TABLE III
P/G TSV SPECIFICATIONS [33]

Characteristic	Value
TSV length (μm)	50
TSV diameter (μm)	10
P/G TSV pitch (μm)	50
P/P TSV pitch (μm)	70.7
TSV type	Frontside via-last
3-D layer number	3
Cu conductivity (S/m)	5.88 x 10^7

TABLE IV
P/G RDL SPECIFICATIONS [33]

Characteristic	Value
RDL line width (μm)	6
RDL line thickness (μm)	3.5
RDL line pitch (μm)	50
RDL layer number	2
Cu conductivity (S/m)	5.88 x 10^7

A. Grid-Based P/G RDL Model

The power network of a 3-D IC is divided into three parts: the 2-D power grid of each layer, the P/G TSVs connecting adjacent layers, and the P/G RDL. A comprehensive model of a 2-D power grid consists of the global power grid, via stacks, and local power rails [1]. As the focus of this article is the interaction among layers due to the RDL, the 2-D power distribution network is treated as a simple two-layer mesh structure, as shown in Fig. 7. Adjacent power and ground metal lines are grouped to form a P/G pair, reducing the power grid inductance and saving on-chip area for the P/G TSVs. In a classic 2-D distributed model, each node is connected to a dc load within the distributed model to eliminate the effects of temporal load variations on the RDL analysis process [42]. DC loads are also assumed to be identical to eliminate the effects of variations on the RDL analysis process due to the location of the load. Specifications of the 2-D power grid are summarized in Table II. The parameters of the circuit model are based on these specifications. Note that the on-chip decoupling capacitance and metal line inductance are not considered in this model since the focus here is on the dc behavior.

A comprehensive TSV model considering coupling capacitance and inductance is discussed in [43] and [44]. In this article, the P/G TSV model is a simple resistor since the focus here is not the P/G TSVs but rather the P/G RDL. Note that within the TSV model, the barrier and seed layer are neglected as the current carried by these layers is negligible. A uniform distribution of the P/G TSVs is assumed across the entire 3-D system. The power and ground TSVs are distributed in an interdigitated manner, as shown in Fig. 7. The specification of the P/G TSVs is listed in Table III. The number of layers in the 3-D power network is assumed to be three. The model is, however, scalable to a higher number of layers.

A direct P2P RDL is described in [10] and [33], where a metal stripe directly connects the P/G TSV to an adjacent power line within a 2-D grid, as shown in Fig. 8(a). Note that only the $V_{\rm dd}$ side of the power network is illustrated in this model as $V_{\rm dd}$ and $G_{\rm nd}$ within the power network in a 3-D IC are assumed to be symmetric [2]. The ground TSVs and ground RDL are within the blank area, as shown in Fig. 8(a). As discussed in Section III, current flows from the P/G TSVs to the loads within each layer through the P/G RDL and 2-D power grid. Several 2-D power grid topologies have been proposed to manage the high-current demand and to reduce power noise [45]. The same high current also passes through the P/G RDL. The direct P2P RDL, only relying on the metal stripe, leads to high power noise and electromigration, particularly when the number of P/G TSVs is insufficient or the distribution of the P/G TSVs is uneven.

A grid-based P/G RDL is therefore proposed. As shown in Fig. 8(b), a two-layer P/G RDL, each layer oriented orthogonally, forms a mesh structure similar to a 2-D power grid. The RDL layers are placed above the metal layers of the power grid, connecting the P/G TSVs to the power grid. Vertical vias are formed where the RDL crosses the power grid. The grid-based P/G RDL can be modeled as an independent system. The inputs to the system are the connections between the P/G TSV and the RDL metal layer, where the number and location of the inputs are dependent on the number and distribution of the P/G TSVs within the 3-D layer. The circuit

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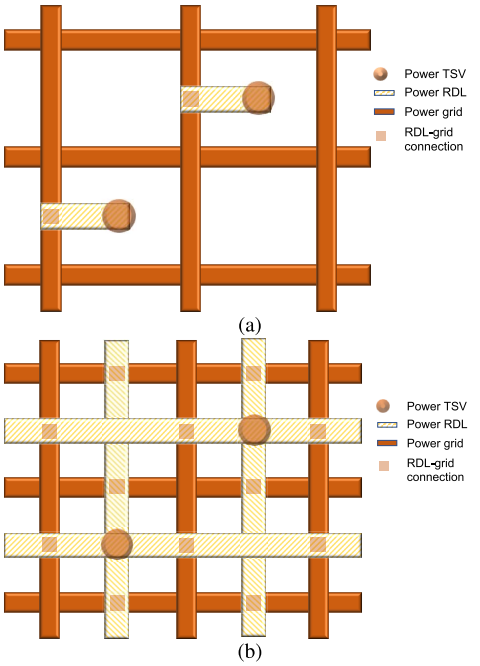

Fig. 8. Model of the P/G RDL connecting the P/G TSVs to the 2-D power grid. (a) Direct P2P RDL. (b) Grid-based RDL.

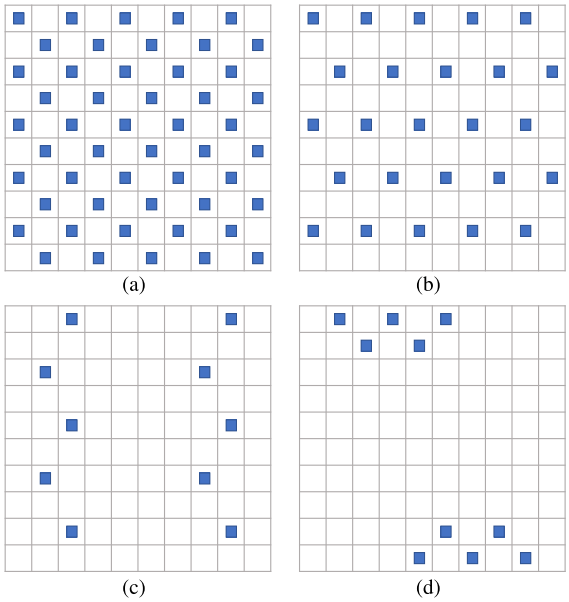

Fig. 9. Distribution topologies of P/G TSV to compare voltage drop between P2P RDL and grid-based RDL. (a) 100 TSVs with uniform distribution. (b) 50 TSVs with uniform distribution. (c) 20 TSVs with uniform distribution. (d) 20 TSVs with uneven distribution.

model of the RDL system, similar to the 2-D power grid, is a standard 2-D resistive grid. The specification of the P/G RDL grid is listed in Table IV. The outputs of the system are the connections between the 2-D power grid and the RDL metal layer. Note that the number and location of the outputs are fixed, which are set by the specifications of the 2-D power grid.

B. Comparison Between Grid-Based RDL and P2P RDL

A comprehensive circuit model of a 3-D power network is described here, combining the previously described models of the 2-D power grid, P/G TSV, and P/G RDL. A three-layer 3-D power network is assumed. The number and magnitude of the resistor within the model of the 2-D power grid are listed in Table II. As discussed in Section III, frontside via-last TSVs and a back-to-face stacking topology are assumed as well as a 10×10 uniform TSV distribution. Each load connected to the 2-D power grid is also connected to a nearby P/G TSV within the range of the pitch of a P/G pair. The resistance of the TSV is listed in Table III. A grid-based structure is initially only applied to the type one RDL to evaluate the effects of an RDL on a single 2-D power grid. The type two RDL is, therefore, neglected. The model generation and simulation are conducted in Cadence Spectre. A comparison of the voltage drop on layer two between the P2P RDL and a grid-based RDL is provided.

A type one RDL is the interface between the P/G TSVs and the 2-D power grid. The distribution topology and number of TSVs can, therefore, affect the performance of the P2P and grid-based RDL. To evaluate the effects of the number of TSVs on the RDL performance, three simulation scenarios are considered, where the TSV distribution topology is assumed uniform and the number of TSVs are 20, 50, and 100. The location of the power TSVs within the different scenarios is shown in Fig. 9. Note that only the power TSVs are illustrated. Only half of the total number of TSVs are, therefore, shown in Fig. 9. To evaluate the TSV distribution topology, another scenario is considered, where the TSV distribution is assumed to be uneven and the number of TSVs is 20. Two groups of TSVs are assigned, respectively, to the top-left and bottom-right corner, as shown in Fig. 9(d).

The voltage drop at each input of the current load in the second layer of the 3-D power network is shown in Fig. 10. Each tile within the figure represents a current load. The shade of the tile illustrates the voltage level of the connected current load, where the darker shade represents a lower voltage level and the lighter shade represents a higher voltage level. A comparison between the grid-based and P2P RDL with 100 P/G TSVs is shown, respectively, in Fig. 10(a) and (b). The voltage drop with the grid-based P/G RDL is quite low, exhibiting a maximum voltage drop of 11.3 mV, compared with the P2P RDL with a maximum voltage drop of 47.1 mV. The larger voltage drop on the right of Fig. 10(b) is due to the connection of the TSV to the adjacent metal line on the left of the P2P RDL, as shown in Fig. 8. The voltage drop increases significantly with fewer P/G TSVs, from 50 to 20, as shown in Fig. 10(c)–(f). In Fig. 10(d) and (f), the loads without a direct connection to the P2P RDL exhibit a much higher voltage drop than the grid-based RDL with a maximum voltage drop of, respectively, 93.1 and 163 mV. Alternatively, the voltage drop of the loads connected to the grid-based RDL is within 5% of the noise margin even with 20 TSVs, as shown in Fig. 10(e). This trend is due to the nature of the grid structure, producing a lower resistance as compared with a simple metal stripe in the P2P RDL. For the same number

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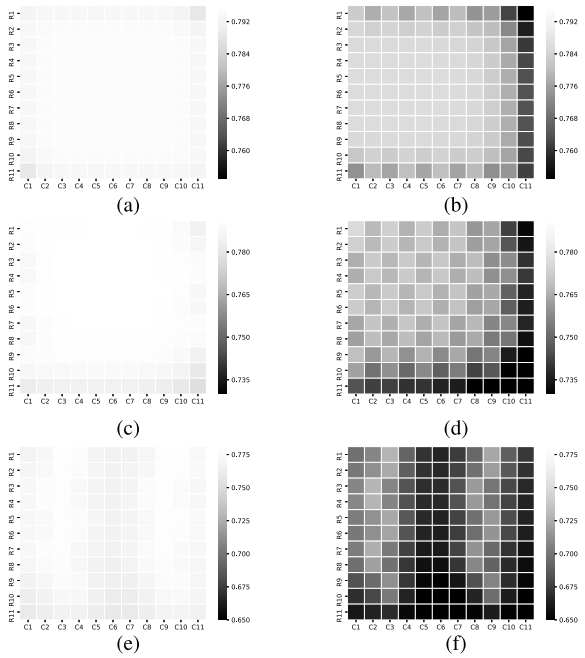

Fig. 10. Variation in voltage drop in 3-D power networks with fewer P/G TSVs for grid-based and P2P P/G RDL. (a) 100 TSVs with grid-based P/G RDL. (b) 100 TSVs with P2P RDL. (c) 50 TSVs with grid-based RDL. (d) 50 TSVs with P2P P/G RDL. (e) 20 TSVs with grid-based P/G RDL. (f) 20 TSVs with P2P P/G RDL.

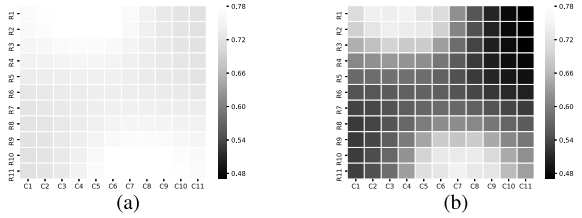

Fig. 11. Comparison of voltage drop between the grid-based and P2P RDL with uneven P/G TSV distribution. (a) 20 unevenly distributed P/G TSVs with grid-based RDL. (b) 20 unevenly distributed P/G TSVs with P2P RDL.

of P/G TSVs and distribution topology, the grid-based RDL produces a much lower voltage drop within the 3-D power network.

In the previous analysis, a uniform distribution of P/G TSVs is assumed. Although a uniform distribution is preferable to suppress the worst case voltage drop in 3-D power networks [9], a uniform distribution may not be a practical design choice due to area constraints. A 3-D power network with an uneven TSV distribution is therefore considered here to evaluate the relative performance of the P2P and grid-based RDL. In this case study, P/G TSVs are distributed at the top-left and bottom-right corner of the IC, as shown in Fig. 9(d). The total number of TSVs is 20. The simulation results are shown in Fig. 11. A significant increase in voltage drop is observed at the location without P/G TSVs in both the P2P and grid-based RDLs. The highest voltage drop of the P2P and grid-based RDL is, respectively, 331.1 and 84 mV. The mesh structure of the grid-based RDL balances any voltage variations across the IC caused by the uneven TSV distribution. A standard

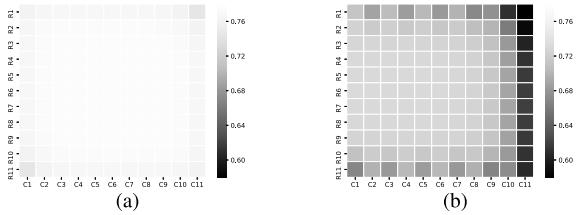

Fig. 12. Comparison of the voltage drop between (a) grid-based RDL and (b) P2P RDL with increasing load current.

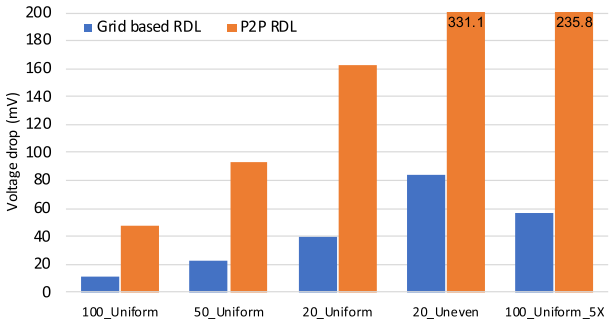

Fig. 13. Comparison of the highest voltage drop in the grid-based RDL and P2P RDL for five different scenarios.

deviation of 0.021 is observed in Fig. 11(a) as compared with a standard deviation of 0.078 in Fig. 11(b).

To evaluate the P/G RDL in a high current environment, a high current 3-D power network is also considered. The average power consumption of each layer is increased from 2 to 10 W; 100 P/G TSVs and a uniform distribution are assumed. The simulation results are shown in Fig. 12. The voltage drops significantly in this scenario as compared with the 2-W scenario [see Fig. 10(a) and (b)]. The P2P RDL cannot support high current 3-D power networks despite the large number of available P/G TSVs. The grid-based RDL is, therefore, also preferable for high current 3-D power networks.

The worst case voltage drop within a grid-based and P2P RDL is compared for the five aforementioned power network scenarios. For the P2P RDL, the worst case voltage drop is larger than the 5% noise margin in all scenarios, as shown in Fig. 13. The P2P RDL is not a feasible choice for 3-D power networks with few TSVs, unevenly distributed TSVs, or high power consumption. For the grid-based RDL, the worst case voltage drop is within the 5% noise margin of the uniform TSV distribution topology. An uneven distribution significantly affects the voltage drop, increasing the worst case voltage drop by 200%. The worst case voltage drop in the scenario of 20 unevenly distributed TSVs utilizing the grid-based RDL is 84 mV, which is lower than the scenario with 50 uniformly distributed TSVs utilizing the P2P RDL. The grid-based RDL can therefore reduce the required number of P/G TSVs in 3-D power networks while better tolerating any area constraints. In addition, the grid-based RDL supports much higher currents with less overhead. As compared with the P2P RDL, 5× greater current can be achieved within the grid-based RDL with a slightly higher worst case voltage drop, as shown in Fig. 13.

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V. Conclusion

Based on the functionality of the P/G RDL, two types of RDLs are introduced: type one RDL that connects P/G TSVs to the 2-D power grid and type two RDL that connects P/G TSVs within adjacent layers. The method of fabricating a TSV and the 3-D stacking topology can affect the impedance and performance characteristics of a P/G RDL. A circuit model of a P/G RDL is therefore described with different TSV and stacking strategies. A grid-based P/G RDL is proposed and compared with a P2P RDL. It is observed that a grid-based RDL significantly suppresses the voltage drop in 3-D power networks, supporting fewer P/G TSVs and higher current demand. A grid-based RDL can also support a nonuniform TSV distribution, alleviating possible area constraints. The grid-based RDL is therefore an effective candidate for high current, heterogeneous 3-D systems.

Appendix I
RDL Within Type A TSV Fabrication Process

Based on the TSV fabrication process, four different TSV types exist: via-first, via-middle, backside via-last, and frontside via-last. Depending on the connections of the P/G TSVs to the 2-D power grid, two types of TSVs are used within these four TSV types. Via-first, via-middle, and backside via-last TSVs are described as a type A TSV, where the P/G TSVs are connected to the 2-D power grid through the BEOL layers. A frontside via-last TSV is described as a type B TSV, where the P/G TSVs are connected to the 2-D power grid through an additional RDL.

In the via-first TSV method, TSVs are fabricated before the front-end-of-line (FEOL) process. Via-first TSVs are connected to the top metal layer by the following FEOL and BEOL processes. As shown in Fig. 14(a), the TSV does not pass through the metal layer, saving on-chip metal resources. To endure high temperatures during the FEOL process, polysilicon is typically utilized as the fill material for the via-first TSVs, leading to high-resistance TSV paths. Via-middle TSVs are fabricated after the FEOL process and prior to the BEOL process. Similar to the via-first method, the TSVs rely on the BEOL process to connect to the top metal layer. The choice of fill material for the via-middle method is, however, relaxed due to the lower temperature during the BEOL process. Tungsten is typically utilized, which exhibits a higher conductivity as compared with polysilicon.

Alternatively, in the via-last method, TSVs are fabricated after the BEOL process. A higher conductivity material, for example, copper, can be utilized as the fill material for the TSVs. Depending on whether the front or the back of the TSV etching process is used, two types of via-last methods exist: backside via-last and frontside via-last. In the backside via-last method [46], [47], the etching starts from the silicon substrate and ends at the bottom layer of the BEOL, for example, M1. The TSVs are therefore quite similar to the via-first and via-middle methods in terms of the connection between the TSV and the power grid, as shown in Fig. 14(a). These TSVs, for convenience, are described in this article as type A TSVs.

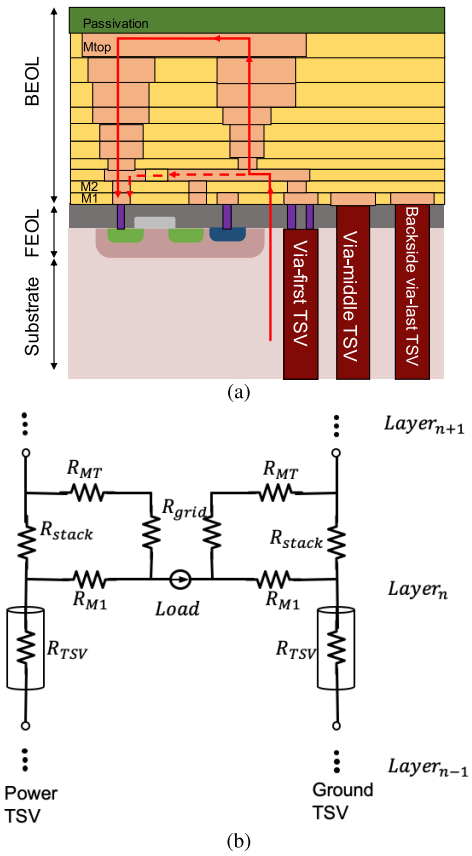

Fig. 14. Type A TSV and current path between the TSV and the load. (a) Cross-sectional view. (b) Lumped circuit model.

Although the fabrication process, physical size, and material of the TSVs vary significantly among type A TSVs, the current paths are quite similar, as shown in Fig. 14(a). Note the current path between the via-first TSV and the load. The power network is symmetric on the power and ground side. The ground side is, therefore, not shown in Fig. 14(a). As highlighted by the solid arrow, current from layer N–1 initially passes through the P/G TSVs in layer N. Due to the connection between the P/G TSV and the BEOL metal lines, current is transferred from the TSVs to the global power grid through a via stack [1]. The current is subsequently distributed to the local circuits through the power network within layer N. Alternative current paths may exist [39], as shown by the dashed arrow in Fig. 14(a). In these alternative paths, current is directly transferred from the P/G TSVs to the local power metal lines, for example, M2 or M3. The current is subsequently transferred to the local circuits, bypassing the via stacks and global power grid. This alternative current path is a physical design option, which does not apply to all 3-D systems [39]. In addition, these alternative current paths utilizing local power metal lines exhibit significant resistance due to interconnect scaling and the relatively large pitch of the P/G TSVs [48].

A lumped circuit model of a single layer of a 3-D power network with a type A TSV is discussed here. The current paths within a single layer are shown in Fig. 14(b), consistent with the other layers. The P/G TSVs, 2-D power grid, and load are included in the circuit model, as shown in Fig. 14(b).

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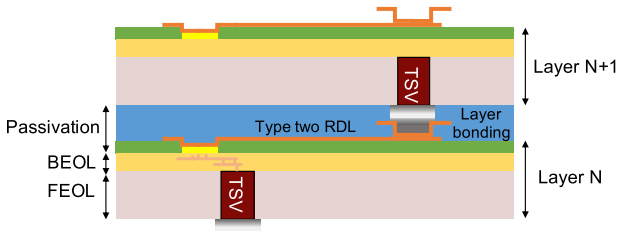

Fig. 15. Cross-sectional view of a type two RDL for type A TSVs. The type two RDL connects the bond pad of the power grid in layer N to the P/G TSVs in layer $N+1$.

R_{TSV}, R_{stack}, R_{MT}, R_{grid}, and R_{M1} represent, respectively, the resistance of the P/G TSV, via stacks between the TSV and the top metal layer, top metal line connecting the via stacks to the 2-D power grid, 2-D power grid, and alternative current paths within the lower metal layer. The voltage drop with a type A TSV on layer n within an m layer 3-D IC is

$$V_{\mathrm{drop}}^{n,m} = I_{\mathrm{laod}}[(m-n+1)R_{\mathrm{TSV}} + \frac{R_{M1}R_{\mathrm{stack}}(m-n+1) + R_{M1}(R_{\mathrm{MT}}+R_{\mathrm{grid}})}{R_{M1}+R_{\mathrm{MT}}+R_{\mathrm{grid}}+R_{\mathrm{stack}}}] \quad \text{(A.1)}$$

where the current demand of each layer is I_{load}. Based on (A.1), high current $I_{\mathrm{load}}(m-n+1)$ passes through the R_{stack} and R_{TSV} paths.

In type A TSVs, a dedicated type one RDL is not required as the via stacks within the BEOL connect the TSVs to the global power grid, as shown in Fig. 14. A type two RDL connects the 2-D power grid in layer N to the P/G TSVs in layer $N+1$, as shown in Fig. 15. Due to the individual manufacturing process of each 3-D layer, mismatches exist between the power grid in layer N and the P/G TSVs in layer $N+1$. A type two RDL is, therefore, required in general 3-D ICs. This issue has been missing in the literature, where a perfect match between the power grid pad and the TSV distribution is assumed [4]–[7].

Appendix II
RDL Within Type B TSV Fabrication Process

Alternatively, in the frontside via-last method [49], the etching starts from the top metal layer of the BEOL and the TSV passes through the entire layer, creating metal routing blockages, as shown in Fig. 16. Due to the unique fabrication process, these TSVs are named here as a type B TSV. Note that type B TSVs are fabricated after the BEOL and passivation processes are completed. In addition, type B TSVs pass through the entire layer, including both FEOL and BEOL. No metal line connections, therefore, exist between the TSVs and the global power grid, as shown in Fig. 16(a). Also note that the alternative current path in type A TSVs does not exist in type B TSVs. This difference is due to the insulation layer process during the TSV fabrication stage [2]. No metal connections, therefore, exist between the TSVs and the local metal power lines.

As highlighted by the solid arrow shown in Fig. 16(a), current is vertically transferred from layer $N-1$ to layer N through the P/G TSVs. The current is subsequently transferred

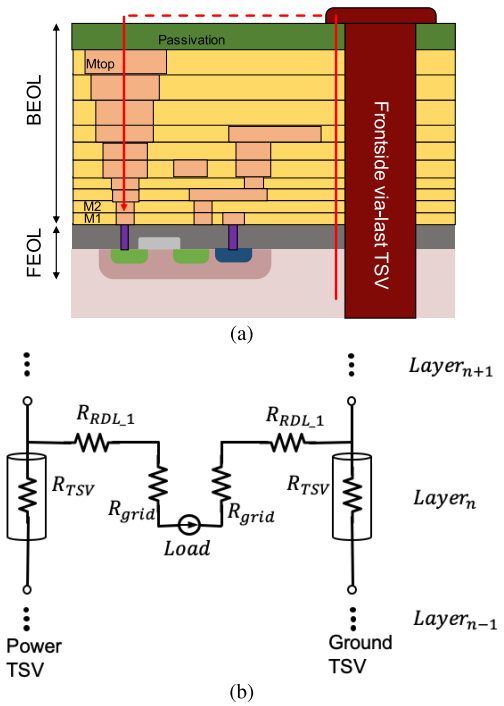

Fig. 16. Type B TSV and current path between TSV and load. (a) Cross-sectional view. (b) Lumped circuit model.

from the P/G TSVs to the global power grid, as shown by the dashed line in Fig. 16(a). As previously discussed, no BEOL metal lines exist to support this horizontal current path. A dedicated type one RDL above the passivation layer is, therefore, required to connect the P/G TSVs to the global power grid. Note that this requirement is one of the major differences between type A and type B TSVs. Similar to type A TSVs, the current is distributed to the loads through the power network within layer N, as highlighted by the solid arrow shown in Fig. 16(a).

A lumped circuit model of a single layer within a 3-D power network with type A TSVs is described here. The current path within a single layer is shown in Fig. 16(b) and can be applied to other layers. R_{TSV}, $R_{\mathrm{RDL_1}}$, and R_{grid} represent the resistance of, respectively, the type B TSV, the type one RDL connecting a TSV to a 2-D power grid, and the 2-D power grid [45]. Note that R_{stack} or R_{MT} in a type A TSV does not exist in a type B TSV, which is replaced, respectively, by R_{TSV} and $R_{\mathrm{RDL_1}}$. The voltage drop within a single layer of a 3-D power network with a type B TSV on layer n within an m layer 3-D IC is

$$V_{\mathrm{drop}}^{n,m} = I_{\mathrm{load}}[(m-n+1)R_{\mathrm{TSV}} + R_{\mathrm{RDL_1}} + R_{\mathrm{grid}}] \quad \text{(B.1)}$$

where the current demand of each layer is I_{load}. Based on (B.1), high current $I_{\mathrm{load}}(m-n+1)$ only passes through the R_{TSV} path.

A type two RDL is also required to support the TSV-to-TSV connections between the adjacent layers that exhibit a TSV mismatch. A comparison among the via-first, via-middle, backside via-last, and frontside via-last TSV is listed in Table V, including the TSV type, RDL type, and TSV to power grid connection. As highlighted in Table V, only

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TABLE V
COMPARISON OF DIFFERENT TSV FABRICATION METHODS

Type of TSV fabrication	TSV type		RDL type		TSV-grid connection	Etching side	Passing layer	Resistivity
	Type A	Type B	Type one	Type two				
Via-first	✓			✓	BEOL	Substrate	Substrate	High
Via-mid	✓			✓	BEOL	Substrate	Substrate	Middle
Backside via-last	✓			✓	BEOL	Substrate	Substrate	Low
Frontside via-last		✓	✓	✓	Type one RDL	Metal	Substrate and metal	Low

the frontside via-last TSV requires both types of RDLs. Also note that significant current passes through R_{stack} to the upper layers in a type A TSV, as shown in (A.1). R_{stack} is the on-chip BEOL, which does not support high current, leading to greater power noise and electromigration. This condition justifies why a type B TSV is assumed in Sections III and IV.

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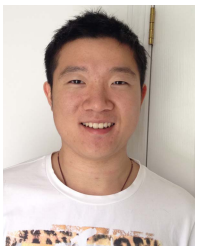

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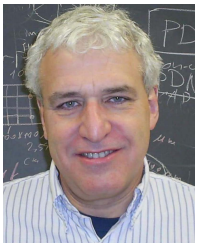

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