On-Board and On-Package Active Capacitors for High Current Systems

Nurzhan Zhuldassov, Yimajian Yan, Mikhail Popovich, and Eby G. Friedman, *Life Fellow, IEEE*

***Abstract*— Due to scaling of semiconductors, the power density in VLSI circuits has increased dramatically. Furthermore, ON-chip power noise requirements have become more stringent as nominal voltages have decreased. As a result, the requirements for voltage variations have become more difficult to satisfy. Voltage drops below the noise margin may cause gate delays, false switching, and even system failure. Passive capacitors are often used to satisfy these stringent voltage drop requirements. However, due to ON-chip and on-package area constraints, including sufficient passive capacitors has become difficult. One solution is active capacitors, which provide a higher density capacitance than passive capacitors. On-package and on-board active capacitors are the focus of this article. An on-board active capacitor has been simulated and experimentally validated using an evaluation board, where a 97-mV reduction in voltage is observed in a 1.2-V system. The simulation model exhibits an accuracy within 10% of the experimental results. Furthermore, the performance of an on-package active capacitor is evaluated for high current conditions and compared with passive capacitors of equal area. A reduction in the voltage drop of 98 mV in an on-package system when compared with a system with on-package passive capacitors is demonstrated in an 800-mV, high current system.**

***Index Terms*— Active circuits, decoupling capacitance, power integrity, voltage regulation.**

I. Introduction

A RELIABLE power supply for integrated circuits (ICs) is of vital importance. This capability is particularly exacerbated with increasing power densities and clock frequencies. The ON-chip power delivery system needs to maintain signal and power integrity, crucial in reducing power noise [1]. Voltage variations cause detrimental effects on circuit performance and reliability such as false logic switching, delay uncertainty, and even functional failure. Consequently, these voltage variations need to be limited. Furthermore, the effects of voltage drops are exacerbated by the variations in fabrication processes [2]. A significant voltage drop can be caused by a sudden demand in current. This voltage drop can be compensated by the primary voltage source, the voltage regulator module (VRM) [3], [4], which supplies current. The voltage source, however, is often placed on-board and is unable to timely respond to sudden increases in current demand.

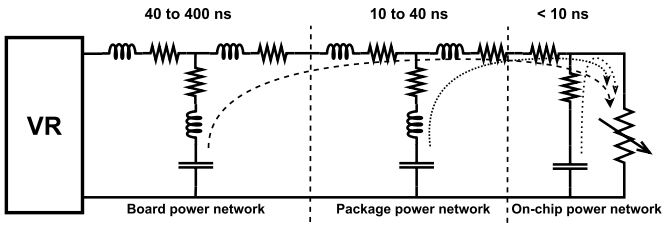

Fig. 1. Response time of decoupling capacitors at different stages (board, package, IC) of a power network.

A common, yet powerful method to mitigate this issue is the use of decoupling capacitors [5], [6], on-board, on-package, and ON-chip [2], [7], [8]. Decoupling capacitors at each physical stage of a system (board, package, and IC) respond at different times after a drop in voltage, supplying current before the primary voltage regulator delivers current to the load. An example of the response time of decoupling capacitors at different stages of the power network is shown in Fig. 1. The response time of these different stages depends upon the impedance characteristics of the power network. The on-board decoupling capacitors typically supply current within 40–400 ns, on-package decoupling capacitors supply current within 10–40 ns, and on-die capacitors supply current in less than 10 ns after a voltage drop. To minimize this drop in voltage, it is preferable to place significant decoupling capacitance close to the load [6]. The area, however, becomes significant when moving from the board to the IC. While it is not difficult to include large decoupling capacitors on-board, placing capacitors on-package and ON-chip is an issue. The available area within the package may be insufficient to place enough capacitance to satisfy instantaneous high current demand, producing a drop in voltage that can exceed voltage noise margins. An example of a voltage drop in a power network with no on-package capacitor is shown in Fig. 2. In this example, three voltage drops are noted. The current is supplied by the on-die decoupling capacitors less than 10 ns after an increase in load current. Between 10 and 40 ns after the increase in load, the current is supplied by the on-package decoupling capacitors. The third drop occurs in 40 ns, after all

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Nurzhan Zhuldassov and Eby G. Friedman are with the Department of Electrical, Computer Engineering University of Rochester, Rochester, NY 14627 USA (e-mail: nzhuldas@ur.rochester.edu).

Yimajian Yan and Mikhail Popovich are with Power Integrity, Google LLC Sunnyvale, Rochester, CA 94089 USA.

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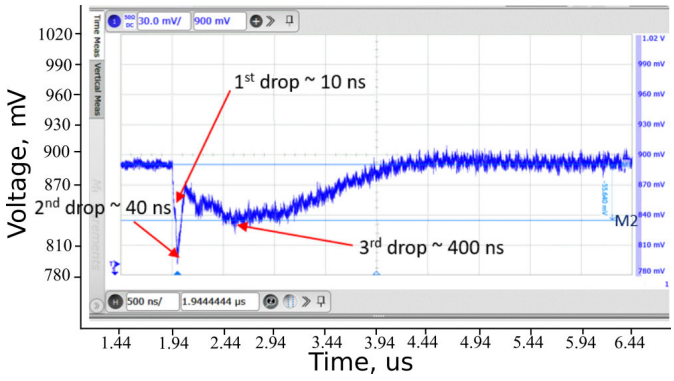


Fig. 2. Voltage drop with no on-package capacitance.

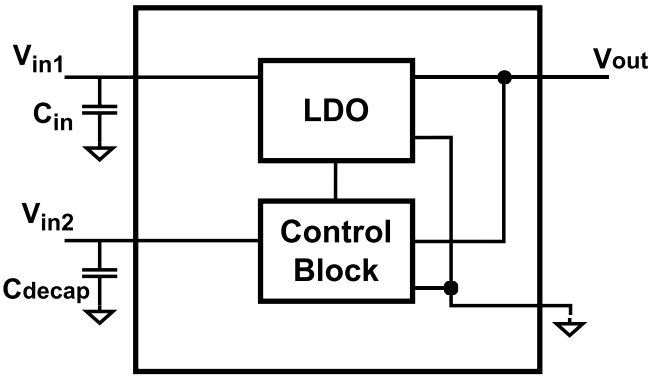


Fig. 3. LDO-based active capacitor.

the charge in the previous stages has been depleted. This current is supplied by the board decoupling capacitors until 400 ns, when the voltage regulator starts to supply current. Note in Fig. 2, the second drop is the largest and below the voltage noise margin (note the solid line M2) Alternative capacitors, such as deep trench capacitors [9], [10] and metal–insulator–metal capacitors [11], which satisfy higher power density requirements, have been proposed. The fabrication cost of these capacitors, however, is much greater than traditional bulk and ceramic capacitors.

An alternative method to provide sufficient capacitance at low area is active capacitors [12]. Several active capacitor topologies have been proposed, including topologies based on dc links [13] and low dropout (LDO) regulators [14]. An active capacitor behaves similar to a traditional capacitor, supplying current when a drop in voltage is detected. A method for reducing the voltage drop with an LDO-based active capacitor is the focus of this article. A practical power network is evaluated, and a lower voltage drop is demonstrated, both experimentally and in simulation. The functionality of the active capacitor model is also verified through simulation [15]. To confirm the simulation results, a printed circuit board with an on-board active capacitor has been fabricated and tested. Both the simulation and experimental measurements on the printed circuit board demonstrate the effectiveness of an active capacitor in reducing voltage drops. The efficacy of the model of the active capacitor is further evaluated by simulating a practical power delivery network under high current demand conditions within a package. These results indicate that an active capacitor successfully minimizes voltage drops in systems with high current demand.

The rest of this article is organized as follows. Insight into the behavior of an active capacitor is described in Section II. Both the simulation and experimental performance of an on-board active capacitor are discussed in Section III. A power delivery network with an on-package active capacitor is described in Section IV. Some conclusions are offered in Section V.

II. Background

An active capacitor is a circuit composed of transistor-based components behaving similar to a passive capacitor [12]. The field of active capacitors is characterized by a scarcity of studies focused on design, modeling, and analysis, increasing the need for further investigation and advancement [12], [13].

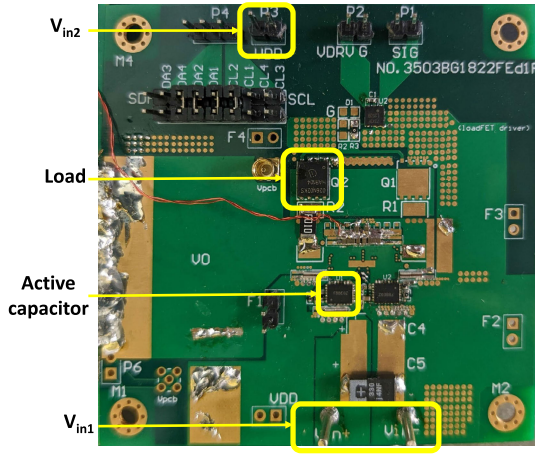
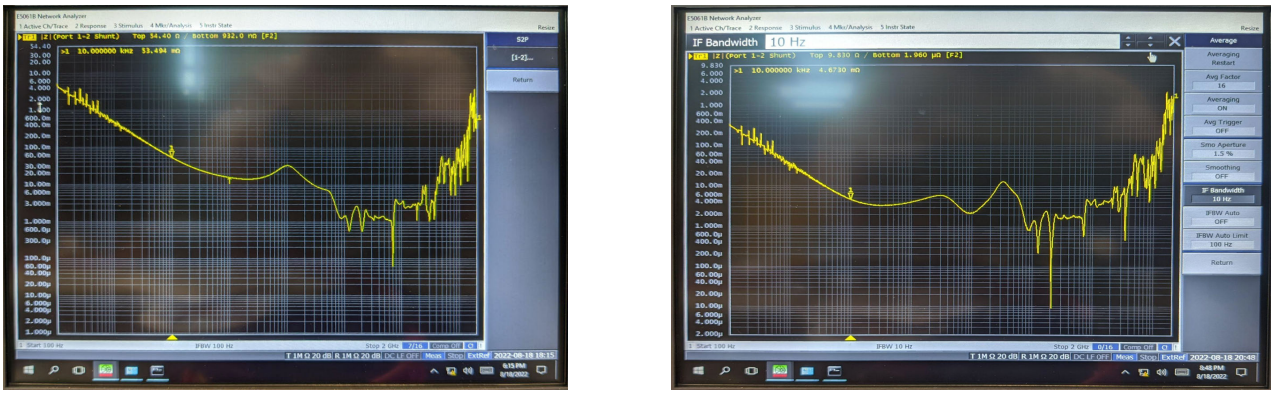


Fig. 4. Printed circuit board used to evaluate the performance of an active capacitor.

An active capacitor comprises several passive elements, samplers, conditioners, an integrated controller, and gate drivers. Similar to a passive capacitor, an active capacitor has two terminals. In an active capacitor, a passive capacitor is serially connected to a low-voltage, full bridge converter, which manages variations in the voltage and current [12]. Voltage control is provided by assessing the voltage across the capacitors within an active capacitor and does not require current feedback.

The active capacitor evaluated here is based on an LDO. A simplified LDO-based active capacitor is depicted in Fig. 3. The active capacitor requires an external power input, illustrated in Fig. 3 as V_{in1} and V_{in2}. The circuit consists of a control block, gate drivers (MOSFETs), a bandpass filter to manage the ripple response, and input and output passive capacitors. Charge from the input capacitors flows to the gate drivers, which passes charge to the output capacitors through the LDO. The gain in capacitance increases in proportion to the ratio of the input voltage noise margin $V\text{in}_{NM}$ to the output voltage noise margin $V\text{out}_{NM}$,

$$\text{Gain in capacitance} = \frac{V\text{in}_{NM}}{V\text{out}_{NM}}. \tag{1}$$



(a) (b)

Fig. 5. Impedance of the active capacitor on the circuit board. (a) Input. (b) Output.

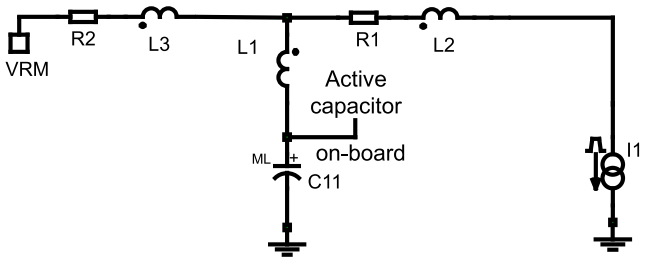


Fig. 6. Power network to assess the effectiveness of an active capacitor.

TABLE I
PARASITIC IMPEDANCES OF THE SIMULATED AND EXPERIMENTAL EVALUATION BOARD

	Inductance	Resistance
Board to active capacitor	6.4 nH	12.8 $m\Omega$
Active capacitor to load	2.5 nH	3.1 $m\Omega$

The voltage noise margin describes the acceptable voltage drop supporting correct operation. The input of the LDO is less sensitive to the noise margin than the load. The total capacitance of an active capacitor is

$$C = \frac{V\text{in}_{NM}}{V\text{out}_{NM}} C_{\text{decap}} \tag{2}$$

where C_{decap} is the capacitance of a passive capacitor at the input of the LDO.

III. EVALUATION OF ACTIVE CAPACITOR

To assess the effectiveness of an active capacitor, a power network is included on the printed circuit board, with the active capacitor positioned in close proximity to the load. The performance of an on-board active capacitor is evaluated with simulation and experimental measurements. The simulations are described in Section III-A. The experimental measurements are discussed in Section III-B.

A. Simulation of Voltage Drop

The voltage drop is assessed using the SIMPLIS simulation tool [15], with the circuit constructed using extracted impedance characteristics of an evaluation board, as depicted in Fig. 4. The impedance characteristics are obtained using a Keysight E5061B network analyzer and are presented in Fig. 5, showcasing the impedance at both the input and output of the active capacitor.

The constructed power network is shown in Fig. 6. Capacitors are placed on the evaluation board. The value of the parasitic inductances and resistances within the power delivery

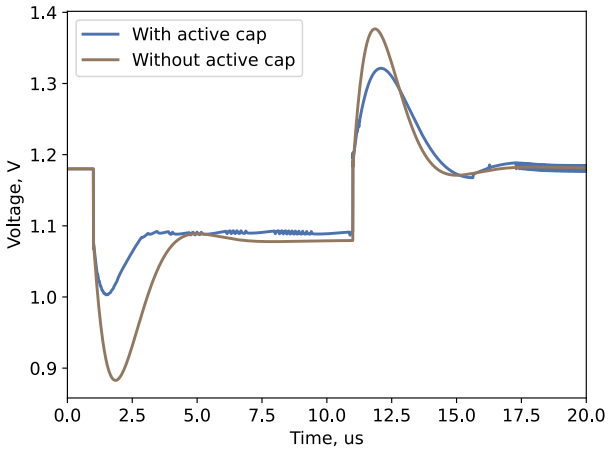


Fig. 7. Transient voltage drop in the evaluation board. The voltage drop is measured both without an active capacitor and with an active capacitor.

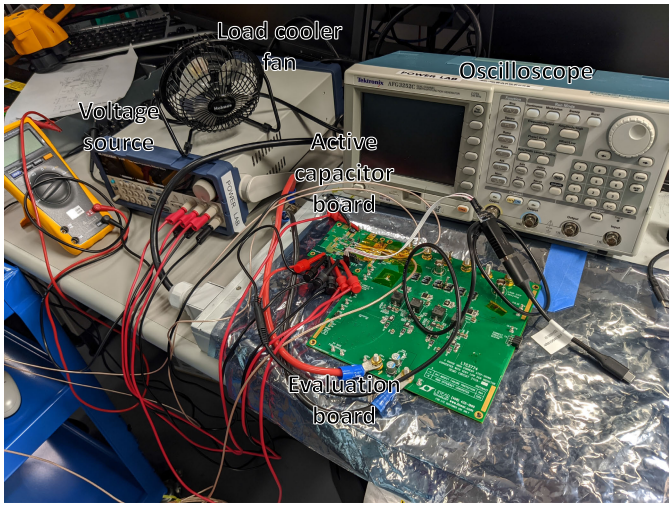


Fig. 8. Setup of work station to measure the performance of the active capacitor. Two boards are fabricated: a board with an active capacitor and a board to simulate sudden demands in current.

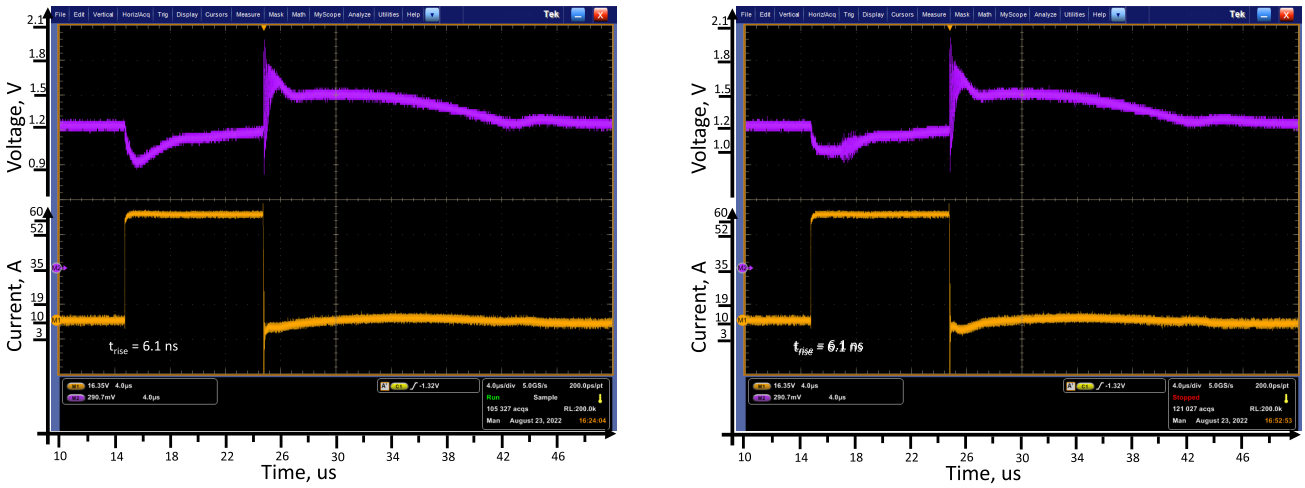


Fig. 9. Transient voltage drop in printed circuit board. (a) Without active capacitor. (b) With active capacitor. The bottom curve is the load current, which increases to 50 A within 6.1 ns. The top curve is the output voltage at 1.2 V. The drop in voltage without an active capacitor is 300 mV and with an active capacitor is 203 mV.

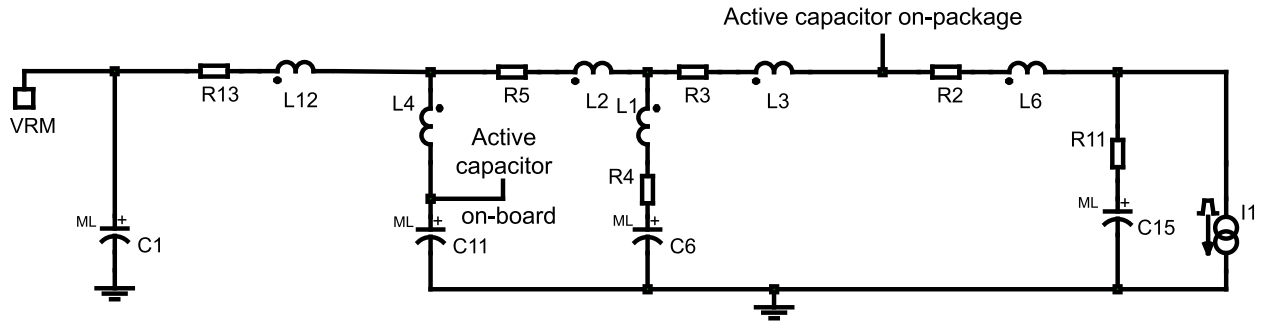


Fig. 10. Power network to evaluate the performance of an active capacitor. The voltage drop without an active capacitor and with an active capacitor, both on-package and on-board, is determined. Only one active capacitor is enabled at a time.

network is listed in Table I. The nominal voltage at the load is 1.2 V. The load current is increased from 10 to 60 A in 6.1 ns. The voltage drop at the load both without an active capacitor and with an active capacitor is illustrated in Fig. 7. Without the active capacitor, the drop in voltage at the load is 317 mV. When an active capacitor is placed on-board, the voltage drop is 200 mV, lowering the drop by 117 mV.

B. Measured Voltage Drop

The simulated model of a power delivery network with an on-board active capacitor has been verified through experimental measurements. To evaluate the performance of an active capacitor, a board with an active capacitor is considered, as illustrated in Fig. 4.

The work station used to measure the performance is depicted in Fig. 8. The nominal voltage at the load is 1.2 V. As in the simulation, a 50-A increase in current in 6.1 ns is induced. The load voltage is evaluated without and with an active capacitor. In Fig. 9, the waveform of the load voltage is shown at the top and the current waveform at the bottom. As noted in Fig. 9(a), the drop in voltage without an active capacitor is 300 mV. When the active capacitor is enabled, the drop in voltage is lowered by 97 to 203 mV.

The outcome of both the simulation and experiment demonstrates a substantial improvement in lowering the voltage drop.

TABLE II
NOISE PERFORMANCE OF ACTIVE CAPACITOR

	Simulation	**Experiment**
Nominal voltage	1,200 mV	1,200 mV
V_{drop} without active capacitor	317 mV	300 mV
V_{drop} with on-board active capacitor	200 mV	203 mV
Improvement	37%	32%

These results are listed in Table II. The 1.2-V system exhibits a 37% reduction in voltage drop, which is confirmed by experiment (demonstrating a 32% improvement). Note that the simulation and experimental data differ by 10%.

IV. ON-PACKAGE APPLICATION

The active capacitor is particularly appropriate for applications requiring high current due to the high charge density. The compact size of 1.35 mm by 1.1 mm (0.053" by 0.043") renders the active capacitor suitable to replace the conventional passive capacitors on a board and package. Accommodating an on-package active capacitor enhances the power density and reduces the delay time within the package.

The power network being evaluated is shown in Fig. 10. Capacitors are attached at different stages within the power network, on-board, on-package, and on-die. The value of the

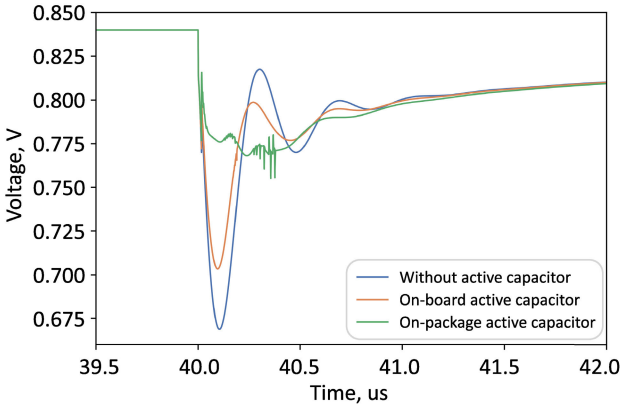


Fig. 11. Transient voltage drop with an active capacitor. The voltage drop is measured without an active capacitor and with an active capacitor for both on-package and on-board.

TABLE III
PARASITIC IMPEDANCES OF THE SIMULATED POWER DELIVERY NETWORK

	Inductance	Resistance
Board to on-board active capacitor	21 pH	265 $\mu\Omega$
Board to package	54 pH	490 $\mu\Omega$
Package to on-package active capacitor	93 pH	540 $\mu\Omega$
On-package active capacitor to load	52 pH	300 $\mu\Omega$

parasitic inductances and resistances within the power delivery network is listed in Table III. The nominal voltage at the load is 840 mV. The load current is increased from 50 to 140 A in 17 ns. Two scenarios, an on-package active capacitor and on-board active capacitor, are considered, removing the passive capacitors to maintain similar area. The voltage drop at the load without an active capacitor and with an active capacitor, both on-package and on-board, is illustrated in Fig. 11. When only passive capacitors are placed on-package, the drop in voltage at the load is 170 mV. When an active capacitor is placed on-board, the voltage drop is 140 mV. When an active capacitor is placed on-package, the voltage drop is reduced to 72 mV, a 58% decrease in voltage drop when compared with only passive capacitors.

V. CONCLUSION

Semiconductor scaling has resulted in increasing power density, placing strict requirements on noise margins. Due to larger voltage drops with higher load currents, significant decoupling capacitance is often required. On-package and ON-chip area is, however, limited.

An active capacitor integrated onto a board has undergone testing, both through simulation and experimental measurements, with the results confirming the effectiveness of active capacitors. The simulation results indicate that the addition of an active capacitor reduces the voltage drop from 317 to 200 mV, representing an improvement of 117 mV (37% improvement in voltage drop). The simulation is confirmed by the experimental measurements, which demonstrate a reduction in voltage drop from 300 to 203 mV, resulting in an improvement of 97 mV (reduction by 32%). The simulated and measured results differ by 10%.

An active capacitor can additionally be used where low voltage drops are encountered. Increasing the capacitance by active capacitors improves the stability and enhances the transient response, thereby ensuring rapid recovery from sudden changes in current. Furthermore, active capacitors reduce stress on the components and increase the efficiency, as the output voltage can be maintained at close to constant levels.

On-package active capacitors are also a promising solution due to the superior capacitive density when compared with passive capacitors. The simulation and experimental results suggest that an active capacitor can be used in on-package applications for high current demand systems. Three different scenarios are considered: without active capacitor, with active capacitor placed on-package, and with active capacitor placed on-board. In an 800-mV system with a 140-A current load, the voltage drop is reduced from 170 mV with passive capacitors to 72 mV using an active capacitor of the same area as the passive capacitors, resulting in a 58% decrease in voltage drop. These findings demonstrate the potential of active capacitors for reducing voltage drops in systems requiring high current.

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