Closed-Form Expressions of 3-D Via Resistance, Inductance, and Capacitance

Ioannis Savidis and Eby G. Friedman, *Fellow, IEEE*

***Abstract*—Closed-form expressions of the resistance, capacitance, and inductance for interplane 3-D vias are presented in this paper. The closed-form expressions account for the 3-D via length, diameter, dielectric thickness, and spacing to ground. A 3-D numerical simulation is used to extract electromagnetic solutions of the resistance, capacitance, and inductance for comparison with the closed-form expressions, revealing good agreement between simulation and the physical models. The maximum error for the resistance, capacitance, and inductance is less than 8%.**

***Index Terms*—Closed-form expressions, electrical characterization, TSV, 3-D.**

I. Introduction

THE ERA of rapid technology scaling has brought revolutionary advancements in system-level integration. Integrated circuits that once performed simple computations have evolved to advanced ubiquitous microprocessors. The natural evolution of the microprocessor to incorporate both analog and digital circuitry has led to system-on-chip integrated technologies. As integrated circuits become more complex, new technologies are required to continue this trend toward massive system-level integration. A potential technology that continues the evolution toward gigascale complexity is 3-D integration [1].

Three-dimensional integration is a novel technology of growing importance that has the potential to offer significant performance and functional benefits as compared with 2-D ICs. Three-dimensional integration provides enhanced interconnectivity, high device integration density, a reduction in the number and length of the long global wires, and the ability to combine disparate heterogeneous technologies [2]–[4]. The primary technological innovation required to exploit the benefits of 3-D integration is the development of a 3-D through silicon via (TSV) technology. Much work is needed to properly characterize and model these interplane TSVs.

Accurate closed-form models of the 3-D via impedance provide an efficient method to characterize the performance of signal paths containing through silicon vias. These closed-form expressions are similar in form to the models developed in [5] and [6] that characterize the capacitance and inductance [7] of on-chip interconnects for VLSI circuits. Most previous work characterizing 3-D vias has focused on bulk silicon and emphasized the experimental extraction of the via resistance and capacitance. Due to the large variation in the 3-D via diameter, length, dielectric thickness, and fill material, a wide range of measured resistances, capacitances, and inductances has been reported in the literature. Single 3-D via resistance values vary from 20 mΩ to as high as 350 Ω [8]–[13], while reported capacitances vary from 2 fF to over 1 pF [14]–[16]. A few researchers have reported measured via inductances that range from as low as 4 pH to as high as 255 pH [9], [13], [16]. Alternatively, preliminary work on modeling 3-D vias has primarily focused on the resistance and capacitance of simple structures to verify measured RLC impedances while providing some physical insight into the 3-D via to 3-D via capacitive coupling [8], [13]–[15]. Furthermore, preliminary work in the electrical modeling of bundled TSVs has been reported in [17]–[19]. This paper expands on this early work and presents closed-form expressions for the resistance, inductance, and capacitance of TSVs (3-D vias), accounting for via length, via diameter, dielectric thickness, and fill material.

This paper will proceed as follows. Before the closed-form expressions of the resistance, capacitance, and inductance are presented, the technique of modeling the 3-D vias as simple cylinders without top and bottom copper landings is reviewed in Section II. Background information describing the geometry of the 3-D vias and the Ansoft Quick 3-D toolset used to simulate the structures for comparison with the proposed models are also presented in Section II. Closed-form expressions of the TSV resistance for both DC and higher frequencies are provided in Section III. Expressions characterizing the 3-D via inductance at both DC and high frequency are provided in Section IV. A model of the mutual inductance between two 3-D vias is also provided in this section. Models of the 3-D via capacitance are provided in Section V. A few concluding remarks are provided in the final section of this paper.

II. Modeling 3-D Vias as Cylinders

The structural complexity of a 3-D via is treated as an equivalent cylindrical structure. A 3-D via typically includes a tapered cylindrical TSV with both a bottom and top metal landing. The electrical parameters produced by the Ansoft electromagnetic simulation tool for a 3-D via represented as a cylinder with top and bottom copper landings [see Fig. 1(a)] are compared

Manuscript received February 12, 2009; revised April 29, 2009. Current version published August 21, 2009. This work was supported in part by the National Science Foundation under Contracts CCF-0541206, CCF-0811317, and CCF-0829915, by Grants from the New York State Office of Science, Technology and Academic Research to the Center for Advanced Technology in Electronic Imaging Systems, and by Grants from Intel Corporation, Eastman Kodak Company, and Freescale Semiconductor Corporation. The review of this paper was arranged by Editor H. Masuda.

The authors are with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY 14627 USA (e-mail: iosavid@ece.rochester.edu; friedman@ece.rochester.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2009.2026200

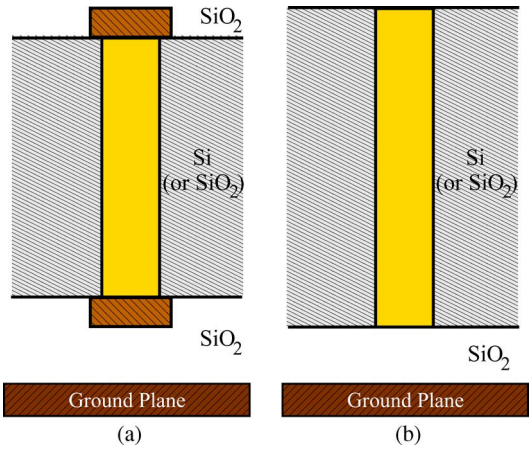

Fig. 1. Three-dimensional via structure. (a) Three-dimensional via with top and bottom copper landings. (b) Equivalent structure without metal landings.

TABLE I
PERCENT ERROR BETWEEN THE 20 μm DIAMETER 3-D VIA MODEL AND THE EQUIVALENT CYLINDRICAL MODEL

	R		L		C
a.r.	DC	1 GHz	DC	f_{asym}	
0.5	41.6	3.6	0	-16.4	6.4
1	16.9	-2.0	0	-13.6	6.2
3	5.4	0.7	-0.04	-0.6	5.4
5	2.9	-0.2	-0.04	-1.4	4.9
7	2.2	-0.4	0.01	-1.4	4.0
9	1.9	0.4	0.02	-0.03	3.1

with those of an equivalent length cylindrical via without the metal landings [see Fig. 1(b)]. A comparison of simulation results for the two aforementioned TSV configurations reveals less than a 7% difference in the resistance, inductance, and capacitance. The exceptions only arise for the DC resistance and high frequency inductance when the aspect ratio is between 0.5 and 1, as listed in Table I. This behavior implies that the use of a simple cylindrical structure without metal landings is sufficient to represent a 3-D via.

The dimensions of a 3-D via are highly technology dependent. For SOI processes, where the buried oxide behaves as a natural stop for wafer thinning, the length $\mathfrak{L}$ of the TSVs is much shorter than the bulk counterparts. The diameter D of the vias follows a similar pattern, where SOI processes utilize smaller diameters than bulk technologies. The 3-D via models developed here for an SOI process therefore consider diameters of 1, 5, and 10 μm, while the 3-D vias implemented in bulk silicon have diameters ranging between 20 and 60 μm. A 20 μm diameter is chosen for the comparison between the 3-D via model and the equivalent cylindrical structure. In all cases, the via lengths are chosen to maintain an aspect ratio $\mathfrak{L}/D$ of 0.5, 1, 3, 5, 7, and 9. In addition, the dielectric thickness for the bulk processes is 1 μm, and the material filling the 3-D vias in both SOI and bulk technologies is tungsten.

The Ansoft Quick 3-D (Q3D) software is used to examine the RLC impedances of the TSVs [20]. Q3D is a 3-D/2-D quasi-static electromagnetic-field simulator used to extract the parasitic impedances and electrical parameters. The tool solves Maxwell's equations by utilizing the finite-element method [21] and the method of moments [22], [23] to compute the RLC or $RLCG$ parameters of a 3-D structure. With regard to the inductance, Q3D is used to determine the asymptotic values of the inductance, the DC and high frequency $(f_{\rm asym})$ values described in the paper and shown in Fig. 2. Q3D simulations do not provide the inductance values for frequencies between the DC and high frequency extrema; the closed-form expression for inductance is therefore valid for frequencies lower and higher than the transitional frequency range (200–800 MHz for this particular example).

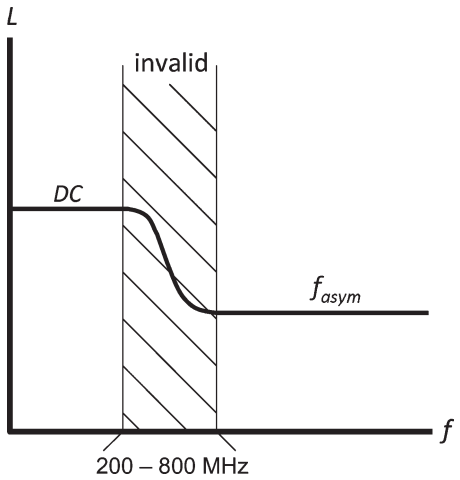

Fig. 2. Frequency range for which Q3D models and closed-form inductance expressions are valid.

III. CLOSED-FORM RESISTANCE MODEL OF A 3-D VIA

Closed-form expressions of the 3-D via resistance at DC and 1 GHz are presented next as (1)–(3), respectively. The DC resistance is only dependent on the length $\mathfrak{L}$, radius $\Re$, and conductivity σ_W of tungsten. The resistance at a frequency of 1 GHz, however, is also dependent on the skin depth, which is the depth below the surface of a conductor where the current density has dropped by a factor of e [24]. Two guidelines are provided in [24] that ensure that the high frequency resistance is valid when considering skin effects. These two guidelines are 1) the return paths are infinitely distant, and 2) all radii of curvature and thicknesses are at least three to four skin depths. The second guideline necessitates the use of the fitting parameter α in (2) and (3) for SOI processes. In addition, α accounts for current losses in the substrate in both bulk and SOI processes.

$$R_{\rm DC} = \frac{1}{\sigma_W}\frac{\mathfrak{L}}{\pi\Re^2} \tag{1}$$

$$R_{1\,\rm GHz} = \begin{cases} \alpha\frac{1}{\sigma_W}\frac{\mathfrak{L}}{\pi[\Re^2-(\Re-\delta)^2]}, & \text{if } \delta < \Re \quad (2) \\ \alpha\frac{1}{\sigma_W}\frac{\mathfrak{L}}{\pi\Re^2}, & \text{if } \delta \geq \Re \quad (3) \end{cases}$$

The effect of the skin depth is included in the 1 GHz resistance as a reduction in the cross-sectional area of the 3-D via. The skin depth δ is

$$\delta = \frac{1}{\sqrt{\pi f \mu_o \sigma_W}} \tag{4}$$

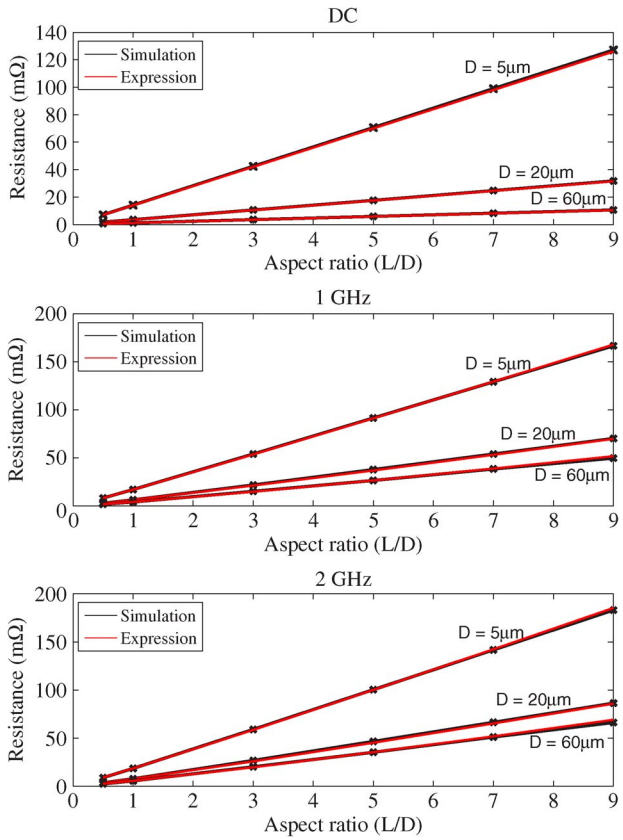

Fig. 3. Resistance of a cylindrical 3-D via at DC, 1 GHz, and 2 GHz.

where f is the frequency and μ_o is the permeability of free space. The permeability of free space is used as neither silicon nor silicon dioxide are magnetic materials.

As noted earlier, the α term in (2) and (3) is an empirical constant used to fit the resistance to the simulations and is

$$\alpha = \begin{cases} 0.0472 D_{\mu\mathrm{m}}^{0.2831} \ln\left(\frac{\mathfrak{L}}{D}\right) + 2.4712 D_{\mu\mathrm{m}}^{-0.269}, & \text{if } \delta < \mathfrak{R} \quad (5) \\ 0.0091 D_{\mu\mathrm{m}}^{1.0806} \ln\left(\frac{\mathfrak{L}}{D}\right) + 1.0518 D_{\mu\mathrm{m}}^{0.092}, & \text{if } \delta \geq \mathfrak{R}. \quad (6) \end{cases}$$

All dimensions (D, S, L) are in meters unless the subscript μm is used to denote micrometers.

For frequencies other than DC and 1 GHz, (2) and (3) can be adjusted to other frequencies using (7). Equation (7) has been evaluated at a frequency of 2 GHz. The resistance of a 3-D via with diameters of 5, 20, and 60 μm at frequencies of DC, 1 GHz, and 2 GHz are illustrated in Fig. 3.

$$R_{f_{\mathrm{new}}} = (R_{1\,\mathrm{GHz}} - R_{\mathrm{DC}}) \sqrt{\frac{f_{\mathrm{new}}}{f_{1\,\mathrm{GHz}}}} + R_{\mathrm{DC}}. \quad (7)$$

The proximity effect [24] is examined through simulations of two 3-D vias over a ground plane. These simulations reveal less than a 0.25% change in the resistance at all examined frequencies as compared with a single 3-D via over a ground plane; these results are therefore not included. This characteristic implies that the proximity of the second 3-D via as a return path does not significantly affect the resistance of the first via. The insignificance of the proximity effect is primarily a consequence of the relatively short length of the vias and the small space between the 3-D vias which is at least equal to the diameter of a single 3-D via.

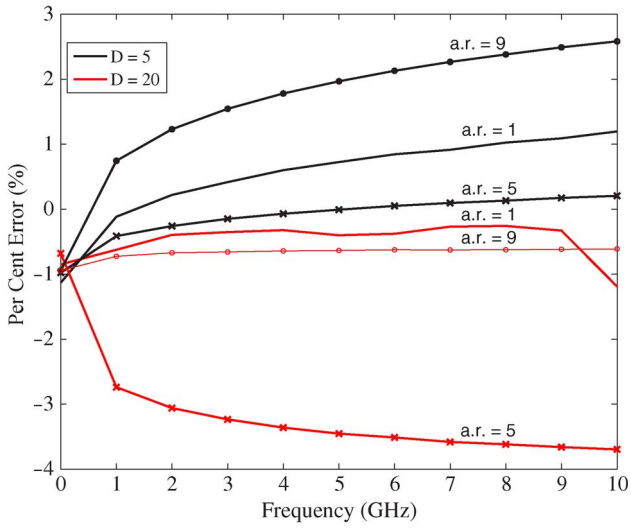

Fig. 4. Percent error as a function of frequency for the resistance of a 3-D via (a.r. = aspect ratio).

An analysis of the percent error between simulation and the closed-form resistance expressions as a function of frequency is provided. These results indicate less than 5% error between simulation and the closed-form expressions for all frequencies between DC and 10 GHz. The percent error for two diameters, 5 and 20 μm, and three aspect ratios, 1, 5, and 9, is shown in Fig. 4.

The percent variation between simulation and the model at frequencies of DC, 1 GHz, and 2 GHz is included in Appendix A as Tables II–IV, respectively. The DC resistance based on the closed-form expressions produces less than 2% error, and the 1 and 2 GHz resistance produces less than a 5.5% difference from the equivalent model characterized by Q3D.

IV. Closed-Form Inductance Model of a 3-D Via

The DC and high frequency self- and mutual inductance of two equal length TSVs is included in Section IV-A. In Section IV-B, the DC and high frequency mutual inductance between two non-equal length TSVs is described. Non-equal length vias are used to approximate the mutual inductance between a single TSV and a stack of TSVs propagating a signal through multiple planes.

A. Inductance of Equal Length 3-D Vias

Expressions for the DC and high frequency partial self-(L_{11}) and mutual (L_{21}) inductances are provided in (8)–(11). The modeled DC and high frequency inductances are asymptotic values of the inductance. These expressions do not account for the transition in inductance from low to high frequency (in the 200–800 MHz range for this particular technology). Note that the inductance transitions smoothly from low to high frequency, indicating that the 3-D via inductance is bound by the DC (upper bound) and asymptotic (lower bound) values within this

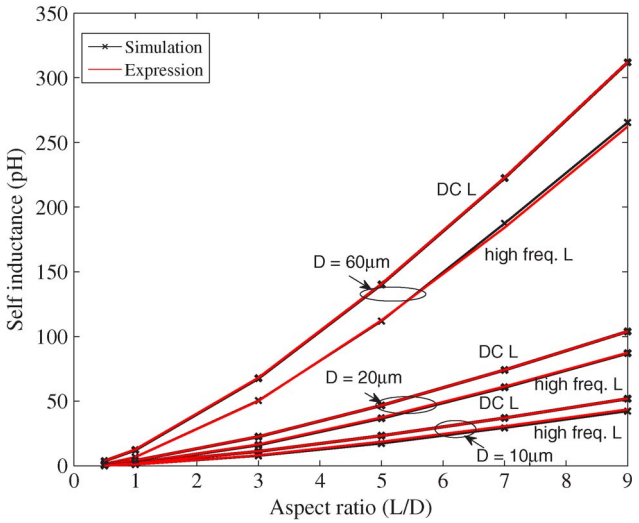

Fig. 5. Self-inductance L_{11} of a cylindrical 3-D via.

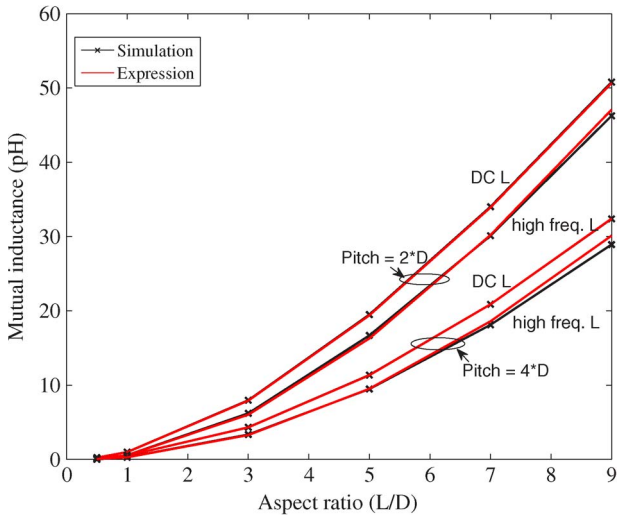

Fig. 6. Mutual inductance L_{21} for a 20 μm diameter cylindrical 3-D via.

transitional range. The inductance models are based on [25] with a fitting parameter to adjust for inaccuracies in the Rosa expressions. The expressions derived by Rosa assume that the length $\mathfrak{L}$ is much larger than both the radius $\mathfrak{R}$ (or diameter D) and the pitch P between the conductors. As $\mathfrak{L}$ is not larger than $\mathfrak{R}$ or P in all of the 3-D via structures examined in this paper, parameters α and β are used to adjust the partial inductances in (8)–(11), as shown in the expressions at the bottom of this page [25], where

$$\alpha = \begin{cases} 1 - e^{\frac{-4.3\,\mathfrak{L}}{D}}, & \text{if } f = \text{DC} \quad (12) \\ 0.94 + 0.52e^{-10\left|\frac{\mathfrak{L}}{D}-1\right|}, & \text{if } f > f_{\text{asym}} \quad (13) \end{cases}$$

$$\beta = \begin{cases} 1, & \text{if } f = \text{DC} \quad (14) \\ 0.1535 \ln\left(\frac{\mathfrak{L}}{D}\right) + 0.592, & \text{if } f > f_{\text{asym}}. \quad (15) \end{cases}$$

The α parameter used to adjust the partial self-inductance approaches unity at DC and 0.94 at high frequencies with increasing aspect ratio $\mathfrak{L}/D$. β, which is used to adjust the partial mutual inductance, is unity at DC and ranges between 0.49 and 0.93 at high frequencies as the aspect ratio increases from 0.5 to 9, respectively. The Rosa expressions are most inaccurate when calculating the mutual inductance of a small aspect ratio 3-D via operating at high frequencies. A comparison of both the partial self- and mutual inductances for the adjusted Rosa expressions with Q3D simulations is shown in Figs. 5 and 6, respectively.

B. Inductance of Non-Equal Length 3-D Vias

An expression for the mutual inductance at DC between two TSVs with nonequal lengths is provided in (16). As for the previous topologies, the DC mutual inductance is the worst case inductance, as shown in Fig. 2. Note also that the delay characteristics of a conductor are weakly correlated to the inductance [26], [27]; the DC and f_{asym} inductances therefore produce similar delay effects.

$$L_{21} = \alpha\beta\frac{\mu_o}{2\pi}\left[\ln\left(\frac{\mathfrak{L}_1+\sqrt{\mathfrak{L}_1^2+P^2}}{P}\right)\mathfrak{L}_1 + P - \sqrt{\mathfrak{L}_1^2+P^2}\right] \quad (16)$$

$$\alpha = 0.8 + 0.1945\left(\frac{S}{D}\right)^{0.52} \quad (17)$$

$$\beta = \beta_1 - 2e^{-0.3\frac{\mathfrak{L}_2}{\mathfrak{L}_1}+\beta_2} \quad (18)$$

$$\beta_1 = 2.1 + 4e^{-0.375\frac{\mathfrak{L}_1}{D}-0.1} \quad (19)$$

$$\beta_2 = e^{-0.21\frac{\mathfrak{L}_1}{D}+0.6} - 0.57. \quad (20)$$

The α parameter adjusts the partial mutual inductance between two non-equal length 3-D vias, accounting for the separation between vias. The β parameter adjusts the mutual inductance based on the ratio of the larger length 3-D via $\mathfrak{L}_2$

$$DC: \begin{cases} L_{11} = \alpha\frac{\mu_o}{2\pi}\left[\ln\left(\frac{\mathfrak{L}+\sqrt{\mathfrak{L}^2+\mathfrak{R}^2}}{\mathfrak{R}}\right)\mathfrak{L} + \mathfrak{R} - \sqrt{\mathfrak{L}^2+\mathfrak{R}^2} + \frac{\mathfrak{L}}{4}\right] & (8) \\ L_{21} = \beta\frac{\mu_o}{2\pi}\left[\ln\left(\frac{\mathfrak{L}+\sqrt{\mathfrak{L}^2+P^2}}{P}\right)\mathfrak{L} + P - \sqrt{\mathfrak{L}^2+P^2}\right] & (9) \end{cases}$$

$$f_{\text{asym}}: \begin{cases} L_{11} = \alpha\frac{\mu_o}{2\pi}\left|\ln\left(\frac{2\mathfrak{L}}{\mathfrak{R}}\right) - 1\right|\mathfrak{L} & (10) \\ L_{21} = \beta\frac{\mu_o}{2\pi}\left[\ln\left(\frac{\mathfrak{L}+\sqrt{\mathfrak{L}^2+P^2}}{P}\right)\mathfrak{L} + P - \sqrt{\mathfrak{L}^2+P^2}\right] & (11) \end{cases}$$

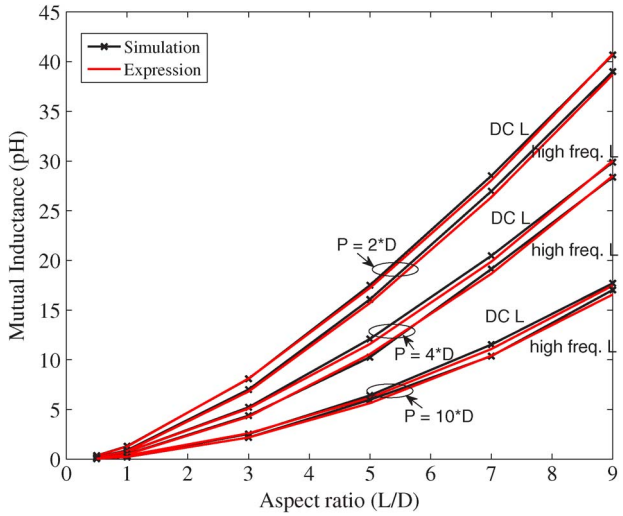

Fig. 7. Mutual inductance L_{21} for two 3-D vias with different lengths ($D = 10\ \mu$m, $3\mathfrak{L}_1 = \mathfrak{L}_2$).

(which represents multiple vertically stacked 3-D vias) to the shorter length via $\mathfrak{L}_1$ (a single 3-D via). $\mathfrak{L}_2$ is therefore always an integer multiple of $\mathfrak{L}_1$. The β term is dependent on the aspect ratio $\mathfrak{L}_1/D$ of a single TSV (non-stacked), as shown by β_1 and β_2. A comparison between the mutual inductance produced by (16) with Q3D simulations is shown in Fig. 7.

The high frequency inductance f_{asym} is determined by multiplying the value produced by (16) with

$$\gamma = 0.955 - 1.1e^{-0.75-0.5\frac{\mathfrak{L}_1}{D}}. \tag{21}$$

The γ term is only dependent on the aspect ratio of a single non-stacked TSV.

The self- and mutual inductance equations produce less than an 8% variation from electromagnetic simulation. The percent variations between simulation and the model of the self- and mutual inductances are listed in Appendix B in Tables V and VI, respectively, and the DC and f_{asym} mutual inductances of two non-equal length 3-D vias are listed in Tables VII and VIII, respectively. The error in all of these tables does not exceed 8% except in those cases where the pitch between vias is greater than $5 \cdot D$ and the aspect ratio is less than two; in these cases, the error does not exceed 30%. The larger error in these cases is due to the small mutual inductance (less than 0.05 pH). The small mutual inductance exacerbates the percent error between (9), (11), or (16) and the simulation results.

V. Closed-Form Capacitance Model of a 3-D Via

Prior works, [13] and [14], examining the capacitance of bulk 3-D vias have neglected two important physical characteristics. The first issue is the formation of a depletion region in the bulk substrate surrounding the TSV, and the second issue is the assumption that the electrical field lines from the 3-D via terminate on a cylinder surrounding the via dielectric liner. Equations (22) and (23) from [13] and [14], respectively, overestimate the 3-D via capacitance,

$$C = \frac{\epsilon_{\text{SiO}_2}}{t_{\text{diel}}} 2\pi\mathfrak{R}\mathfrak{L} \tag{22}$$

$$C = \frac{\epsilon_{\text{SiO}_2}}{\ln\left(\frac{\mathfrak{R}+t_{\text{diel}}}{\mathfrak{R}}\right)} 2\pi\mathfrak{L}. \tag{23}$$

Equation (24) accounts for both the formation of a depletion region surrounding a p-type bulk substrate and the termination of the electrical field lines on a ground plane below the 3-D via. The termination of the field lines from the 3-D via to the ground plane forms a capacitance to the on-chip metal interconnect,

$$C = \alpha\beta \cdot \frac{\epsilon_{\text{SiO}_2}}{t_{\text{diel}} + \frac{\epsilon_{\text{SiO}_2}}{\epsilon_{\text{Si}}} x_{\text{d}Tp}} 2\pi\mathfrak{R}\mathfrak{L}. \tag{24}$$

Note that (24) is dependent on the depletion region depth x_{dTp} in doped p-type silicon (the doped acceptor concentration N_A is 10^{21} m^{-3} in this case). The depletion region is, in turn, dependent on the p-type silicon work function ϕ_{f_p}. The intrinsic semiconductor concentration n_i is 1.5×10^{16} m^{-3}, and the silicon permittivity is $11.7 \times (8.85 \times 10^{-12})$ F/m. The thermal voltage kT/q at $T = 300$ K is 25.9 mV, where q is the electron charge (1.6×10^{-19} C) and k is the Boltzmann constant, 1.38×10^{-23} J/K,

$$x_{dTp} = \sqrt{\frac{4\epsilon_{\text{Si}}\phi_{f_p}}{qN_A}} \tag{25}$$

$$\phi_{f_p} = V_{\text{th}} \ln\left(\frac{N_A}{n_i}\right). \tag{26}$$

The fitting parameters α and β are used to adjust the capacitance for the two physical factors. The β parameter adjusts the capacitance of a 3-D via since a smaller component of the capacitance is contributed by the portion of the 3-D via farthest from the ground plane. A decrease in the growth of the capacitance therefore occurs as the aspect ratio increases. The α term is used to adjust the capacitance based on the distance to the ground plane S_{gnd}. As S_{gnd} increases, the capacitance of the 3-D via decreases. The α and β terms are

$$\alpha = \left(-0.0351\frac{\mathfrak{L}}{D} + 1.5701\right) S_{\text{gnd}_{\mu\text{m}}}^{0.0111\frac{\mathfrak{L}}{D}-0.1997} \tag{27}$$

$$\beta = 5.8934 D_{\mu\text{m}}^{-0.553} \left(\frac{\mathfrak{L}}{D}\right)^{-(0.0031 D_{\mu\text{m}}+0.43)}. \tag{28}$$

A plot of the 3-D via capacitance for diameters of 20, 40, and 60 μm is shown in Fig. 8. The percent variation between simulation and the model is included in Appendix C as Table IX. The error of the capacitance produced by (24) does not exceed 8%.

In addition to a closed-form expression for the capacitance of a single 3-D via over a ground plane, an expression for the coupling capacitance between two 3-D vias over a ground plane is presented. The expression for the coupling capacitance between two 3-D vias is

$$C_c = 0.4\alpha\beta\gamma \cdot \frac{\epsilon_{\text{Si}}}{S}\pi D\mathfrak{L}. \tag{29}$$

The 0.4 multiplier in (29) adjusts the sheet capacitance between two TSVs when assuming that all electric field lines originating from half of the surface of one TSV terminate

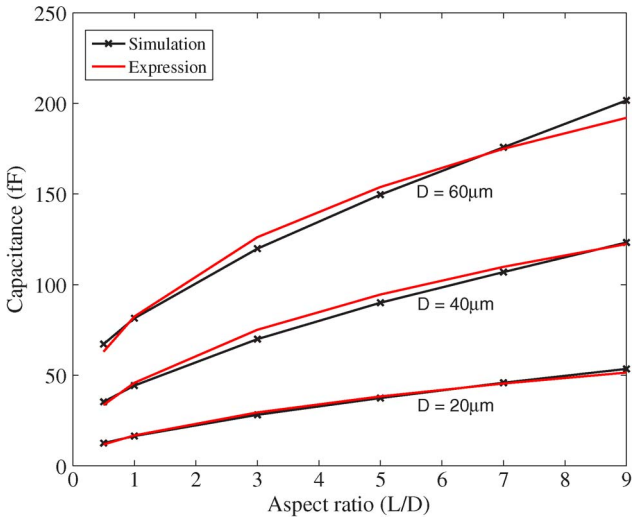

Fig. 8. Capacitance of a cylindrical 3-D via over a ground plane.

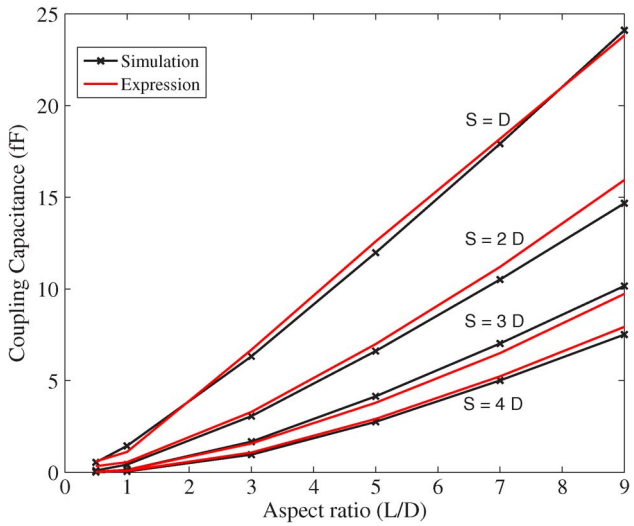

Fig. 9. Coupling capacitance between two 3-D vias over a ground plane ($D = 20\ \mu$m).

on the other TSV. Each fitting parameter (α, β, and γ) is used to adjust the coupling capacitance for a specific physical factor. The α term accounts for the nonlinearity of the coupling capacitance as a function of the aspect ratio $\mathfrak{L}/D$. The effect of the separation between the TSVs to the ground plane $S_{\rm gnd}$ on the coupling capacitance is included in β. Note that the β term is dependent on the aspect ratio of the TSV. Finally, the γ parameter accounts for the nonlinearity of the coupling capacitance as a function of the distance S between the two TSVs. The γ parameter is also dependent on the TSV aspect ratio. The pitch P, which is the sum of the distance between the two vias and a single TSV diameter ($P = S + D$), is also included in γ. The three terms are

$$\alpha = 0.225 \ln\left(0.97\frac{\mathfrak{L}}{D}\right) + 0.53 \tag{30}$$

$$\beta = 0.5711 \left(\frac{\mathfrak{L}}{D}\right)^{-0.988} \ln(S_{\mathrm{gnd}_{\mu\mathrm{m}}}) + \left(0.85 - e^{-\frac{\mathfrak{L}}{D}+1.3}\right) \tag{31}$$

$$\gamma = \begin{cases} 1, & \text{if } \frac{S}{D} \le 1 \quad (32) \\ \zeta\left[\ln\left(\frac{\mathfrak{L}}{D} + 4e^{-\frac{S_{\mu\mathrm{m}}}{9}} + 2.9\right) - 10.625 S_{\mu\mathrm{m}}^{-0.51}\right], & \text{if } \frac{S}{D} > 1 \quad (33) \end{cases}$$

where ζ includes the dependence on the ratio of the pitch to the diameter and is given by

$$\zeta = \left(1 + e^{-\left[\left(0.5 + \left|\frac{P}{D} - 4\right|\right)\frac{\mathfrak{L}}{D}\right]}\right). \tag{34}$$

A plot of the 3-D via coupling capacitance for diameters of 20, 40, and 60 μm is shown in Fig. 9. The percent variation between simulation and the model is described in Appendix D. The error of the capacitance produced by (29) does not exceed 15% for all aspect ratios greater than 1. When the aspect ratio is between 0.5 and 1, the error between the simulation and the closed-form expression is much larger once the coupling capacitance between the 3-D vias drops below 1.5 fF.

VI. Concluding Remarks

Closed-form expressions of the resistance, inductance, and capacitance of a 3-D via have revealed good agreement with full-wave electromagnetic simulation. Errors of less than 6% between the closed-form models and simulation have been demonstrated for both the resistance and inductance of a 3-D via. Errors of less than 8% for the capacitance have also been reported. The use of these closed-form expressions rather than full-wave electromagnetic simulations to estimate the 3-D via impedances enhances the system-level design process. These models of the via impedance are accurate over a wide range of diameters, lengths, dielectric thickness, and spacing.

Appendix A
Percent Variation in Resistance

The percent error between the closed-form expressions and the electromagnetic simulation for the DC and 1 and 2 GHz resistances are listed in Tables II–IV, respectively. None of the errors listed in Tables II–IV exceeds 5.5% for all investigated diameters and aspect ratios.

Appendix B
Percent Variation in Inductance

The percent error between the closed-form expressions and electromagnetic simulation for the self- (L_{11}) and mutual (L_{21}) inductances of a 3-D via for several diameters and aspect ratios are listed in Tables V and VI, respectively. The worst case DC and high frequency mutual inductance L_{21} between two non-equal length 3-D vias is listed in Tables VII and VIII, respectively. The error does not exceed 8% in all cases except for those cases where the spacing between the 3-D vias is at least four times the diameter. In these cases, the mutual inductance is sufficiently small that minor deviations between the expression and the simulation produce a large percent variation.

TABLE II
PERCENT ERROR BETWEEN SIMULATION AND CLOSED-FORM EXPRESSIONS OF A 3-D VIA, DC RESISTANCE

Diameter (μm)	Aspect ratio					
	0.5	1	3	5	7	9
1	-1.1	-1.1	-1.0	-1.0	-1.0	-1.0
5	-1.1	-1.1	-1.0	-1.0	-1.1	-0.9
10	-1.1	-1.0	-0.9	-0.9	-1.0	-0.9
20	-1.1	-0.9	-0.9	-0.7	-0.9	-0.9
40	-1.1	-1.1	-0.8	-0.9	-0.9	-0.9
60	-1.7	-0.9	-0.9	-0.9	-1.0	-0.9

TABLE III
PERCENT ERROR BETWEEN SIMULATION AND CLOSED-FORM EXPRESSIONS OF A 3-D VIA, 1 GHz RESISTANCE

Diameter (μm)	Aspect ratio					
	0.5	1	3	5	7	9
1	0.1	-0.1	0.04	0.1	-0.1	0.1
5	0.5	-0.1	-0.9	-0.4	0.2	0.7
10	0.9	-0.1	-0.2	0.8	0.8	1.9
20	1.4	-0.5	-3.3	-2.7	-1.7	-0.7
40	4.4	0.9	-2.7	-1.5	-0.1	1.9
60	2.3	-0.2	-2.7	0.04	1.4	4.1

TABLE IV
PERCENT ERROR BETWEEN SIMULATION AND CLOSED-FORM EXPRESSIONS OF A 3-D VIA, 2 GHz RESISTANCE

Diameter (μm)	Aspect ratio					
	0.5	1	3	5	7	9
1	0.6	0.2	0.4	0.5	0.2	0.5
5	1.0	0.2	-0.8	-0.3	0.5	1.2
10	1.4	0.2	-0.1	1.2	1.3	2.6
20	1.5	-0.4	-3.7	-3.1	-1.8	-0.7
40	5.2	1.0	-2.9	-1.6	0	2.2
60	2.7	-0.4	-2.9	0.1	1.5	4.4

TABLE V
PERCENT ERROR BETWEEN SIMULATION AND CLOSED-FORM EXPRESSIONS OF A 3-D VIA, SELF-INDUCTANCE (L_{11})

Diameter (μm)		Aspect ratio					
		0.5	1	3	5	7	9
1	DC	-1.6	0	0.9	0	0	0
	High f	3.6	-8.3	7.7	6.8	-1.6	0.5
5	DC	0	2.9	0.5	0.2	0.1	0
	High f	-6.7	-8.2	-0.2	-1.1	-1.9	-2.8
10	DC	-1.6	2.4	0.7	0.2	0.08	0.04
	High f	3.6	0.9	6.5	8.0	4.2	3.2
20	DC	0	2.7	0.7	0.2	0.1	0.04
	High f	3.6	1.8	2.8	1.8	0.9	0.3
40	DC	-0.4	2.8	0.6	0.2	0.1	0.04
	High f	2.7	-0.9	-0.6	-0.7	-2.1	-2.1
60	DC	-0.3	2.7	0.7	0.2	0.1	0.04
	High f	3.0	-1.2	-0.6	0.6	-1.7	-1.2

APPENDIX C
PERCENT VARIATION IN CAPACITANCE

The percent variation between the closed-form expression and electromagnetic simulation for the capacitance of a 3-D via over a ground plane is listed in Table IX. All errors listed in Table IX exhibit a deviation of less than 8% between the expressions and simulation.

TABLE VI
PERCENT ERROR BETWEEN SIMULATION AND CLOSED-FORM EXPRESSIONS OF A 3-D VIA, MUTUAL INDUCTANCE (L_{21})

Diameter (μm)	Pitch		Aspect ratio					
			0.5	1	3	5	7	9
1	$2{\cdot}D$	DC	-7.7	-2.0	0	0	0	-0.4
		High f	0	-6.5	0	1.3	4.1	0.9
5	$2{\cdot}D$	DC	-1.6	0	-0.5	-0.4	-0.2	-0.3
		High f	0	0	-3.8	-3.1	-1.2	0.9
10	$2{\cdot}D$	DC	-1.6	2.4	0.7	0.2	0.08	0.04
		High f	3.6	0.9	6.5	8.0	4.2	3.2
20	$2{\cdot}D$	DC	0	-1.0	-0.6	-0.5	-0.3	-0.3
		High f	0	0	-3.1	-2.5	0.3	1.8
	$3{\cdot}D$	DC	0	-1.5	-0.4	-0.2	-0.2	-0.2
		High f	0	-2.5	-4.1	-2.4	0.4	4.5
	$4{\cdot}D$	DC	-7.7	0	-0.2	-0.2	0	0.1
		High f	1.7	-3.3	-2.1	0.3	2.6	4.1
	$5{\cdot}D$	DC	0	0	-0.3	-0.1	-0.1	0.1
		High f	19.5	0	-4.3	-1.5	0.5	2.7
40	$2{\cdot}D$	DC	-2.0	-1.5	-0.7	-0.4	-0.3	-0.3
		High f	0	-0.9	-3.8	-1.4	-0.1	2.5
60	$2{\cdot}D$	DC	-1.3	-1.3	-0.7	-0.4	-0.3	-0.2
		High f	0	-1.7	-4.2	-2.6	-0.1	1.4

TABLE VII
PERCENT ERROR BETWEEN SIMULATION AND CLOSED-FORM EXPRESSIONS OF TWO 3-D VIAS WITH NON-EQUAL LENGTH DC MUTUAL INDUCTANCE (L_{21})

Diameter (μm)	$\frac{\mathfrak{L}_{via2}}{\mathfrak{L}_{via1}}$	Pitch	Aspect ratio					
			0.5	1	3	5	7	9
1	1	$2{\cdot}D$	-7.7	-2.0	0	0	0	-0.39
	2	$2{\cdot}D$	-4.0	-3.2	-2.4	-4.7	-4.0	-1.7
	3	$2{\cdot}D$	-5.6	-3.1	0	-1.7	-1.4	0.3
10	1	$2{\cdot}D$	-4.8	-2.0	-0.8	-0.4	-0.3	-0.2
	2	$2{\cdot}D$	-6.0	-3.2	-2.6	-4.5	-4.0	-1.6
	3	$2{\cdot}D$	-5.8	-3.1	0.4	-1.6	-1.6	0.2
	3	$4{\cdot}D$	5.4	1.4	-2.5	-4.2	-2.9	0.4
	3	$6{\cdot}D$	16.7	8.2	-1.8	-5.6	-4.1	-0.6
	3	$10{\cdot}D$	28.0	20	3.2	-3.7	-3.9	-1.4
40	1	$2{\cdot}D$	-2.0	-1.5	-0.7	-0.4	-0.3	-0.3
	2	$2{\cdot}D$	-5.1	-3.2	-2.5	-4.5	-4.0	-1.6
	3	$2{\cdot}D$	-6.3	-3.3	0.4	-1.6	-1.6	0.2

TABLE VIII
PERCENT ERROR BETWEEN SIMULATION AND CLOSED-FORM EXPRESSIONS OF TWO 3-D VIAS WITH NON-EQUAL LENGTH HIGH FREQUENCY MUTUAL INDUCTANCE (L_{21})

Diameter (μm)	$\frac{\mathfrak{L}_{via2}}{\mathfrak{L}_{via1}}$	Pitch	Aspect ratio					
			0.5	1	3	5	7	9
1	1	$2{\cdot}D$	0	-6.5	0	1.3	4.1	0.9
	2	$2{\cdot}D$	-7.1	-10.8	-0	-0.8	0.9	2.1
	3	$2{\cdot}D$	-5.0	-15.8	0	1.3	3.1	4.6
10	1	$2{\cdot}D$	0	0	0.3	3.0	4.1	5.7
	2	$2{\cdot}D$	0	-1.7	-3.2	-3.9	1.3	-2.3
	3	$2{\cdot}D$	-5.0	-10.1	-2.7	-2.2	-2.3	-0.8
	3	$4{\cdot}D$	1.9	-7.8	-2.5	3.0	-2.5	0.4
	3	$6{\cdot}D$	8.3	-2.9	-0.6	-6.7	-4.9	-2.1
	3	$10{\cdot}D$	20.5	9.5	0	-5.7	0.3	-2.6
40	1	$2{\cdot}D$	0	-0.9	-3.8	-1.4	-0.1	2.5
	2	$2{\cdot}D$	0	-6.1	-2.9	-2.2	-2.1	1.0
	3	$2{\cdot}D$	-9.8	-10.8	-1.4	-1.4	-0.2	1.3

APPENDIX D
PERCENT VARIATION IN COUPLING CAPACITANCE

The percent variation between the closed-form expression and electromagnetic simulation for the coupling capacitance between two 3-D vias over a ground plane is listed in Table X.

TABLE IX
PERCENT ERROR BETWEEN SIMULATION AND CLOSED-FORM EXPRESSIONS OF A 3-D VIA, CAPACITANCE

Diameter (μm)	Space to Gnd (μm)	Aspect ratio					
		0.5	1	3	5	7	9
20	10	-5.8	2.0	4.7	2.4	-1.0	-3.9
	30	2.4	-8.0	-5.9	-2.1	0.7	3.1
	50	6.1	-5.6	-4.4	-0.9	2.3	3.3
40	10	-4.9	3.4	7.4	5.1	2.7	-0.7
60	10	-6.2	1.2	5.3	2.8	-0.5	-4.7

TABLE X
PERCENT ERROR BETWEEN SIMULATION AND CLOSED-FORM EXPRESSIONS OF A 3-D VIA, COUPLING CAPACITANCE

Diameter (μm)	Space to Gnd (μm)	Space to Via (μm)	Aspect ratio					
			0.5	1	3	5	7	9
20	10	D	9.3	-22.9	5.7	5.1	1.5	-1.2
		$2{\cdot}D$	230	31.0	7.5	5.7	6.6	8.7
		$3{\cdot}D$	95	0	-6.0	-8.5	-7.4	-4.2
		$4{\cdot}D$	275	83.7	12.5	5.8	4.4	5.6
	30	D	-3.3	-16.2	4.3	4.6	1.4	-1.0
	50	D	-4.6	-14.5	3.4	3.7	0.9	-1.3
40	10	D	71	-10.1	2.3	-1.1	-3.4	-6.5
60	10	D	103	-5.9	1.4	-2.5	-5.8	-9.4

All errors listed in Table X exhibit a deviation of less than 15% between the expressions and simulation for all aspect ratios greater than 1.

REFERENCES

[1] V. F. Pavlidis and E. G. Friedman, "Interconnect-based design methodologies for three-dimensional integrated circuits," *Proc. IEEE*, vol. 97, no. 1, pp. 123–140, Jan. 2009.

[2] L. Xue, C. Liu, H.-S. Kim, S. Kim, and S. Tiwari, "Three-dimensional integration: Technology, use, and issues for mixed-signal applications," *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 601–608, Mar. 2003.

[3] W. R. Davis, J. Wilson, S. Mick, J. Xu, H. Hua, C. Mineo, A. M. Sule, M. Steer, and P. D. Franzon, "Demystifying 3D ICs: The pros and cons of going vertical," *IEEE Des. Test Comput.*, vol. 22, no. 6, pp. 498–510, Nov./Dec. 2005.

[4] V. F. Pavlidis and E. G. Friedman, *Three-Dimensional Integrated Circuit Design*. San Mateo, CA: Morgan Kaufmann, 2009.

[5] T. Sakurai and K. Tamaru, "Simple formulas for two- and three-dimensional capacitances," *IEEE Trans. Electron Devices*, vol. ED-30, no. 2, pp. 183–185, Feb. 1983.

[6] M. I. Elmasry, "Capacitance calculations in MOSFET VLSI," *IEEE Electron Device Lett.*, vol. EDL-3, no. 1, pp. 6–7, Jan. 1982.

[7] A. Ruehli, "Inductance calculations in a complex integrated circuit environment," *IBM J. Res. Develop.*, vol. 16, no. 5, pp. 470–481, Sep. 1972.

[8] A. Rahman, J. Trezza, B. New, and S. Trimberger, "Die stacking technology for terabit chip-to-chip communications," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2006, pp. 587–590.

[9] L. L. W. Leung and K. J. Chen, "Microwave characterization and modeling of high aspect ratio through-wafer interconnect vias in silicon substrates," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 8, pp. 2472–2480, Aug. 2005.

[10] F. M. Finkbeiner, C. Adams, E. Apodaca, J. A. Chervenak, J. Fischer, N. Doan, M. J. Li, C. K. Stahle, R. P. Brekosky, S. R. Bandler, E. Figueroa-Feliciano, M. A. Lindeman, R. L. Kelley, T. Saab, and D. J. Talley, "Development of ultra-low impedance through-wafer micro-vias," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 520, no. 1–3, pp. 463–465, Mar. 2004.

[11] E. M. Chow, V. Chandrasekaran, A. Partridge, T. Nishida, M. Sheplak, C. F. Quate, and T. W. Kenny, "Process compatible polysilicon-based electrical through-wafer interconnects in silicon substrates," *J. Microelectromech. Syst.*, vol. 11, no. 6, pp. 631–640, Dec. 2002.

[12] I. Luusua, K. Henttinen, P. Pekko, T. Vehmas, and H. Luoto, "Through-wafer polysilicon interconnect fabrication with in situ boron doping," in *Proc. Mater. Res. Soc. Symp.*, 2005, vol. 872, pp. 77–81.

[13] I. Savidis and E. G. Friedman, "Electrical modeling and characterization of 3-D vias," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2008, pp. 784–787.

[14] J. H. Wu, "Through-substrate interconnects for 3-D integration and RF systems," Ph.D. dissertation, MIT, Cambridge, MA, Oct. 2006.

[15] S. M. Alam, R. E. Jones, S. Rauf, and R. Chatterjee, "Inter-strata connection characteristics and signal transmission in three-dimensional (3D) integration technology," in *Proc. IEEE Int. Symp. Qual. Electron. Des.*, Mar. 2007, pp. 580–585.

[16] K. A. Jenkins and C. S. Patel, "Copper-filled through wafer vias with very low inductance," in *Proc. IEEE Int. Interconnect Technol. Conf.*, Jun. 2005, pp. 144–146.

[17] R. Weerasekera, D. Pamunuwa, M. Grange, H. Tenhunen, and L.-R. Zheng, "Closed-form equations for through-silicon via (TSV) parasitics in 3-D integrated circuits (ICs)," in *Proc. Workshop 3-D Integr., DATE Conf.*, Apr. 2009.

[18] A. Y. Weldezion, R. Weerasekera, D. Pamunuwa, L.-R. Zheng, and H. Tenhunen, "Bandwidth optimization for through-silicon-via (TSV) bundles in 3D integrated circuits," in *Proc. Workshop 3-D Integr., DATE Conf.*, Apr. 2009.

[19] R. Weerasekera, "System interconnection design trade-offs in three-dimensional integrated circuits," Ph.D. dissertation, KTH School Inform. Commun. Technol., Stockholm, Sweden, Dec. 2008.

[20] *Ansoft Quick 3-D*. [Online]. Available: http://www.ansoft.com/products/si/q3d_extractor/

[21] D. L. Logan, *A First Course in the Finite Element Method*, 4th ed. Phoenix, AZ: Nelson Eng., 2007.

[22] A. R. Hall, *Generalized Method of Moments*. New York: Oxford Univ. Press, 2005.

[23] E. K. Miller, L. Medgyesi-Mitschang, and E. H. Newman, Eds., *Computational Electromagnetics: Frequency-Domain Method of Moments*. New York: IEEE Press, 1992.

[24] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed. New York: Cambridge Univ. Press, 2004.

[25] E. B. Rosa, "The self and mutual inductances of linear conductors," *Bull. Bur. Standards*, vol. 4, no. 2, pp. 301–344, 1908.

[26] Y. I. Ismail and E. G. Friedman, "On the extraction of on-chip inductance," *J. Circuits Syst. Comput.*, vol. 12, no. 1, pp. 31–40, Feb. 2003.

[27] D. E. Khali, Y. I. Ismail, M. Khellah, T. Karnik, and V. De, "Analytical model for the propagation delay of through silicon vias," in *Proc. IEEE Int. Symp. Qual. Electron. Des.*, Mar. 2008, pp. 553–556.

Ioannis Savidis received the B.S.E. degree in electrical and computer engineering and biomedical engineering from Duke University, Durham, NC, in 2005. He received the M.Sc. degree in electrical and computer engineering from the University of Rochester, Rochester, NY, in 2007, and is currently working toward the Ph.D. degree in electrical and computer engineering under the guidance of Professor E. G. Friedman.

He interned at Freescale Semiconductor Corporation, Austin, TX, during the summers of 2006 and 2007, where he worked on the electrical characterization and modeling of interplane 3-D vias. During the summers of 2008 and 2009, he interned at IBM's T. J. Watson Research Center, Yorktown Heights, NY, where he worked on electrical characterization and modeling, reticle design, and DC and high frequency electrical measurements of test vehicles implementing various interplane 3-D via topologies. His research interests include analysis, modeling, and design methodologies for high performance digital and mixed-signal integrated circuits, with an emphasis on electrical and thermal modeling and characterization, signal and power integrity, and power and clock delivery for 3-D stacking technologies.

Eby G. Friedman (F'00) received the B.S. degree in electrical engineering from Lafayette College, Lafayette, PA, in 1979, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Irvine, in 1981 and 1989, respectively.

From 1979 to 1991, he was with Hughes Aircraft Company, rising to the position of manager of the Signal Processing Design and Test Department and responsible for the design and test of high performance digital and analog ICs. He has been with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY, since 1991, where he is a Distinguished Professor and the Director of the High Performance Very Large Scale Integration/IC Design and Analysis Laboratory. He is also a Visiting Professor at the Technion—Israel Institute of Technology, Haifa, Israel. He is the author of about 350 papers and book chapters and numerous patents and the author or editor of eleven books in the fields of high speed and low power CMOS design techniques, high speed interconnect, and the theory and application of synchronous clock and power distribution networks. He is the Regional Editor of the *Journal of Circuits, Systems and Computers* and a member of the Editorial Boards of the *Analog Integrated Circuits and Signal Processing*, the *Microelectronics Journal*, the *Journal of Low Power Electronics*, and the *Journal of Signal Processing Systems*. His current research and teaching interests are in high performance synchronous digital and mixed-signal microelectronic design and analysis with application to high speed portable processors and low power wireless communications.

Dr. Friedman is a Senior Fulbright Fellow. He is the Chair of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATED (VLSI) SYSTEMS Steering Committee and a member of the technical program committees of a number of conferences. Previously, he was the Editor in Chief of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATED (VLSI) SYSTEMS, a member of the Editorial Board of the PROCEEDINGS OF THE IEEE and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: ANALOG AND DIGITAL SIGNAL PROCESSING, a member of the CAS Society Board of Governors, the Program and Technical Chair of several IEEE conferences, and a recipient of the University of Rochester Graduate Teaching Award and a College of Engineering Teaching Excellence Award.