Synaptic Characteristics of Ag/AgInSbTe/Ta-Based Memristor for Pattern Recognition Applications

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***Abstract*— The memristor, a promising candidate for synaptic interconnections in artificial neural network, has gained significant attention for application to neuromorphic systems. One common method is using two memristors as one synapse to represent the positive and negative weights. In this paper, the synaptic behavior of a Ag/AgInSbTe/Ta (AIST)-based memristor is experimentally demonstrated. In addition, a neural architecture using one AIST memristor as a synapse is proposed, where both the plus and minus weights of the neural synapses are realized in a single memristive array. Moreover, the memristor-based neural network is extended to a multilayer architecture, and modified memristor-based backpropagation learning rules are implemented on-chip to achieve pattern recognition. The effects of device variations and input noise on the performance of a memristor-based multilayer neural network (MNN) are also described. The proposed MNN is capable of pattern recognition with high success rates and exhibits several advantages, such as good accuracy, high robustness, and noise immunity.**

***Index Terms*— Crossbar array, memristor, multilayer neural networks (MNNs), pattern recognition, synaptic weight.**

I. Introduction

THE traditional Von Neumann computer architecture has become increasingly insuficient to satisfy the demand for high-performance computing. Alternative methods are therefore desired for high-performance memory, logic, and neuromorphic computing systems [1]–[3]. One of the most promising candidates is the memristor, the discovery of which has further broadened the scope of hybrid CMOS architectures to nonconventional architectures [4], such as threshold logic [5] and neuromorphic systems [6]. Memristors are particularly appealing for realizing synaptic weights in artificial neural networks [7]–[12] for the following reasons. First, memristors are a simple two-terminal structure, supporting high density crossbar arrays. Second, the device conductance, which represents the synaptic weight, can be changed by simple positive and negative voltage pulses.

One common method to achieve the positive and negative weights is utilizing two memristors as one synapse for pattern recognition [13]–[17]. More complex memristor-based multilayer neural networks (MNNs) with online gradient descent training have been realized by using a single memristor and two CMOS transistors (2T1M) per synapse [18]. A simpler memristor-based crossbar array architecture is described in [19], where both plus-polarity and minus-polarity connection matrices are realized by a single memristor-based crossbar array.

In this paper, the synaptic behavior of Ag/AgInSbTe/Ta (AIST)-based memristive devices is experimentally demonstrated. Reproducible gradual resistance tuning as an electronic synapse is shown in our previous study [20]. The resistance is precisely tuned by regulating the polarity, amplitude, width, and number of applied voltage pulses [21], [22]. In addition, a memristor-based neural network is extended to multilayers using one memristor as a synapse with a modified memristor-based backpropagation (BP) learning rule implemented on-chip. The effects of conductance variations cannot, however, be accurately controlled by adjusting the synaptic weight. Random variations in the conductance are therefore added to the adjustment process of the synaptic weights.

II. Experiment

Ag (100 nm)/AgInSbTe (25 nm)/Ta (100 nm) stacked capacitorlike memristors have been fabricated and characterized. An image of the devices from a scanning electron microscope (SEM) is shown in Fig. 1(a). The contact areas of the devices are $100 \times 100\ \mu m^2$, $200 \times 200\ \mu m^2$, and $300 \times 300\ \mu m^2$. In this system, positive and negative voltages are applied to change the conductance of the memristive device, as shown in Fig. 1(b). The positive bias is from the top Ta electrode to the bottom Ag electrode.

The current–voltage (I–V) characteristics of a $100 \times 100\ \mu m^2$ device is shown in Fig. 1(c). The pinched hysteresis loop exhibits a memristor fingerprint, and no electroforming process is needed to induce resistive switching. During a

Manuscript received December 5, 2016; revised February 8, 2017; accepted February 13, 2017. Date of publication March 1, 2017; date of current version March 22, 2017. This work was supported by the National Natural Science Foundation of China under Grant 61374150 and Grant 61376130. The review of this paper was arranged by Editor G.-H. Koh. *(Corresponding authors: Yi Li; Xiaoping Wang.)*

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Digital Object Identifier 10.1109/TED.2017.2671433

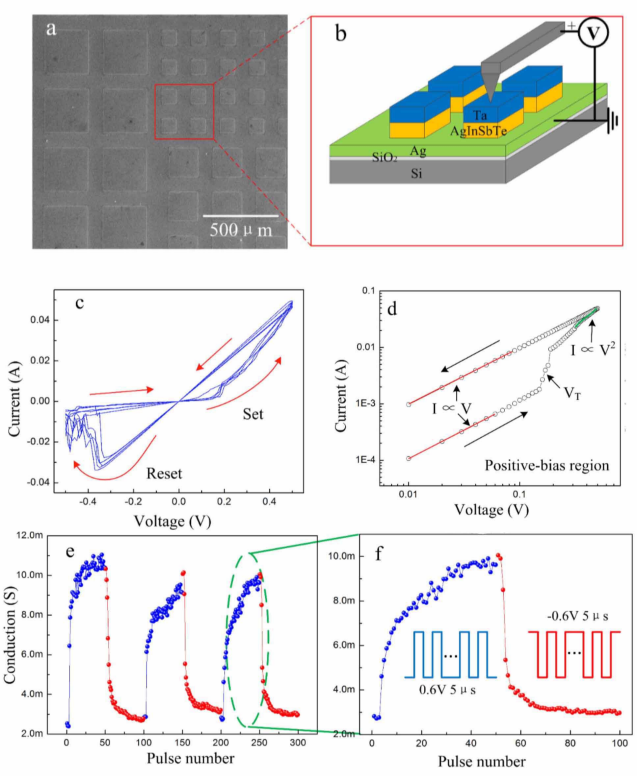

Fig. 1. Memristive behavior of Ag/AgInSbTe/Ta memristor. (a) Top SEM view of the Ag (100 nm)/AgInSbTe (25 nm)/Ta (100 nm) stacked capacitorlike devices with various contact areas deposited on the Si/SiO_2 Substrate. (b) Scheme of the devices and measurement setup. (c) Bipolar resistive switching I–V characteristics. (d) Double logarithmic plots of I–V curves in the positive bias region, indicating an SCLC mechanism. (e) Repetitive gradual device conductance modulation under pulse stimulation. (f) Experimental evolution of the conductance under the stimulus of 50 positive pulses (0.6 V, 5 μs) and 50 negative pulses (-0.6 V, 5 μs).

linear direct current (dc) voltage sweep, a relatively small SET voltage at approximately 0.19 V drives the memristor to a low-resistance state from a high-resistance state, whereas a RESET voltage of approximately -0.37 V switches the device to the high-resistance state. The logarithmic I–V characteristics of the positive region is shown in Fig. 1(d), which exhibits an ohmic behavior (with a slope of approximately 1) in the low-voltage region, followed by a rapid nonlinear increase in current in the high-voltage region. Several switching mechanisms have been proposed, such as space charge-limited conduction (SCLC), electrochemical metallization, and valence change mechanism. This phenomenon indicates that the memristive behavior could be characterized by the SCLC mechanism [20], [21], [23]. In the low-voltage region of 0–0.19 V, the thermally generated carriers exceed the injected carriers, resulting in a linear I–V behavior. At the threshold voltage (V_T) of the memristor, the increased injected carriers are absorbed as charge traps originating from the distorted structure of the amorphous AgInSbTe. When the traps are filled by injected carriers, an abrupt increase in the current occurs. When the space charge accumulates in the material, a field is established that hinders further injection, and the slope reduces to 2, consistent with the Mott–Gurney law ($I \propto V^2$) [24]. In contrast, a negative bias releases the carriers, and the device returns to the high-resistance state.

The gradual conductance tuning property under positive or negative voltage pulses has also been examined, as shown in Fig. 1(e) and (f). Due to the application of ten consecutive periods of 50 positive pulses (0.6 V, 5 μs) and 50 negative pulses (-0.6 V, 5 μs), the device conductance can be continuously increased or decreased, representing the potentiation or depression of the memristive synapse. The upper and lower limit of the conductance is, respectively, 2.4 and 11.1 mS, although cycle-to-cycle variations exist. This characteristic can be utilized in electronic synapses for synaptic weight adjustment. This gradual change in conductance may result from homogenous charge trapping and detrapping processes rather than a localized filamentary conduction mechanism.

Three layers of the stacked devices have been prepared by dc magnetron sputtering (JZCK-640S) at room temperature. The bottom 100-nm Ag electrode is deposited on a Si/SiO_2 (1 μm) substrate. The pattern of the upper 25-nm AgInSbTe and 100-nm Ta layers is formed by photolithography (Karl Suss MJB3), followed by a sequential AgInSbTe/Ta deposition and lift-off process. During AgInSbTe film deposition, the sputtering power and argon pressure are maintained, respectively, at 30 W and 0.5 Pa. An SEM image of the memristors is from a Nova NanoSEM 450. Electrical characterization is performed using a probe station (Cascade S300) equipped with a semiconductor characterization system (Keithley 4200-SCS) under a dc voltage sweep mode and pulse mode. During electrical measurements, the positive bias is the current flowing from the Ta electrode to the bottom Ag electrode. All measurements are performed at room temperature in air.

III. Application to Neural Networks

A. Memristor-Based Multilayer Neural Networks

A CMOS analog transmission gate (TG) is used as a switch, as shown in Fig. 2(a). When $C = 0$ and $\overline{C} = V_{DD}$, the TG turns OFF. Alternatively, when $C = V_{DD}$ and $\overline{C} = 0$, the TG turns on [see Fig. 2(b)]. A neural network structure using a crossbar array of memristors controlled by TGs is adopted, as shown in Fig. 2(c), where the M input channels are connected to the rows and the N output channels are connected in the first layer to the columns of the memristor crossbar network. The second layer supports the N input channels and P output channels.

The network is trained on black white images of size 3×5 pixels, as shown in Fig. 3(a) and (c). For example, the input voltages of image 3 are [111; 001; 010; 001; 111] and the target outputs are [0; 0; 1; 1] ("1" represents V_H). Pattern recognition for eight digit numbers [see Fig. 3(c)] is simulated on a two layer network of 15 inputs $\times$7 hiddens $\times$4 outputs, as shown in Fig. 3(b). The corresponding outputs of numbers 0 to 7 are (0, 0, 0, 0) to (0, 1, 1, 1) [see Fig. 3(d)].

To change the weight of the memristor-based neural network, $V_{DD}/2$ and $V_{DD}/3$ write schemes [25] can be used. However, due to the proposed circuits and threshold voltage of the AgInSbTe memristor, the conventional $V_{DD}/2$ or $V_{DD}/3$ write scheme cannot satisfy the weight updating process. The

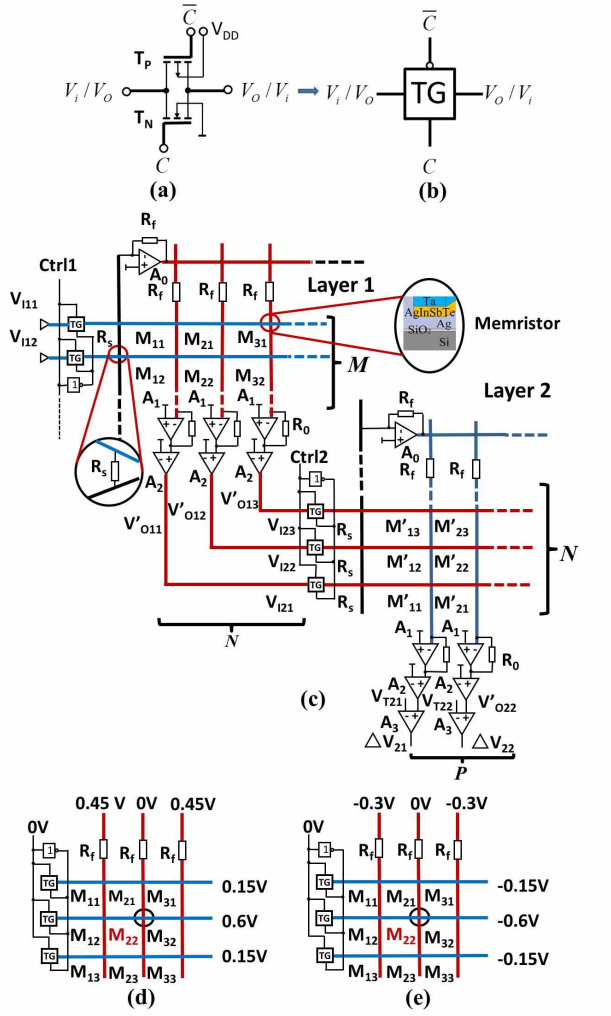

Fig. 2. Memristor-based MNN. (a) Structure of CMOS TG. (b) Symbol for CMOS TG. (c) Proposed memristor-based MNN. (d) Voltages for conductance of M_{22} increasing. (e) Conductance of M_{22} decreasing.

relative protection voltages are therefore determined, and the weight change method is shown in Fig. 2(d) and (e). Different grid crossbar sizes have been tested, and a 3×3 crossbar array is considered as an example. Only memristor M_{22} is assumed to change and the other memristors remain unchanged. The voltages in the process of conductance change are shown in Fig. 2(d) and (e).

Assume that a learning system operates on K discrete iterations of inputs, indexed by $k = 1, 2, \ldots, K$. During each iteration k, the system receives a pair of two vectors of size M and N: inputs $\mathbf{V_I}^{(k)} \in \mathbb{R}^M$ and outputs $\mathbf{V_O}^{(k)} \in \mathbb{R}^N$.

For example, assume that $\mathbf{W}$ is an adjustable $N \times M$ matrix, and consider the estimator [18]

$$\mathbf{V_O}^{(k)} = \mathbf{W}^{(k)} \mathbf{V_I}^{(k)} \tag{1}$$

or

$$V_{Oj}^{(k)} = \sum_{i=1}^{M} W_{ji}^{(k)} V_{Ii}^{(k)} \tag{2}$$

where $i = 1, 2, \ldots, M$ and $j = 1, 2, \ldots, N$.

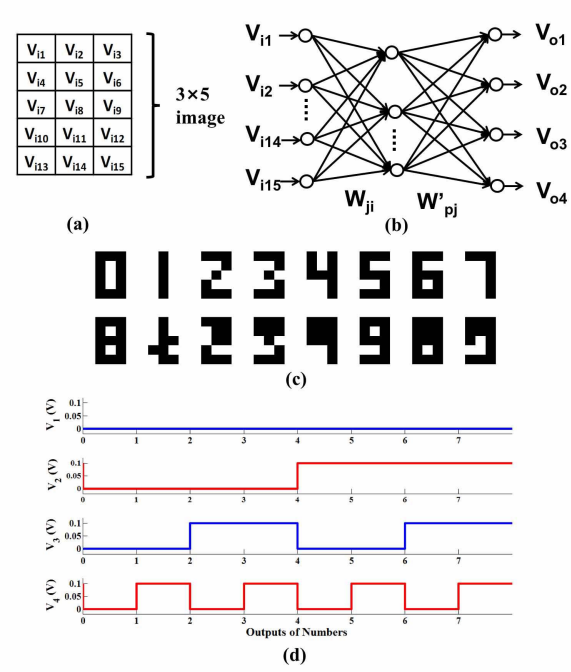

Fig. 3. Memristor-based MNN for pattern recognition of eight-digit numbers (0-7). (a) 3×5 input image. (b) MNN for classification of 3×5 binary images. (c) Ideal input images and noisy images with 15% random pixels. (d) Output of numbers 0–7 are (0, 0, 0, 0) to (0, 1, 1, 1).

A synaptic array circuit composed of a single crossbar array of $M^-(G_{ji})$ and a constant-term circuit of G_s are shown in Fig. 2(c). Here, G_s $(= 1/R_s)$ is the conductance of R_s, and G_{ji} $(=1/R_{ji})$ is the memristor conductance at the crossing point between the ith row and jth column. V_{Ii} is the input voltage applied to the ith row. According to Kirchhoff's voltage law, the synaptic weight is

$$W_{ji} = R_0 \times (G_s - G_{ji}). \tag{3}$$

The comparator enables V'_{Oj} as

$$V'_{Oj} = f(V_{Oj}) = \begin{cases} V_H & \text{if } V_{Oj} > 0 \\ V_{\mathrm{L}} & \text{if } V_{Oj} \le 0 \end{cases} \tag{4}$$

where V_H and V_{L} $(V_{\mathrm{L}} = 0)$ are, respectively, the high and low voltage of the comparator. The *output* of the estimator $\mathbf{V_O} = \mathbf{W}\mathbf{V_I}$ predicts the *target* output $\mathbf{V_T}$ for new unseen *inputs* $\mathbf{V_I}$. To solve this problem, the synapse *weights* $\mathbf{W}$ are updated to minimize the error between the outputs and target outputs over a K_0-long subset of the training set $(k = 1, 2, \ldots, K_0)$. The error vector is

$$\Delta \mathbf{V}^{(k)} = \mathbf{V_T}^{(k)} - \mathbf{V'_O}^{(k)}. \tag{5}$$

The final error E_e is

$$E_e = \sqrt{\frac{1}{K_0} \sum_{k=1}^{K_0} \| \Delta \mathbf{V}^{(k)} \|^2}. \tag{6}$$

A modified BP learning rule is applied to reduce the error E_e to zero.

TABLE I
FITTING PARAMETERS TO PRACTICAL MEMRISTIVE DEVICES

Parameters of Synaptic Model [26]	*AIST-based memristor*
$R_{\mathrm{ON}}(\Omega)$	10
$R_{\mathrm{OFF}}(\Omega)$	420
V_{T-} (V)	-0.19
V_{T+} (V)	0.37
D (nm)	3
μ_v ($\mathrm{m^2 s^{-1} \Omega^{-1}}$)	1.6e-12
i_{on} (A)	1
i_{off} (A)	1e-5
i_0 (A)	1e-3

B. Effects of Device Variations

To obtain a desirable change in the memristor conductance, a voltage of appropriate magnitude and polarity for a suitable duration (pulse number) is applied across the memristor. The memristance of the AIST-based memristive device can be described by the synaptic model [26]

$$R(t) = R_{\mathrm{ON}}\frac{w(t)}{D} + R_{\mathrm{OFF}}\left(1 - \frac{w(t)}{D}\right) \tag{7}$$

where $w(t)$ is the width of the doped region, D is the thickness, R_{OFF} and R_{ON} are, respectively, the internal high and low memristances. The derivative of the width is

$$\frac{dw(t)}{dt} = \begin{cases} \mu_v \dfrac{R_{\mathrm{ON}}}{D}\dfrac{i_{\mathrm{OFF}}}{i(t) - i_0} f(w(t)), & v(t) > V_{T+} > 0 \\ 0, & V_{T-} \le v(t) \le V_{T+} \\ \mu_v \dfrac{R_{\mathrm{ON}}}{D}\dfrac{i(t)}{i_{\mathrm{ON}}} f(w(t)), & v(t) < V_{T-} < 0 \end{cases} \tag{8}$$

where i_0, i_{OFF}, and i_{ON} are constants, μ_v denotes the average ion mobility, and V_{T+} and V_{T-} are, respectively, positive and negative threshold voltages. The parameters of the AIST-based memristor are listed in Table I.

However, due to cycle-to-cycle variations of practical devices, the change in each step cannot be accurately controlled. To verify the effects of device variations on network performance, the relevant device parameters are assumed to follow a Gaussian distribution. The exact value of a parameter for a given device is randomly chosen using a Monte Carlo method during the simulation process [27]. The abrupt changes of the practical devices reduce the successful recognition rate of complex functions. Another method is using the stochastic memristive model in neuromorphic system design [28]. In this paper, the synaptic model mentioned previously is built to evaluate the effect of abrupt changes of the conductance. Moreover, considering the effects of device variations, the weight (conductance) is not precisely adjusted. During each step, more than one pulse may be applied to update the weight. The effect of random noise on the conductance during each step is also compared, as shown in Fig. 4(a). The different random noise rates are 0%, 5%, 10%, and 15% for four different tests. The corresponding cycle numbers are, respectively, 31, 55, 64, and 70. Changes in the corresponding output voltages during the first ten cycles and final ten cycles are, respectively, shown in Fig. 5(a) and (b). Based on measurement data,

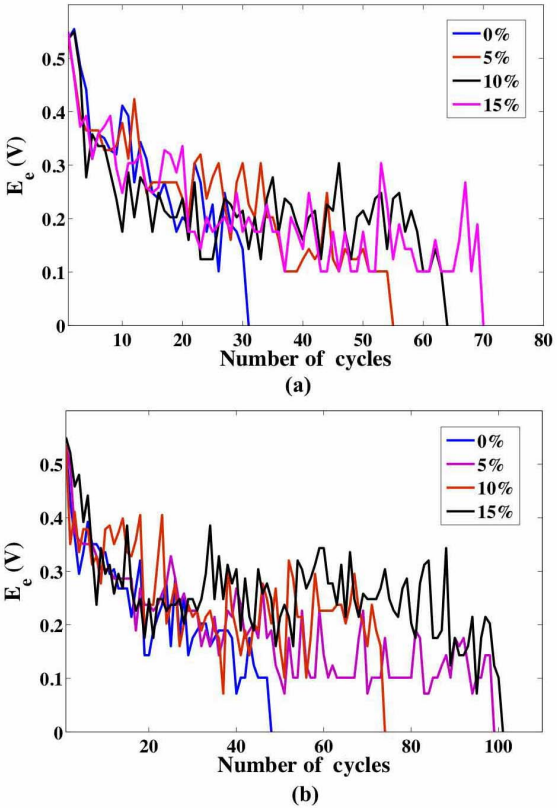

Fig. 4. Training error in each cycle for pattern recognition in an MNN assuming device variations and noisy images. (a) Number of cycles of random noise of the conductance adjusted for each step. (b) Number of cycles of different noise levels for the noisy input images.

the level of noise for successful recognition is 14.91%. The proposed memristor-based MNN is verified to be inherently tolerant to device variations.

The results of training errors during each cycle for the correct recognition patterns in a memristor-based MNN for six different runs are illustrated in Fig. 6(a). The learning rate η is 0.05 for six different tests (from Run 1 to Run 6), and the corresponding cycle numbers are, respectively, 52, 43, 48, 52, 37, and 63 [see Fig. 6(a)]. Additionally, the results of training errors during each cycle for the correct pattern recognitions at different learning rates are shown in Fig. 6(b). The learning rate $\eta = 0.05, 0.01, 0.03, 0.06, 0.02$, and 0.008 for six different runs, and the corresponding cycle numbers are, respectively, 58, 187, 62, 39, 100, and 868. If the learning rate is excessively high ($\eta = 0.07$), the weights are updated too fast and can overshoot the optimal value. Alternatively, if the learning rate is too small ($\eta = 0.005$), the weights are updated too slow and may not be able to overcome a local minima [27]. When $\eta \le 0.005$ or $\eta \ge 0.07$, the error cannot converge to 0 within 2000 cycles, suggesting that the learning rate needs to be properly chosen ($\eta = 0.05$) to balance between the learning speed and the accuracy.

When pattern recognition is operated on-chip, the input voltages are assumed to be affected by a different amount of random noise. The inputs are changed from 0 to V_H to evaluate the robustness of the circuit. Noisy images are acquired by randomly flipping 15% of the pixels as black in the character

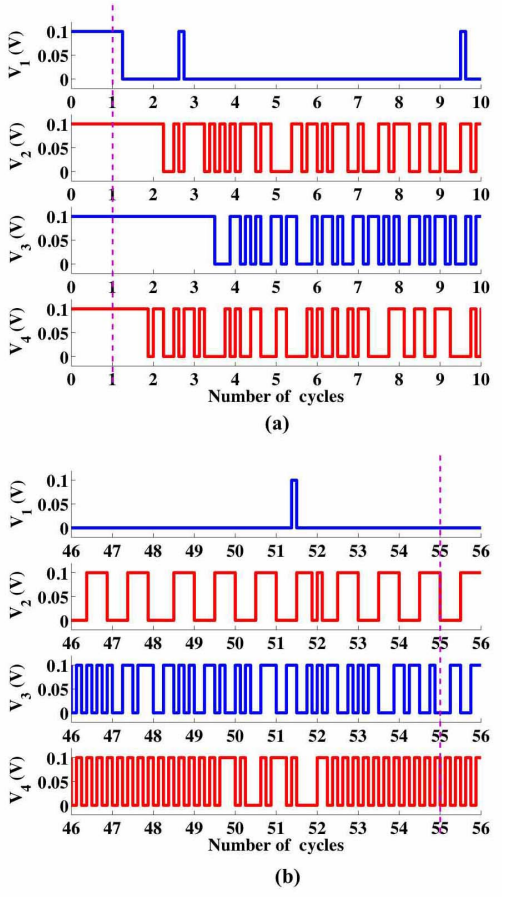

Fig. 5. Change in output voltages during each cycle. (a) Change in the outputs (V'_{O21}, V'_{O22}, V'_{O23}, and V'_{O24}) during the first ten cycles, and (b) change in the outputs (V'_{O21}, V'_{O22}, V'_{O23}, and V'_{O24}) during the last ten cycles.

images, as shown in Fig. 3(d). The different noise levels for the input noisy images are compared, as shown in Fig. 4(b). The different noise levels are 0%, 5%, 10%, and 15% for four different runs, and the corresponding cycle numbers are 48, 99, 74, and 101. The proposed memristor-based MNN, therefore, exhibits the advantages of good accuracy, high robustness, and noise immunity.

C. Energy Reducing Method and Comparion

AIST-based memristors have been fabricated in neural networks as synapses. The proposed memristive neural network has been extended to multilayers. The MNN can be effectively described as a modified on-chip BP learning rule and trained to perform eight digit number recognition. Although the energy consumption of the AIST-based memristors is relatively high, several methods exist to reduce the energy, such as scaling the cell size to nanometers [29], controlling the conductive filament formation/disruption process [30], and inserting an additional insulating layer [31]. The proposed memristor-based synaptic crossbar circuit requires fewer memristors as compared with PCMO-based memristive synaptic circuits [13], [14], [17] and metal–oxide memristive synaptic circuits [15], [16], since the synapse can be realized by a single memristor. The control circuits within the peripheral

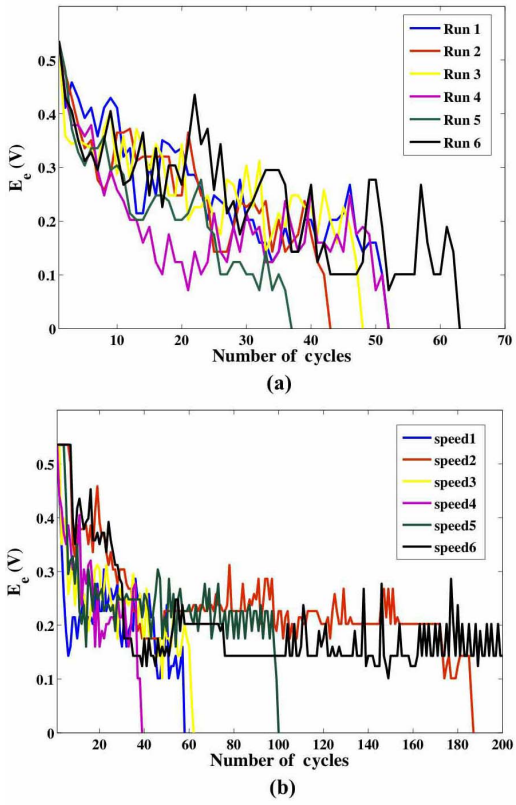

Fig. 6. Training error in each cycle for pattern recognition in an MNN for six different runs. (a) $\eta = 0.05$ for six different runs, and (b) different rates, $\eta = 0.05, 0.01, 0.03, 0.06, 0.02$, and 0.008.

circuits of the proposed neural network are therefore simpler than using two memristors as one synapse. Moreover, a memristor-based neural network has also been extended to multilayers, and a modified BP learning rule is applied to achieve on-chip pattern recognition. After learning the principal input images, the memristor-based MNN successfully classifies the different digit numbers. Another highlight of this paper is that successful learning and classification are obtained in the memristor-based MNN despite the presence of device variations, demonstrating the reliability of the MNN architecture and the proposed learning algorithm.

IV. Conclusion

The proposed AIST memristor is verified to behave as a synapse within a neural architecture, where both the plus and minus weights of the neural synapses are realized in a single memristor array. Moreover, the extended MNN exhibits several advantages, such as good accuracy, high robustness, and noise immunity, which is verified by simulation. The ability to reliably achieve on-chip learning and perform classification tasks in the presence of unreliable devices is also demonstrated. This approach can be extended to larger MNNs and other learning algorithms to achieve more complex tasks.

Acknowledgment

The authors would like to thank the facility support of the Center for Nanoscale Characterization and Devices of WNLO.

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