Stability of Distributed Power Delivery Systems With Multiple Parallel On-Chip LDO Regulators

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***Abstract*—High quality power delivery for high performance integrated circuits is a significant design challenge. To provide high quality power, the on-chip power needs to be regulated with ultra-small locally distributed power efficient converters. While the quality of the power supply can be efficiently addressed with distributed on-chip power supplies, the stability of these parallel connected voltage regulators is a primary concern. A passivity-based stability criterion is proposed for maintaining a stable power delivery system composed of multiple regulators. To evaluate the proposed approach, a fully integrated power delivery system with distributed on-chip low-dropout (LDO) regulators has been fabricated in a 28 nm CMOS process. The experimental results of a distributed power delivery system composed of six on-chip LDO regulators satisfy this stability criterion, yielding a stable system response within −25°C to 125°C, 10% voltage variations, and 50% to 200% load sharing variations. The system is believed to be one of the first successful silicon demonstrations of stable parallel analog LDO regulators.**

***Index Terms*—Distributed power delivery, low-dropout (LDO), on-chip voltage regulators, stability.**

I. Introduction

DELIVERING high quality power to support power efficient systems is a fundamental requirement of all integrated circuits (ICs) [1]. While the quality of the power supply can be efficiently addressed with a point-of-load (POL) power delivery system [2]–[6], the complexity of a dynamically controllable distributed POL power supply system is a significant design issue. Hundreds of on-chip power regulators need to be co-designed with billions of nonlinear current loads within a power domain, imposing a critical stability challenge on a distributed power delivery system.

With the increasing diversity of modern systems, dynamic voltage scaling and fine grain power management are becoming increasingly common. These modern heterogeneous systems are partitioned into a fine grain structure and the power is individually delivered and dynamically managed within each domain. With dynamic voltage scaling, maintaining the stability of distributed power delivery systems has become even more challenging.

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Low-dropout (LDO) regulators suitable for on-chip integration have recently been proposed [7]–[17], exhibiting fast load regulation, high power efficiency, as well as stability over a wide range of current loads and process, voltage, and temperature (PVT) variations. The LDO is, therefore, a key component in on-chip power management. A distributed system with multiple LDO regulators delivering power to a single grid may, however, exhibit degraded stability due to complex interactions among the LDO regulators, power distribution network, and current loads. To provide a stable distributed power delivery system, a stability analysis criterion is necessary.

The stability of a single closed loop system is traditionally determined by the phase margin (PM) of the open loop response. In systems with multiple dependent loops, the open loop approach is, however, not practical since no straightforward method exists to identify unstable loops. A computer-aided design (CAD) framework based on the passivity and gain of a power grid has recently been proposed for evaluating the stability of distributed power delivery systems with LDO regulators [18], [19]. While recognition of the stability challenge is an important cornerstone to the distributed power grid design process, the accuracy and efficiency of the approach requires demonstration on practical power delivery systems. In this paper, an alternative passivity-based stability criterion (PBSC) is proposed to use with existing CAD tools and design flows, and is not limited to LDO based power delivery systems.

A distributed power delivery system based on the proposed stability criterion has been fabricated in an advanced 28 nm CMOS technology, and exhibits stable voltage regulation over a wide range of temperature, voltage, and load sharing conditions. The power delivery system with six ultra-small LDO regulators features an adaptive current boost bias and an adaptive RC compensation network controlled individually within each LDO regulator, increasing the power efficiency and stability of the overall system over a wide range of load currents and PVT variations. The distributed power delivery system has been tested under a wide range of PVT variations, yielding a stable loop response and 99.49% current efficiency.

The rest of the paper is organized as follows. The stability criterion is introduced in Section II. A power delivery system for evaluating the proposed stability criterion with six fully integrated LDO regulators, adaptive current boost bias, and RC compensation networks is described and evaluated based on the proposed stability criterion in Section III. Simulation results exhibit strong correlation between the stability of a distributed power delivery system and the proposed PBSC criterion. Experimental results for a distributed power delivery system with six on-chip LDOs are presented in Section IV. The paper is concluded in Section V.

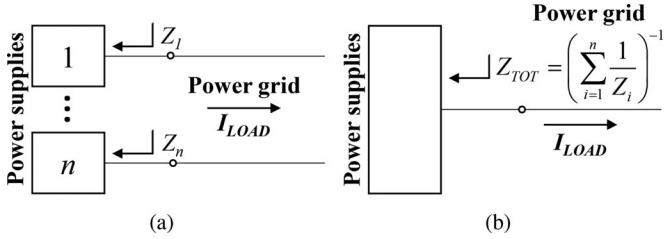

Fig. 1. Power delivery system (a) with $n \geq 2$ distributed power supplies, and (b) reduced single port network.

II. Passivity-Based Stability of Distributed Power Delivery Systems

Understanding the effects of the frequency domain parameters on the time-domain characteristics provides significant insight into the analysis and transient behavior of complex systems [20]–[24]. Traditionally, the phase margin of the open loop transfer function determines the stability of a single LDO regulator. Similarly, a straightforward criterion is required for determining the stability of a distributed power delivery system.

A distributed power delivery system with $n \geq 2$ power supplies driving a single power grid is depicted in Fig. 1(a). In this distributed system, the power supplies can be combined into a single power delivery system, yielding an equivalent single port network, as shown in Fig. 1(b). Note that the output impedance of the equivalent single port network, Z_{TOT} in Fig. 1(b), is the parallel combination of all of the output impedances $Z_i, i = 1, \ldots, N$ of the individual power supplies shown in Fig. 1(a). The output impedance of a distributed power delivery system is, therefore, straightforward to evaluate based on the individual output impedance of the parallel connected components. Alternatively, there is no straightforward method to identify the single loop that causes instability within a system with multiple interacting feedback paths. The open loop transfer function, traditionally used to determine the stability of a lumped power delivery system, cannot be applied to a distributed power delivery system with multiple control loops [25]. A criterion for evaluating the stability of a multi-feedback path system composed of distributed power regulators is, therefore, needed.

Sufficient conditions for a stable distributed power delivery system are described in this section. These conditions are based on the observation, proven in [26], that a linear, time invariant (LTI) system is stable when coupled to an arbitrary passive environment if and only if the driving point impedance is a passive system. Thus, a distributed power delivery system is stable if and only if the equivalent output impedance Z_{TOT} satisfies passivity requirements. The passivity of an LTI system is described here in terms of frequency domain parameters.

An LTI system is passive if the system can only absorb energy, yielding, in mathematical terms [27]

$$\int_{-\infty}^{T} v(t)i(t)dt \geq 0, \forall\, T \tag{1}$$

where $v(t)$ and $i(t)$ are, respectively, the voltage across the system and current flowing through the system. The total energy

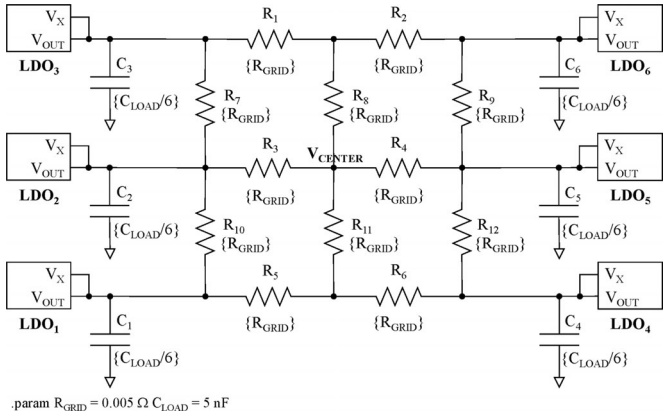

Fig. 2. Model of distributed LDO and power distribution network.

delivered to a passive system is determined from (1) based on the Parseval Theorem, exhibiting, for all positive currents

$$\frac{1}{\pi}\int_{0}^{+\infty} Re[Z(j\omega)]|I(j\omega)|^2 d\omega \geq 0 \tag{2}$$

where $Z(s) = V(s)/I(s)$ is the system impedance, and $V(s)$ and $I(s)$ are, respectively, the phasor voltage and current of the system. The passivity condition based on (2), $\{Re[Z(\sigma + j\omega)] \geq 0, \forall \sigma > 0\}$, can be simplified based on [28] and specialized for a particular frequency range of interest *S*, yielding the following sufficient conditions for passivity of an LTI system: $Z(s)$ has no right-half plane (RHP) poles, and the phase of $Z(s)$ is within the $(-90^\circ, +90^\circ)$ range $\forall\, s \in S$.

A distributed system is, therefore, exponentially stable (converges within an exponential envelope) if the impedance of the system satisfies these passivity requirements, marginally stable (oscillates with constant amplitude) if the voltage and current phasors are shifted by precisely 90°, and unstable otherwise. The phase of the output impedance is an efficient alternative to determine the stability of these distributed systems, since the traditional phase margin approach is not practical due to the multiple control loops.

III. Power Delivery System

A power delivery system with six fully integrated LDO regulators is described in this section. The system converts 1.0 V into 0.7 V, supplying up to 788 mA to the load. A model of the power delivery system with six LDO regulators and a distributed power delivery network is shown in Fig. 2. The accuracy of the power grid model with n lumped sections, rise time t_r, inductance L, and capacitance C is verified with the $n \geq 5\sqrt{LC}/t_r$ rule of thumb (see [29]), exhibiting less than 2.5% error in the characteristic impedance for $n = 1$. A single current load is considered to account for the worst case load characteristics with the maximum current step and fastest load transition.

Current sharing is a primary concern in a distributed power delivery system. Each LDO contributes differently to the voltage regulation of a power network based on the position of the active current loads and the level of consumed current. Load

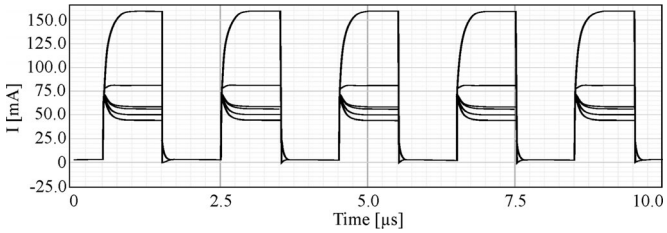

Fig. 3. Load sharing in distributed power delivery system.

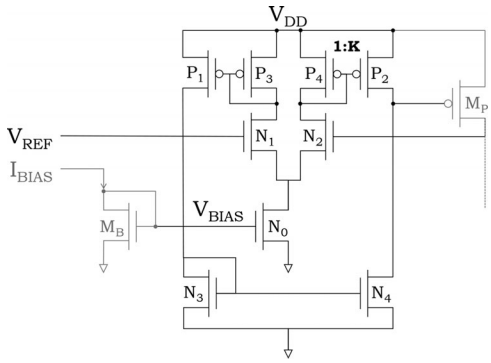

Fig. 4. Three current mirror OTA.

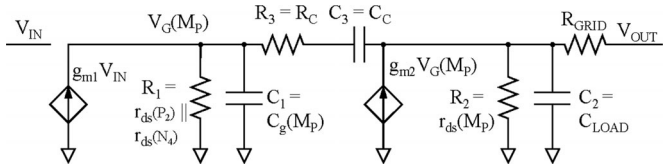

Fig. 5. Small signal linear model of LDO.

sharing among the LDO regulators is illustrated in Fig. 3 with a single current load (at the upper right corner of the power network) switching between 18 mA and 450 mA. The LDO at the upper right corner (see Fig. 2) is located in close proximity with the current load and supplies the largest portion (up to 160 mA) of the total current requirements, which is higher by a factor of two than the average current load supplied by a single LDO. Alternatively, the remote LDO at the bottom left corner supplies significantly less current (up to 40 mA), only half of the average LDO load current. In the specific configuration, the LDO in the upper right corner regulates voltage under larger load current steps and exhibits enhanced stability characteristics. In modern high performance circuits, the load map may change significantly over time [30] and under PVT variations. Mechanisms are, therefore, required to co-design the distributed on-chip regulators to dynamically stabilize the power delivery system over time. Adaptive mechanisms are described in this paper that respond to load variations at the output of each of the LDO regulators, increasing the power efficiency of the system and enhancing the performance and stability. The stability of the system is evaluated based on the proposed passivity-based criterion.

An adaptive current boost bias and an adaptive RC compensation network are included within each LDO to, respectively, enhance the slew rate with low power overhead, and stabilize the power regulation over a wide range of load currents and PVT variations. The operation of the dynamic mechanisms is controlled within the individual LDO regulators, providing fine grain regulation of the output voltage. Alternatively, both mechanisms within each LDO are adaptively triggered by the same sensing circuit, exhibiting a more compact power delivery system. The components of the power delivery system are described in Sections III-A, III-B, III-C, and III-D. The stability of the overall system is analyzed in Section III-E.

A. Op Amp-Based LDO

The open loop output resistance, load capacitance, and control loop gain and bandwidth are important criteria when developing a fast LDO. To address these challenging transient requirements, a three current mirror operational transconductance amplifier (OTA) topology [14] is used within each LDO, as shown in Fig. 4. A linear model that considers the effects of the open loop output resistance, load capacitance, and control loop gain and bandwidth is used to model the behavior of the three current mirror OTA. Miller compensation is used to achieve a dominant pole. This model is shown in Fig. 5. The open loop gain of the LDO regulator is

$$A(s) = \frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{-(g_{m1}R_1)\cdot(g_{m2}R_2)(1+N\cdot s)}{1+D_1\cdot s+D_2\cdot s^2+D_3\cdot s^3} \tag{3}$$

where

$$N = \left(R_3 - \frac{1}{g_{m2}}\right)C_3, \tag{4}$$

$$D_1 = R_1C_1 + R_2C_2 + R_3C_3 + R_1C_3 + R_2C_3(1+g_{m2}R_1), \tag{5}$$

$$D_2 = R_1R_2C_1C_2 + R_1C_1R_3C_3 + R_2C_2R_3C_3 + R_1R_2(C_1+C_2)C_3, \tag{6}$$

$$D_3 = R_1C_1R_2C_2R_3C_3. \tag{7}$$

The zero of the LDO regulator is formed by the compensation network at the frequency $f(z) \approx 1/2\pi(R_3C_3)$. The dominant pole frequency $f(p_1)$ is assumed to be significantly lower than the frequency of the other poles, $f(p_2)$ and $f(p_3)$ ($f(p_1) << f(p_2), f(p_3)$). All of the poles are assumed to be real and approximated over a feasible range of g_{mi}, R_i, and C_i components, yielding, $f(p_1) \approx 1/2\pi(g_{m2}R_2)(R_1C_3)$, $f(p_2) \approx g_{m2}2\pi C_2$, and $f(p_3) \approx 1/2\pi R_3C_1$. The DC gain and closed loop bandwidth of the LDO regulator $A_0 = (g_{m1}R_1g_{m2}R_2)$ is listed in Table I. An average gain of 57 dB is listed with less than 10% variations over a wide range of process, temperature, and load variations. A minimum bandwidth of 50 MHz is listed at the slow process corner under a light load of 1 mA.

To analyze the stability and compensation of a single LDO regulator, the small signal transconductance and drain source resistance of the output device are assumed to be, respectively, $g_{m2} \propto \sqrt{I_{\text{Load}}}$ and $R_2 \propto 1/I_{\text{Load}}$. Other parameters are assumed

TABLE I
DC GAIN AND CLOSED LOOP BANDWIDTH OVER A RANGE OF LOAD CURRENTS AT SLOW (SS, −30°C), TYPICAL (TT, 25°C), AND FAST (FF, 105°C) CORNERS

Corner	I_{Load} [mA]	DC gain [dB]	BW [MHz]
Slow	70, 20, 1	58.7, 60.4, 61.2	129.5, 86.0, 50.3
Typical	100, 25, 3	56.7, 58.4, 57.2	136.9, 98.7, 86.2
Fast	150, 100, 70	51.2, 53.4, 54.4	146.7, 144.6, 134.4

to be approximately independent of the load current within the region of interest. Under these assumptions, the frequency of the first and second poles increases with $\sqrt{I_{\text{Load}}}$, while the zero frequency $f(z)$ and third pole frequency $f(p_3)$ are approximately constant under load current variations. The value of R_C is chosen to ensure that the frequency of the third pole $f(p_3)$ is larger than the unity gain frequency in the region of interest, yielding a second-order system to enhance stability.

To increase stability over a wide range of load capacitance, the dominant pole is determined by the compensation capacitor, yielding $f(p_1) < f(p_2)$ and, therefore

$$C_C > \frac{C_2}{g_{m2} R_2 R_1} > 3 \text{ pF}. \tag{8}$$

The maximum phase margin is achieved when the second pole is canceled by the zero, yielding a first-order system under the following constraint on the compensation network:

$$R_C = \frac{C_2}{g_{m2} C_C} < 3 \text{ k}\Omega. \tag{9}$$

Finally, the first-order system exhibits a unity gain at $f_t \approx A_0 \cdot f(p_1) = g_{m1}/2\pi C_C < 130$ MHz, fulfilling the requirement $f_t < f(p_3)$ under the constraints (8) and (9)

$$R_C < \frac{C_C}{g_{m1} C_1} < 2 \text{ k}\Omega. \tag{10}$$

Under the constraints, (8), (9), and (10), the LDO regulator is a first-order system with a phase margin between 45° and 90° (the PM is reduced over three decades by 90° due to p_1 and a portion of 45° due to p_3).

The transconductance of the output device g_{m2} increases, however, with $\sqrt{I_{\text{Load}}}$. Thus, under current load variations, the second pole is shifted from the zero frequency, violating the first-order assumption, and degrading the stability of the LDO regulator. The behavior of the PM is, therefore, primarily determined by the variation of the frequency of the second pole, as shown in Fig. 6, linearly decreasing with a larger $|\log(f(p_2)/f(z))|$ ratio

$$PM(f(z)) - PM(f(p_2)) \propto \left| \log\left(\frac{g_{m2} R_C C_C}{C_{\text{Load}}} \right) \right|. \tag{11}$$

Note the high accuracy of this approximation ($R^2 = 0.9511$).

To maximize the stability of an LDO regulator over a range of load currents, the compensation should be modified with changing transconductance g_{m2}, maintaining $g_{m2} R_C C_C / C_{\text{Load}} \to 1$. The preferable phase margin is shown in Fig. 7 with two different compensation resistors, $R_C = 0.7$ kΩ and $R_C = 1.7$ kΩ, and a compensation capacitor of $C_C = 8.5$ pF for a range of low load

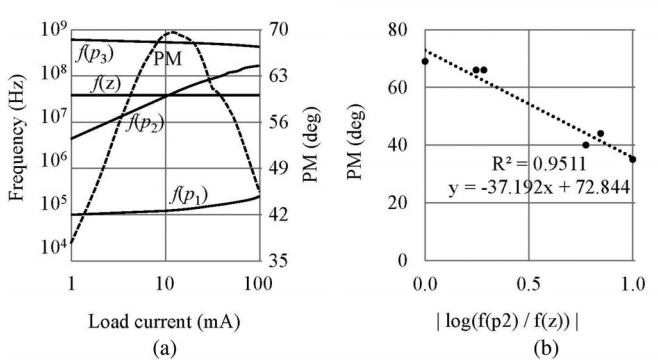

Fig. 6. Stability of the LDO regulator as a function of (a) load current I_{Load}, and (b) compensation accuracy.

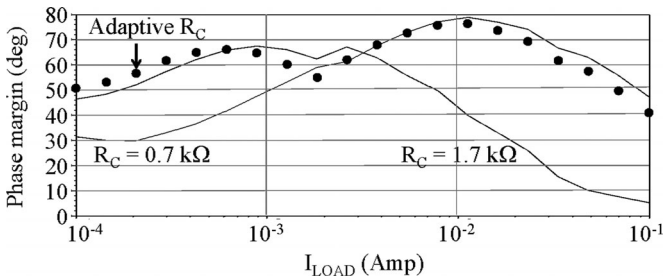

Fig. 7. PM with different constant compensation resistors and adaptive compensation.

currents. At low currents of $I_{\text{Load}} < 3$ mA, compensation with a larger resistor ($R_C = 1.7$ kΩ) results in a higher phase margin. At higher currents of $I_{\text{Load}} > 3$ mA, a lower compensation resistance ($RC = 0.7$ kΩ) is preferable. Ultimately, the compensation network is adaptively modified with the load current, increasing the phase margin over a wide range of load and PVT variations, as described in Section III-D.

The speed of a three current mirror OTA topology is limited by the bias current that flows into the input differential pair. To produce fast transitions at the load, a higher bias current is preferable. Alternatively, to lower power losses, the OTA should operate under low bias currents. To enhance the loop response while dissipating less power, an adaptive bias is employed within the power delivery system, as described in Section III-C.

B. Current Sensor

A current sensor is used to adaptively control the bias current through the differential pair and RC compensation of the system. The sensor mirrors a portion of the load current, and compares the mirrored current with a threshold current. When the output current is below a threshold current, adaptive mechanisms are activated through the Boost signal, as shown in Fig. 8. Hysteresis is employed to prevent the comparator from oscillating at the threshold current. The transient and DC response of the Boost signal is shown in Fig. 9. The threshold current is determined by the width of the transistor N_{P0} (see Fig. 8), and is an important design parameter. The system is configured to activate and deactivate the Boost mode at, respectively, $I_{\text{LOAD}} = 3.8$ μA and

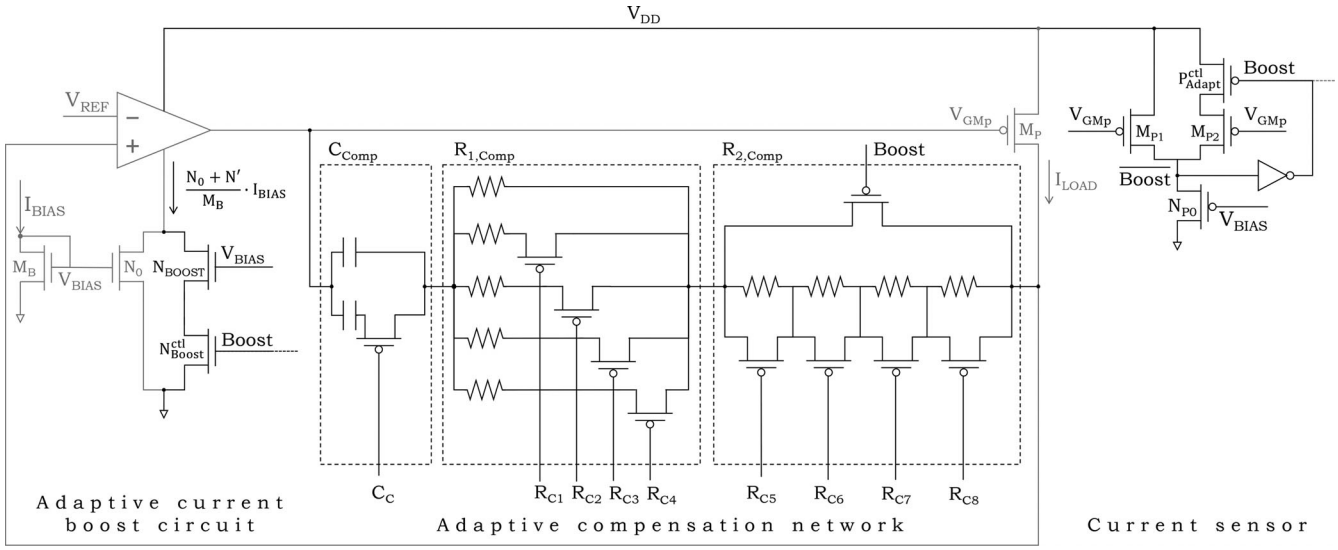

Fig. 8. Adaptive bias boost and compensation networks.

$I_{\rm LOAD} = 1.8\ \mu$A (see Fig. 9), enhancing the performance (voltage droop, slew rate, and current efficiency) and stability of the system, as described, respectively, in Sections III-C, and III-D.

C. Adaptive Bias

A self-adaptive bias current mechanism is described in this section that temporarily boosts the bias current to mitigate fast fluctuations while lowering power losses. The current boost circuit is composed of a sensor block that follows the output voltage at the drain of transistor $M_{\rm P}$, and a current boost block that controls the current through the differential pair, as shown in Fig. 8. The current boost transistor $N_{\rm Boost}$ is connected in parallel with the bias transistor N_0, and controlled by the Boost line. During the boost mode of operation (the Boost voltage is high), the current into the differential pair is raised, increasing the slew rate of the LDO. Alternatively, during regular mode (the Boost voltage is low), transistor $N_{\rm Boost}$ is off and no additional current flows into the differential pair, enhancing the power efficiency of the LDO. The Boost line is controlled by the sensor block, and is activated when the load current drops below a threshold current of 3.8 mA, exhibiting faster regulation and a lower voltage droop at the output of the LDO. To prevent oscillations at the threshold current, a hysteretic mechanism is used. The Boost line is, therefore, deactivated when the load current increases above 1.8 mA, improving the power efficiency of the LDO.

To evaluate the performance of the adaptive biasing technique, the load current is switched in 10 ns from 3 mA to 100 mA. The voltage droop $\Delta V_{\rm OUT}$ and quiescent current I_Q are recorded for three different adaptive modes. In the first mode, the current boost mechanism is disabled, limiting the bias current through the differential pair to $(N_0/M_B)I_{\rm BIAS}$. In the second mode, the Boost line is maintained at a high voltage, boosting the current through the differential pair at a constant rate to $((N_0 + N')/M_B)I_{\rm BIAS}$. In the third mode, the Boost line is adaptively boosted in real time by the sensor block, exhibiting a bias current between $(N_0/M_B)I_{\rm BIAS}$ and $((N_0 + N')/M_B)I_{\rm BIAS}$ through the differential pair. Simulation results for each of the modes are shown in Fig. 10.

Due to enhanced biasing, the voltage droop is decreased by 35% (from 43 mV to 25 mV) at the expense of a significant increase of 137% in current consumption. The bias current is adaptively enhanced under light loads, exhibiting an 18.6% decrease in voltage droop while avoiding excessive power loss over time.

A power delivery system in modern high performance circuits draws significant leakage current from the power regulators. Minimum load currents of 1 mA, 3 mA, and 70 mA are assumed for a single LDO regulator for, respectively, the slow, typical, and fast corners. Quiescent current simulations for different load currents are listed in Table II with and without adaptive biasing.

Without adaptive biasing, an average quiescent current of 423 μA with less than 2% variations is demonstrated at 25°C for all load currents. This current is increased to 1 mA by adaptively biasing at light loads at the slow, typical, and fast corners.

D. Adaptive Compensation Network

The large gate capacitance of the pass transistor together with the wide range of possible values of $C_{\rm Load}$ produce a complicated system transfer function of poles and zeros. The low frequency non-dominant poles within the unity gain frequency of the feedback loop create a negative phase shift, degrading the stability of the overall system. To compensate for the negative phase shift, the Miller compensation technique [17] is used. The wide range in load capacitance and currents and significant PVT variations, however, make compensation with fixed RC values impractical in nanoscale technologies. A digitally configurable compensation network is, therefore, used that adaptively modifies the dominant pole, maintaining system stability for all values of $C_{\rm Load}$ and $I_{\rm Load}$. Due to complex interactions among the parallel connected LDO regulators, shared power grid, and current loads, this compensation network is necessary to maintain

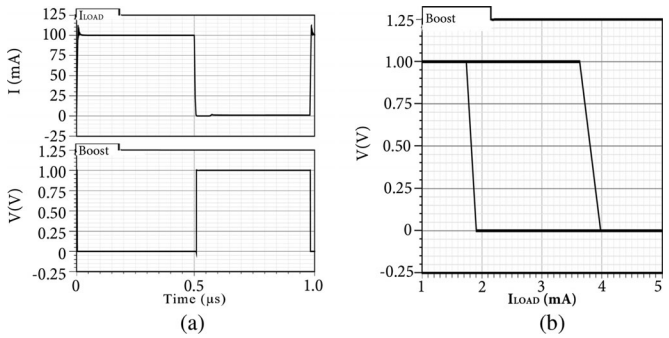

Fig. 9. Load current tracking through the boost signal, (a) transient response, and (b) DC response.

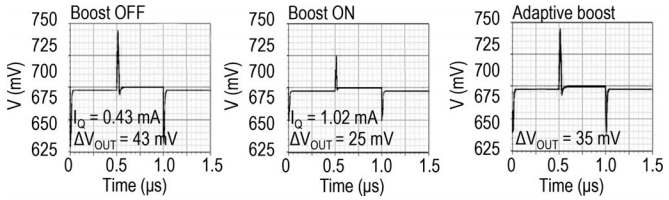

Fig. 10. Voltage droop and quiescent current with and without adaptive biasing at typical corner (TT, 25°C).

TABLE II
QUIESCENT CURRENT WITH AND WITHOUT ADAPTIVE BIASING

	−30°C		25°C		125°C	
I_{Load} [mA]	Adapt. I_Q [mA]	Const. I_Q [mA]	Adapt. I_Q [mA]	Const. I_Q [mA]	Adapt. I_Q [mA]	Const. I_Q [mA]
0.5	0.841	0.347	1.001	0.416	1.223	0.524
2.0	0.353	0.353	0.433	0.433	1.258	0.538
100	0.353	0.353	0.424	0.424	0.543	0.543

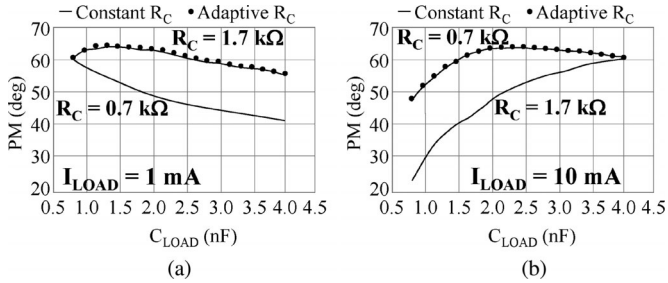

Fig. 11. Phase margin with different compensation and load capacitance for (a) $I_{\text{Load}} = 1$ mA, and (b) $I_{\text{Load}} = 10$ mA.

stability in distributed power delivery systems. Conventional LDO regulators without the compensation network can easily become unstable from device mismatch, offset voltage, and varying load current when connected in parallel [18], [19], [31]–[34]. The compensation network is comprised of a capacitive block connected in series with two resistive blocks, as shown in Fig. 8. The capacitive (C_{Comp}) and resistive ($R_{1,\text{Comp}}$ and $R_{2,\text{Comp}}$) blocks are digitally controlled by, respectively, control signals C_{C} and RC_{i}, i = 1, ..., 8. These RC impedances are digitally configured within each of the LDO regulators after fabrication to compensate for process variations. The second resistive block is also controlled by the Boost signal, which is adaptively activated (bypassed) by the current load sensor within each LDO regulator when the individual Boost signal is high (low), compensating for voltage, temperature, and current load variations in run time. During the high-to-low current load transition, the output impedance increases. Thus, the pole introduced by the load is pushed to a lower frequency, degrading the stability of the LDO. Alternatively, the Boost signal is activated during this transition, increasing the compensation impedance, $(R_{1,\text{Comp}} + R_{2,\text{Comp}}) \cdot C_{\text{Comp}}$, to maintain a stable response. At other times, the Boost signal is deactivated, and the LDO is stabilized with $R_{1,\text{Comp}} \cdot C_{\text{Comp}}$.

To illustrate the effect of the compensation on the LDO performance, the phase margin of a single LDO is presented in Fig. 11 over a range of C_{Load} values for two load currents, $I_{\text{Load}} = 1$ mA and $I_{\text{Load}} = 10$ mA. For a light load current of 1 mA, the phase margin increases with higher compensation resistance, PM($R_C = 1.7$ kΩ) > PM($R_C = 0.7$ kΩ). Alternatively, for a higher load current of 10 mA, a smaller compensation resistor is preferable. The adaptive compensation illustrated in Fig. 11 exhibits a higher phase margin as compared to nonadjustable compensation. The same behavior can be observed in Fig. 7, where the compensation network is adaptively reconfigured as a function of the load current, yielding the largest PM as compared to nonadjustable compensation networks.

E. Passivity Analysis of a Distributed Power Delivery System

Based on typical load current variations, as shown in Fig. 3, the distributed power delivery system can exhibit significant current sharing variations (between 50% and 200% for an individual LDO regulator). To address worst case current sharing variations and a wide range of PVT variations, each LDO regulator is optimally compensated around $I_{\text{Load}} = 10$ mA with $R_C C_C = 700\ \Omega \cdot 6$ pF to provide a stable response with $40^\circ < PM < 70^\circ$ for high load currents of $10\ \text{mA} < I_{\text{Load}} < 160\ \text{mA}$. Alternatively, at low load currents, the compensation is adaptively increased, enhancing the stability of the system. Due to the distributive nature of the power delivery system, adaptive compensation and bias are activated individually within each LDO regulator based on locally sensed load currents, providing fine grain control over the local adaptive mechanisms. The same load sensing circuit within each LDO regulator triggers both the adaptive compensation and bias mechanisms, saving area.

The output impedance of parallel connected voltage regulators is a primary factor in determining the stability of a distributed power delivery system, and is a strong function of the poles and zeros of the individual LDO regulators. To maintain a stable distributed system, the effect of load current variations on the relative location of the poles and zeros in the distributed system needs to be determined. A distributed power delivery system that addresses the issue of load sharing variations is shown in Fig. 12. The small signal model shown in Fig. 5

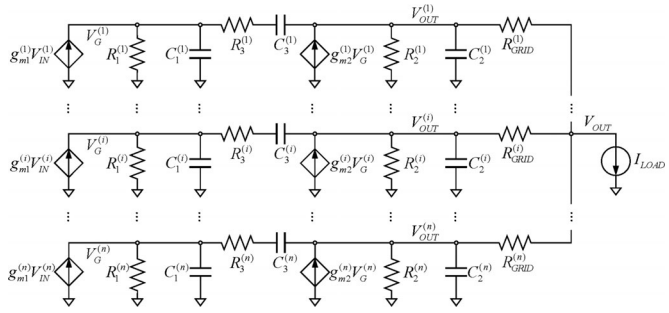

Fig. 12. Distributed power delivery system with n LDO regulators driving a common power grid.

is assumed for each individual LDO regulator. Capacitors $C_2^{(i)}$, $i = 1, \ldots, n$ in Fig. 12 are equivalent to capacitors C_i, $i = 1, \ldots, n$ in Fig. 2 for $n = 6$. The total load current I_{LOAD} in the model is distributed based on the individual power grid resistors, $R_{\text{GRID}}^{(i)}, i = 1, \ldots, n$. Each of the resistors $R_{\text{GRID}}^{(i)}$ represents the equivalent output resistance as seen by the ith, LDO regulator, as depicted in Fig. 2. The load variations can be efficiently evaluated by modifying the value of these parallel connected output resistors. The output impedance accounts for both the power grid and current load of the desired system. The LDO system is, therefore, designed for a specific rather than an arbitrary load.

The stability of the power delivery system is evaluated based on the proposed passivity-based criterion. The output impedance of the system under this load sharing scenario is evaluated for each of the LDO regulators and the overall distributed power delivery system. To demonstrate the effect of the phase of the output impedance on the stability of a distributed system, the transient response and phase of the output impedance $\angle Z_{\text{OUT}}$ of the distributed system with six LDO regulators is shown in Fig. 13. In agreement with the PBSC, the output response diverges (oscillates with increasing amplitude), and converges within an exponential envelope for, respectively, $|\angle Z_{\text{OUT}}| > 90^\circ$ and $|\angle Z_{\text{OUT}}| < 90^\circ$. Note that the system with $C_C = 0.5$ pF and $\max_{\forall f}\{\angle Z_{\text{OUT}}\} = 89^\circ$ slowly converges to the steady-state solution, exhibiting an underdamped response inappropriate for voltage regulation in power delivery systems. Alternatively, a system with $C_C = 5$ pF and $\max_{\forall f}\{\angle Z_{\text{OUT}}\} = 70^\circ$ exhibits an overdamped response with a significant stability margin. A strong correlation therefore exists between the phase shift of the output voltage and load current, and the effective stability margin of the system. Based on this observation, the phase margin of the output impedance for a distributed power delivery system is

$$PM(Z_{\text{out}}) = 90^\circ - \max_{\forall f}\{\angle Z_{\text{OUT}}\}. \tag{12}$$

A distributed power delivery system is, therefore, unstable, stable, or marginally stable if the phase margin of the output impedance is, respectively, negative, positive, or zero. A safe phase margin of the output impedance should be determined based on specific design criteria to avoid excessively underdamped and overdamped voltage regulation systems.

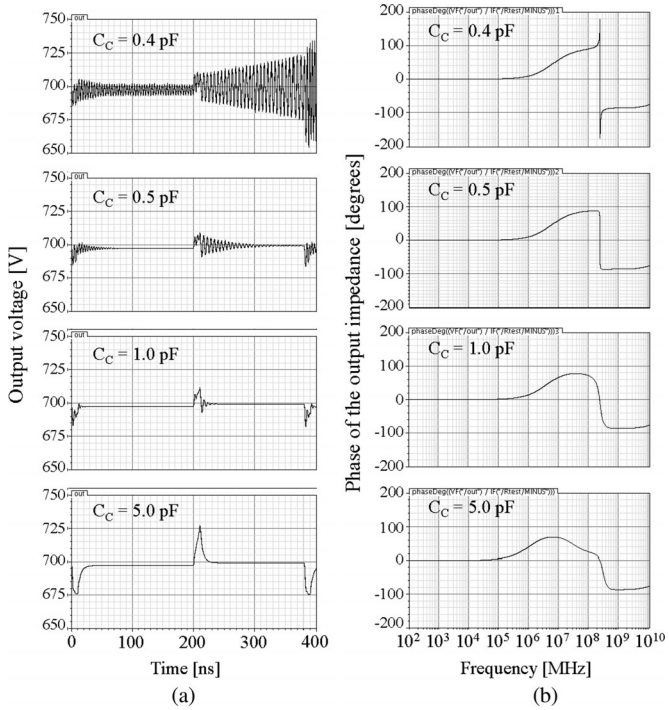

Fig. 13. Output response of a distributed power delivery system with different compensation ($C_C = 0.4$pF, $C_C = 0.5$pF, $C_C = 1$pF, and $C_C = 5$pF), showing the correlation between the (a) transient response, and (b) phase of the output impedance.

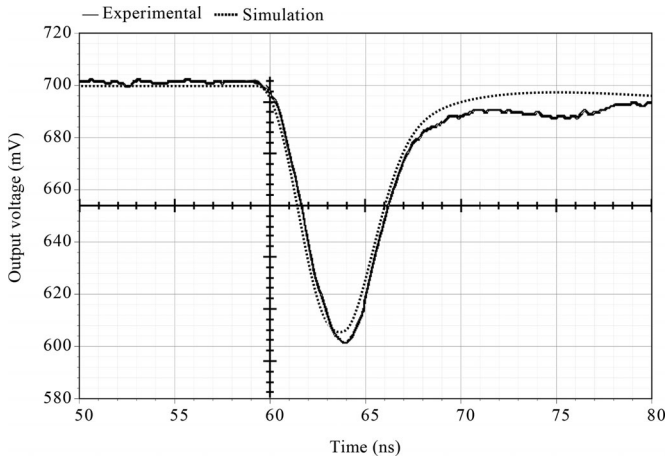

Fig. 14. Measured and simulated transient response for a load current step from 52 mA to 788 mA in 5 ns.

IV. Experimental Results

A power delivery system with six LDO regulators has been designed based on the proposed PBSC and fabricated in an advanced 28 nm CMOS technology. The regulators are distributed around the perimeter of the on-chip circuits, as shown in Fig. 2, regulating the power grid at 0.7 V with an input voltage of 1.0 V and maximum load current of 788 mA. The on-chip regulators simultaneously drive a power network, delivering current to the on-chip loads. To evaluate the system response under different load conditions, controllable current loads are integrated onto

TABLE III
TRANSIENT STEP RESPONSE AT THE LOAD UNDER LINE AND TEMPERATURE VARIATIONS

Type of variation (V_{IN}, temperature)	DC V_{OUT} at low I_{LOAD}			DC V_{OUT} at high I_{LOAD}			Voltage droop		
	Simulated (mV)	Measured (mV)	Error (%)	Simulated (mV)	Measured (mV)	Error (%)	Simulated (mV)	Measured (mV)	Error (%)
1.0 V, 25°C	699.7	700.8	0.16	697.5	698.9	0.20	64.5	64.9	0.06
1.1 V, 25°C	700.6	701.1	0.07	698.4	699.0	0.09	62.0	61.4	0.09
0.9 V, 25°C	698.6	698.3	0.04	696.1	696.0	0.01	71.0	71.1	0.01
1.0 V, 125°C	698.1	692.3	0.83	695.6	690.0	0.80	47.9	55.0	1.00
1.0 V, −25°C	702.4	704.3	0.27	698.7	702.4	0.53	63.1	63.3	0.03

the test circuit. These current loads can be activated separately or simultaneously, exhibiting different current loads at individual LDO regulators. All of the measurements are performed on the LDO regulators within the distributed power delivery system.

Load sharing variations are a primary concern for maintaining stability in distributed power delivery systems. Feasible current loads for the power delivery system are based on system specifications. When all of the integrated loads are simultaneously activated, the distributed system is loaded with a maximum current of 6×131.3 mA $= 788$ mA. Assuming a uniform distribution of load circuits, the maximum load current is evenly distributed among the voltage regulators. Alternatively, currents lower than the maximum load current can be drawn by those circuits located in close proximity to a specific regulator and farther from the other regulators, exhibiting significant load sharing variations.

To demonstrate the stability of the distributed power delivery system under maximum load currents and fast load transitions, the load current of the system is ramped from 52 mA to 788 mA in 5 ns at 25°C. The measured transient response for nominal input and output voltages of, respectively, 1.0 V and 0.7 V is illustrated in Fig. 14, exhibiting a stable response and voltage droop of 0.1 V. The simulation results for the power delivery system with six on-chip LDOs are also shown in Fig. 14, exhibiting a voltage droop of 0.94 V and strong correlation with the experimental results. The quiescent current of the power delivery system of six distributed LDO regulators under a maximum current load of 788 mA at 25°C is 4 mA, yielding 99.49% current efficiency.

To evaluate the effect of load sharing variations on the stability of a power delivery system, the system is measured for different PVT variations. The total load current of the distributed power delivery system with six LDO regulators is ramped in 5 ns from 17 mA to 309 mA, from 52 mA to 441 mA, and from 420 mA to 900 mA for, respectively, −25°C, 25°C, and 125°C. In addition, the system is evaluated at 25°C under ±10% line variations. Due to load sharing and PVT variations, the load current of a single LDO regulator significantly increases or decreases as compared to the nominal current, as described in Section III-E. The DC voltages and voltage droop for a transient response of both the experimental and simulated distributed systems are listed in Table III for ±10% input voltage variations, and −25°C, 25°C, and 125°C, exhibiting less than 1.2% error when the simulation results are compared with the measured results. For all types

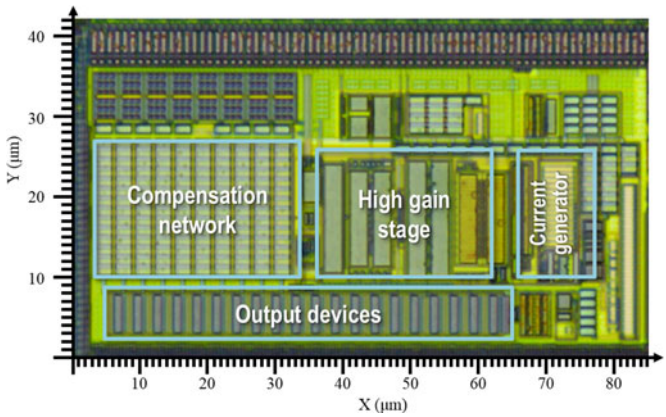

Fig. 15. Die microphotograph of a single LDO regulator and current generating circuit.

of variations, the distributed power delivery system exhibits a stable response over a wide range of temperatures with less than 10% voltage droop. Note the strong correlation between the simulated and measured results. An extended set of measurements and comparison with an existing state-of-the art power delivery system can be found in [35]. A die microphotograph of the LDO is shown in Fig. 15. The area occupied by the LDO with all capacitors is 85 μm $\times$ 42 μm.

V. CONCLUSION

Distributed on-chip power regulation and delivery are necessary for delivering high quality power to modern high performance ICs. Significant load sharing and PVT variations, however, pose stability challenges on the co-design of these multiple on-chip voltage regulators. The design complexity of the parallel voltage regulators driving the same power grid can be traded off for high power quality. To design a stable closed loop regulator, sufficient phase margin in the open loop transfer function is required. Phase margin is, therefore, a sufficient parameter for determining the stability of a single LDO. Evaluating the open loop characteristics is, however, not practical with parallel LDO regulators due to the multiple regulation loops. Evaluation of the stability of a distributed power delivery system is, therefore, not possible with the traditional phase margin criterion.

An alternative PBSC is proposed for evaluating the stability of parallel voltage regulators driving a single power grid. Based on this criterion, a distributed power delivery system is stable

if the total output impedance of the parallel connected LDOs exhibits no RHP poles and a phase between -90° and $+90^\circ$. Similar to a single voltage regulator, the phase margin of the output impedance (the difference between the maximum phase and 90°) determines the stability of a distributed power delivery system. Integration of the proposed stability criterion within a design automation flow should be considered as part of a general framework for designing stable power delivery systems.

A distributed power delivery system with six ultra-small fully integrated LDO regulators has been designed based on the proposed passivity-based criterion and fabricated in a 28 nm CMOS process. An adaptive bias technique is used to enhance the transient performance and increase the power efficiency by, respectively, boosting and decreasing the bias current. In addition, an adaptive compensation network is employed within the power delivery system that supports the co-design of a system of distributed parallel LDO regulators, yielding a stable system response from -25°C to 105°C with 10% voltage variations. The proposed PBSC is shown to be a simple and efficient method to evaluate the stability of a distributed power delivery system. The system is believed to be one of the first successful silicon demonstrations of stable parallel analog LDO regulators.

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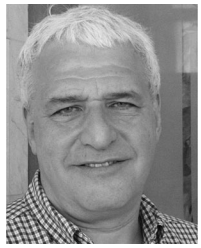

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