Inductive Properties of High-Performance Power Distribution Grids

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***Abstract*—The design of high integrity, area efficient power distribution grids has become of practical importance as the portion of on-chip interconnect resources dedicated to power distribution networks in high performance integrated circuits has greatly increased. The inductive characteristics of several types of gridded power distribution networks are described in this paper. The inductance extraction program FastHenry is used to evaluate the inductive properties of grid structured interconnect. In power distribution grids with alternating power and ground lines, the inductance is shown to vary linearly with grid length and inversely linearly with the number of lines in the grid. The inductance is also relatively constant with frequency in these grid structures. These properties permit the efficient estimation of the inductive characteristics of power distribution grids. To optimize the process of allocating on-chip metal resources, inductance/area/resistance tradeoffs in high speed performance distribution grids are explored. Two tradeoff scenarios in power grids with alternating power and ground lines are considered. In the first scenario, the total area occupied by the grid lines is maintained constant and the grid inductance versus grid resistance tradeoff is evaluated as the width of the grid lines varies. In the second scenario, the metal area of the grid is maintained constant and the grid inductance versus grid area tradeoff is investigated. In both cases, the grid inductance increases virtually linearly with line width, rising more then eightfold for a tenfold increase in line width. The grid resistance and grid area, however, decrease relatively slowly with line width. This decrease in grid resistance and area is limited to a factor of two under assumed interconnect characteristics.**

***Index Terms*—Inductance, mutual inductance, partial inductance, power distribution networks, power grids.**

I. Introduction

THE ONGOING miniaturization of integrated circuit (IC) feature size has placed significant requirements on the power and ground distribution network. Circuit integration densities rise with each very deep submicrometer (VDSM) technology generation due to smaller devices and larger dies; the current density and the total current increase accordingly. At the same time the higher speed switching of smaller transistors produces faster current transients in the power distribution network. The higher currents cause large ohmic IR voltage drops and fast current transients cause large inductive $L(di/dt)$ voltage drops (ΔI noise) in the power distribution networks. Power distribution networks must be designed to minimize these voltage drops, maintaining the local supply voltage within specified design margins. If the power supply voltage sags too low, the performance and functionality of the circuit is severely compromised. Alternatively, excessive overshoot of the supply voltage can affect circuit reliability. Further exacerbating these problems is the reduced noise margins as the supply voltage is decreased with each generation of VDSM process technology.

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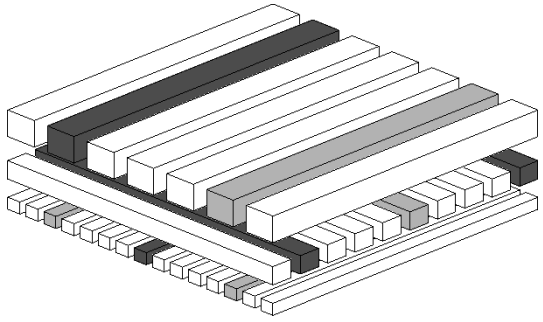

Fig. 1. A multilayer interconnect with the power distribution grid highlighted; the ground lines are light gray, the power lines are dark gray, and the signal lines are white.

Power distribution networks in high-performance digital ICs are commonly structured as a multilayer grid. In such a grid, straight power/ground (P/G) lines in each metallization layer span the entire die (or a large functional unit) and are orthogonal to the lines in the adjacent layers. The power and ground lines typically alternate in each layer. Vias are used to connect a power (ground) line to another power (ground) line at the overlap sites. The power grid concept is illustrated in Fig. 1, where three layers of interconnect are depicted with the power lines shown in dark gray and the ground lines shown in light gray. The power/ground lines are surrounded by signal lines.

A. Inductance of On-Chip Power Grid

To maintain the local supply voltage within specified design margins, the power distribution network should be low impedance as seen from the power terminals of the circuit elements. With transistor switching times as low as a few picoseconds, the on-chip signals typically contain significant harmonics at frequencies as high as $\sim$100 GHz. For on-chip lines, the inductive reactance ωL dominates the overall line impedance beyond $\sim$10 GHz. The on-chip inductance affects the integrity of the power supply through two phenomena. First, the magnitude of the ΔI noise is directly proportional to the power network inductance as seen at the current sink. Second, the network resistance, inductance, and decoupling capacitance

form an RLC network with multiple resonances. The peak impedance of this RLC circuit must be lowered to guarantee the target power supply noise margins. Thus, characterizing the information is needed to perform accurate RLC modeling and analysis of power distribution networks.

The term "inductance" has been used to designate two different aspects. The strict meaning of the term is the *absolute inductance*, which is measured in Henrys. Sometimes, however, the term inductance has been loosely used to denote the *inductive behavior* of a circuit; namely, overshoots, ringing, signal reflections, etc. The inductive behavior is not the same as the absolute inductance of the circuit. Specific metrics have been developed to evaluate the onset of inductive behavior in high speed digital circuits [1], [2], [3]. The primary focus of this paper is on the absolute inductance of power distribution grids.

B. Tradeoffs in Power Distribution Grids

Global on-chip power distribution networks are typically designed at the early stages of the design process, when little is known about the power demands at specific locations on an integrated circuit (IC). Furthermore, allocating additional metal resources for the global power distribution at the later stages of the design process in order to improve the local electrical characteristics of the power network is likely to necessitate a complete redesign of the surrounding global signals and, therefore, can be prohibitively expensive. For these reasons, power distribution networks tend to be conservatively designed [4], sometimes using more than a third of the on-chip metal resources [5], [6]. Overengineering the power supply system is, therefore, costly in modern interconnect limited, high complexity digital integrated circuits.

Various tradeoffs exist in the design of on-chip power distribution networks. Design objectives in power distribution networks, such as low impedance (low inductance and resistance), small area, and low current densities (for improved reliability) are typically in conflict. Widening the line to increase the conductance and improve the electromigration reliability also increases the grid area. Replacing wide metal lines with narrow interdigitated power/ground (P/G) lines increases the line resistance if the grid area is maintained constant or increases the area if the net cross section of the lines is maintained constant. It is therefore important to make a balanced choice under these conditions. A quantitative model of the inductance/area/resistance tradeoff in high performance power distribution networks is therefore needed to achieve an efficient power distribution network. The second important result presented here is quantitative tradeoff guidelines and physical intuition for the design of high performance power distribution networks.

C. Outline

This paper is organized as follows. Existing work on the design of on-chip power distribution networks in high complexity digital circuits is surveyed in Section II. A brief overview of the partial inductance concept is presented in Section III. The dependence of inductance on frequency is discussed in Section IV. The simulation setup is described in Section V. In Section VI, the inductive characteristics of a current loop formed by a power transmission line are established. The three types of grid structures considered in this paper are described in Section VII. The dependence of the inductance characteristics on the line width is discussed in Section VIII. The differences in the inductive properties among the three types of grids are reviewed in Section IX. The dependence of the grid inductance on grid dimensions is described in Section X. The dependence of the power distribution inductance on frequency is discussed in Section XI. Inductance/area/resistance tradeoffs in high performance power distribution grids are analyzed in Section XII. The conclusions are summarized in Section XIII.

II. Background

Research in on-chip power distribution networks can be classified into several categories: automated sizing and routing, modeling and simulation, and design and optimization methodologies. Of these categories, the design methodology and optimization topic is the least developed, with relatively little published work.

The problem of optimizing on-chip multilevel power distribution grids has been considered by Song and Glasser [7]. In their early work published in 1986, a simple model is presented to estimate the maximum on-chip IR drop as a function of the number of metal layers and the metal layer thickness. The optimal thickness of each metal layer to produce minimum IR drops is determined. Design guidelines are provided that maximize signal wiring area while maintaining a constant IR drop. Application of these results to current high complexity VDSM integrated circuits is, however, limited.

An alternative approach for on-chip power distribution called a "cascaded power/ground ring" has been proposed by Cao and Krusius [8]. This approach focuses on maximizing the amount of wiring resources available for signal routing.

The inductance of on-chip power distribution networks has traditionally been neglected because the network inductance has been dominated by the parasitic inductance of the package pins, traces, and bond wires. The situation is changing due to the increasing switching speed of integrated circuits [9] and the lower inductance of advanced flip-chip packaging. Priore noted in [10] that replacing wide power and ground lines with narrower interdigitated power and ground lines reduces the self inductance of the supply network. He also suggested an approximate expression for the time constant of the response of a power supply network to a voltage step input signal. Zheng and Tenhunen [11] proposed replacing the wide power and ground lines with an array of interdigitated narrow power and ground lines, decreasing the characteristic impedance and inductance of the power grid. A technique for constructing a detailed RLC model of on-chip circuits, including the inductance of the power grid, is presented in [12]. Circuit simulations are used to explore the impact of various model components on the integrity of on-chip signals.

III. Partial Inductance

The construct of a partial self and mutual inductance is useful in evaluating the inductive properties of circuits. The concept of

a partial inductance was first developed by Rosa in 1908 in application to linear conductors [17]. The need for a partial inductance arose because single linear conductors do not form closed loop circuits in which the total magnetic flux through the circuit can be clearly defined, permitting the circuit inductance to be readily determined through calculation of the magnetic flux. Thus, the partial (self and mutual) inductance is intended to represent the inductance that a circuit segment contributes *as a part of a closed loop circuit*. Rosa made an intuitive argument that for this purpose only the magnetic lines between the two planes perpendicular to a linear conductor and intersecting the conductor ends should be considered. That is, the magnetic flux of interest is the flux through the loop formed by the conductor and the two lines originating from and perpendicular to the conductor ends; the loop is closed at infinity. The remaining magnetic flux is considered when the closed loop inductance is calculated from the self and mutual partial inductance of the circuit segments according to the standard formulæ for series and parallel connections of inductors. The concept proved useful and was utilized in the inductance calculation formulæ and tables developed by Rosa and Cohen [18], Rosa and Grover [19], and Grover [20]. A rigorous theoretical treatment of the subject was first provided by Ruehli in [21], where a general definition of the partial inductance of an arbitrarily shaped conductor is given in terms of the magnetic vector potential. Ruehli also coined the term "partial inductance."

The process of calculating the inductance through the partial inductance concept proceeds as follows. A closed loop circuit structure is broken into smaller elements; each of these elements does not by itself form a closed circuit. Typically, the circuit is partitioned into elements of simple shape, such as straight line elements of constant cross section, for which precise and convenient analytical partial inductance formulæ are available. Each of these elements is assigned a *partial* self inductance. Each pair of these elements is assigned a *partial* mutual inductance (although none of the elements forms a closed loop). The partial self and mutual inductances of the circuit fragments and the topology of the fragment connections are all of the information required to calculate the total self and mutual inductance of the circuit. If the circuit is complete and forms a loop, the resulting total inductance is the *loop* inductance of the circuit. If the circuit is a subcircuit of a larger circuit, the resulting total inductance is the partial inductance of the open circuit.

The relationship between the loop and partial inductances is particularly straightforward for a circuit composed of series connected elements. Given a number of series connected elements N, the partial inductances can be arranged as a matrix $L_{ij}\, 1 \leq i, j \leq N$, where L_{ii} is the partial self inductances of the element i and $L_{ij}\ i \neq j$ is the partial mutual inductance between elements i and j $(L_{ij} = L_{ji})$. The value of L_{ij} is negative if the currents in the associated elements flow in opposite directions. The inductance of the entire loop is the sum of all of the elements of the matrix: $L_0 = \sum_{i=1}^{N} \sum_{j=1}^{N} L_{ij}$.

The relationship between the loop inductance of a circuit and the partial inductances of circuit segments becomes more complicated in more complex topologies. Network reduction methods can be applied to simplify the network by coalescing several segments into one circuit element. For example, several elements connected in series (or in parallel) can be replaced by a single element with the self and mutual inductances calculated from the inductances of the original elements. If a new circuit element does not form a complete loop, the resulting self and mutual inductance of the element is similar to a partial inductance. In a general case, such "incomplete" inductances may contain branching and merging currents and therefore may not comply in a strict sense with the definition of a partial inductance. For the purpose of the present work, the difference between incomplete and partial inductances is insignificant and both are referred to as "partial."

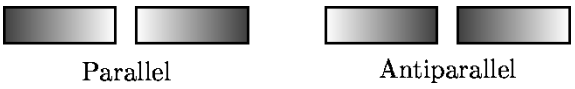

Fig. 2. Current density distribution in the cross section of two closely spaced lines at high frequencies. Darker shades of gray indicate higher current densities. In lines carrying current in the same direction (parallel currents), the current concentration is shifted away from the parallel current, minimizing the effective coupling between the two currents and, therefore, the circuit inductance. In lines carrying current in opposite directions (antiparallel currents), the current concentrates toward the antiparallel current, minimizing the current loop area, and, therefore, minimizing the circuit inductance.

IV. Dependence of Inductance on Frequency

The inductance of the on-chip structures can decrease significantly with signal frequency. It is, therefore, important to choose the relevant frequency when evaluating the inductance. This dependence of inductance on frequency is due to several effects.

Part of the decrease in inductance at high frequency is due to the decrease in the internal inductance. The partial inductance of a conductor can be expressed as $L_{\text{line}} = L_{\text{internal}} + L_{\text{external}}$, where L_{external} is the inductance due to the magnetic field outside the conductor and L_{internal} is the inductance due to the magnetic field inside the conductor. With the onset of the skin effect, the current concentrates near the conductor surface, reducing the magnetic field in the line core and, consequently, the internal inductance of the line L_{internal}. For a round line at low frequency (where the current distribution is uniform across the line cross section), the internal inductance is 0.05 nH/mm independent of the radius (see the derivation in [22]). For a line with a rectangular cross section, the internal inductance is similar to the internal inductance of the round line and decreases with the aspect ratio of the cross section. On-chip structures typically exhibit a loop inductance between 0.4 and 1 nH/mm. The reduction in the internal inductance due to the skin effect is, therefore, relatively insignificant.

The inductance is also reduced by the proximity effect. At high frequencies, the current distribution profile in closely placed lines shifts so as to minimize the circuit inductance, as shown in Fig. 2. However, in ICs this effect is only significant in immediately adjacent wide lines operating at very high frequencies.

The redistribution of the current among several alternative paths is typically the primary cause of the decrease in on-chip inductance with frequency. This mechanism will henceforth be referred to as multipath current redistribution. For example, in standard single-ended digital logic the forward current path is

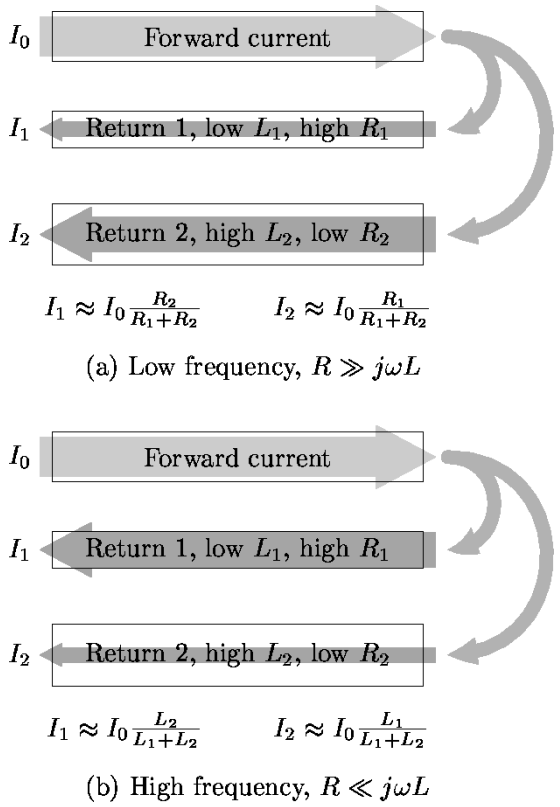

Fig. 3. Current loop with two alternative current return paths. The forward current I_0 returns both through return path one with resistance R_1 and inductance L_1, and return path two with resistance R_2 and inductance L_2. In this structure, $L_1 < L_2$ and $R_1 > R_2$. At low frequencies (a), the path impedance is dominated by the line resistance and the return current is distributed between two return paths according to the resistance of the lines. Thus, at low frequencies, most of the return current flows through the return path of lower resistance, path two. At very high frequencies (b), however, the path impedance is dominated by the line inductance and the return current is distributed between two return paths according to the inductance of the lines. Most of the return current flows through the path of lower inductance, path one, minimizing the overall inductance of the circuit.

typically composed of a single line. No redistribution of the forward current occurs. The current return path, though, is typically not explicitly specified (although local shielding for particularly sensitive nets has become common) and adjacent signal and power lines provide several alternative current return paths. A significant redistribution of the return current among these return paths can occur as signal frequencies increase. At low frequencies, the line impedance $Z(\omega) = R(\omega) + j\omega L(\omega)$ is dominated by the interconnect resistance $R(\omega)$. In this case, the distribution of the return current over the available return paths is determined by the resistance of the paths, as shown in Fig. 3(a). The return current spreads out far from the signal line to reduce the resistance of the return path and, therefore, the impedance of the current loop. At high frequencies, the line impedance $Z(\omega) = R(\omega) + j\omega L(\omega)$ is dominated by the reactive component $j\omega L(\omega)$ and the minimum impedance path is primarily determined by the inductance $L(\omega)$, as shown in Fig. 3(b). In power grids, the redistribution of both the forward and return currents can occur as both the forward and return paths consist of multiple conductors connected in parallel.

The phenomenon underlying these three frequency effects (the reduction of the internal inductance, the proximity effect, and multipath current redistribution) is, essentially, the same: the current path is altered to minimize the total impedance. At very high signal frequencies, the inductance dominates the circuit impedance; therefore, the path of minimum loop inductance is the path of minimum impedance. The difference between the aforementioned effects is that in the case of multi-path current redistribution the current is redistributed among several different lines, while in the case of the reduction in internal inductance and the proximity effect the current is redistributed across the cross section of the same line. A thick line can be considered to be composed of multiple thin lines bundled together in parallel. The reduction in internal inductance and the proximity effect in a thick line can be considered as special cases of current redistribution among multiple thin lines forming a thick line. These effects are therefore accurately modeled by multipath current redistribution if thick lines are considered as bundles of thin lines.

In this investigation, a frequency of 1 GHz is used to analyze the low frequency case, where the reactance is comparable to the resistance but does not yet dominate the interconnect impedance for typical on-chip lines. A frequency of 100 GHz is used to analyze the high frequency case, where the line reactance completely dominates the impedance and the line resistance has a minimal effect on the inductive properties of the circuit.

V. Simulation Setup

The inductance extraction program FastHenry [23] is used to explore the inductive properties of grid structures. FastHenry efficiently calculates the frequency dependent self and mutual impedances, $R(\omega) + \omega L(\omega)$, in complex three-dimensional interconnect structures. A magnetoquasistatic approximation is assumed, meaning the distributed capacitance of the line and any related displacement currents associated with the capacitance are ignored. The accelerated solution algorithm employed in the program provides approximately a 1% worst case accuracy as compared with the direct solution of the system of linear equations characterizing the system [23].

A conductivity of 58 S/μm $\simeq$ (1.72 $\mu\Omega \cdot$ cm)$^{-1}$ is assumed for the interconnect material. The inductive portion of the impedances is relatively insensitive to the interconnect resistivity in the range of 1.7 $\mu\Omega \cdot$ cm to 2.5 $\mu\Omega \cdot$ cm (typical for advanced processes with copper interconnect [24], [25], [26]). A conductivity of 40 S/μm (2.5 $\mu\Omega \cdot$ cm)$^{-1}$ yields an inductance that is less than 4% larger than the inductance obtained for a conductivity of 58 S/μm.

A line thickness of 1 μm is assumed for the interconnect structures. In the analysis, the lines are split into multiple filaments to account for skin and proximity effects, as discussed in Section IV. The number of filaments is chosen to be sufficiently large to achieve a 1% accuracy of the computed values. Simulations are performed at three frequencies, 1 GHz, 10 GHz, and 100 GHz. Typical simulation run times for the structures are under one minute on a Sun Blade 100 workstation.

VI. Power Transmission Circuit

Consider a power transmission circuit as shown in Fig. 4(a). The circuit consists of the forward current (power) path and the

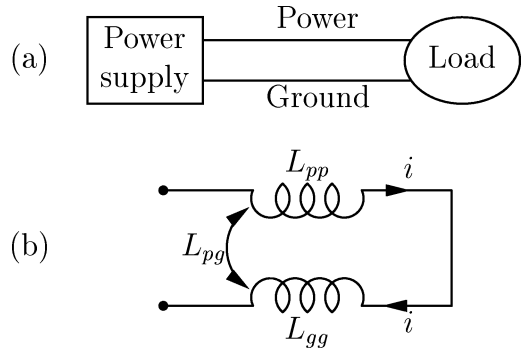

Fig. 4. A simple power transmission circuit; (a) block diagram, (b) the equivalent inductive circuit.

return current (ground) path forming a transmission current loop between the power supply at one end of the loop and a power consuming circuit at the other end. In a simple case, the forward and return paths each consist of a single conductor. In general, a "path" refers to a multi-conductor structure carrying current in a specific direction (to or from the load), which is the case in power distribution grids. The circuit dimensions are assumed to be sufficiently small for the lumped circuit approximation to be valid. The inductance of both terminating devices is assumed negligible as compared to the inductance of the transmission line. The inductive characteristics of the current loop are therefore, determined by the inductive properties of the forward and return current paths.

The power transmission loop consists of the forward and return current paths. The equivalent inductive circuit is depicted in Fig. 4(b). The partial inductance matrix for this circuit is

$$L_{ij} = \begin{bmatrix} L_{pp} & -L_{pg} \\ -L_{gp} & L_{gg} \end{bmatrix} \tag{1}$$

where L_{pp} and L_{gg} are the partial self inductances of the forward and return current paths, respectively, and L_{pg} is the absolute value of the partial mutual inductance between the paths. The loop inductance of the power transmission loop is

$$L_{\text{loop}} = L_{pp} + L_{gg} - 2L_{pg}. \tag{2}$$

The mutual coupling L_{pg} between the power and ground paths reduces the loop inductance. This behavior can be formulated more generally: *the greater the mutual coupling between antiparallel (flowing in opposite directions) currents, the smaller the loop inductance of a circuit*. The effect is particularly significant when the mutual inductance is comparable to the self inductance of the current paths. This is the case when the line separation is comparable to the dimensions of the line cross section.

The effect of the coupling on the net inductance is reversed when currents of the two inductive coupled paths flow in the same direction. For example, in order to reduce the partial inductance L_{11} of line segment 1, another line segment 2 with partial self inductance L_{22} and coupling L_{12} is placed in parallel with segment 1. A schematic of the equivalent inductance

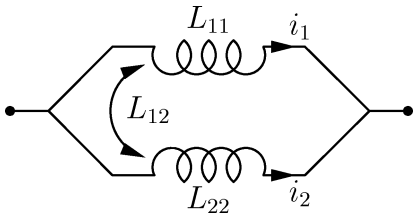

Fig. 5. Two parallel coupled inductors.

is shown in Fig. 5. The resulting partial inductance of the current path is

$$L_{1\|2} = \frac{L_{11}L_{22} - L_{12}^2}{L_{11} + L_{22} - 2L_{12}}. \tag{3}$$

For the limiting case of no coupling, this expression simplifies to $L_{11}L_{22}/(L_{11} + L_{22})$. In the opposite case of full coupling of segment 1, $L_{11} = L_{12}$ $(L_{11} \leq L_{22})$ and the total inductance becomes L_{11}. For two identical parallel elements, (3) simplifies to $L_{\|} = (L_{\text{self}} + L_{\text{mutual}})/2$. In general, *the greater the mutual coupling between parallel (flowing in the same directions) currents, the greater the loop inductance of a circuit*. To present this concept in an on-chip perspective, consider a 1000 μm long line with a 1 μm $\times$ 3 μm cross section, and a partial self inductance of 1.342 nH (at 1 GHz). Adding another identical line in parallel with the first line with a 17 μm separation (20 μm line pitch) results in a mutual line coupling of 0.725 nH and a net inductance of 1.033 nH ($\sim$55% higher than $L_{\text{self}}/2 = 0.671$ nH).

The inductive coupling among the conductors of the same circuit can, therefore, either increase or decrease the total inductance of the circuit. To minimize the circuit inductance, the coupling of conductors carrying currents in the same direction should be reduced by increasing the distance between the conductors. The coupling of conductors carrying current in opposite directions should be increased by physically placing the conductors closer to each other. This optimization naturally occurs in grid structured power distribution networks with alternating power and ground lines, as discussed in the following sections.

VII. Grid Types

To assess the dependence of the inductive properties on the power and ground lines, the coupling characteristics of three types of power/ground grid structures have been analyzed. In the grids of the first type, called *noninterdigitated grids*, the power lines fill one half of the grid and the ground lines fill the other half of the grid, as shown in Fig. 6(a). In *interdigitated grids*, the power and ground lines are alternated and equidistantly spaced, as shown in Fig. 6(b). The grids of the third type are a variation of the interdigitated grids. Similar to interdigitated grids, the power and ground lines are alternated, but rather than placed equidistantly, the lines are placed in equidistantly spaced pairs of adjacent power and ground lines, as shown in Fig. 6(c). These grids are called *paired grids*. Interdigitated and paired grids are grids with alternating power and ground lines.

The number of power lines matches the number of ground lines in all of the grid structures. The number of power/ground line pairs is varied from one to ten. The grid lines are assumed to be 1 mm long and are placed on a 20 μm pitch. The specific

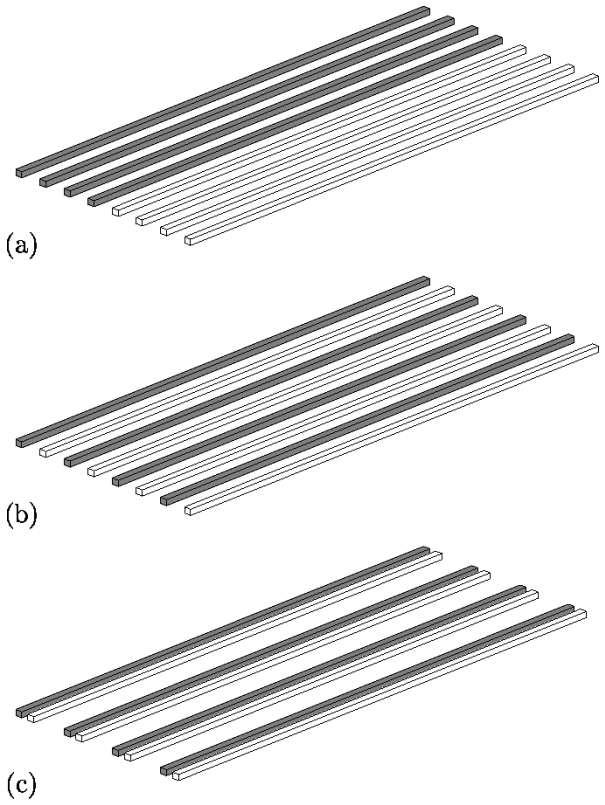

Fig. 6. Power/ground grid structures under investigation: (a) a noninterdigitated grid, (b) a grid with the power lines interdigitated with the ground lines, and (c) a paired grid, the power and ground lines are in close pairs. The power lines are gray colored, the ground lines are white colored.

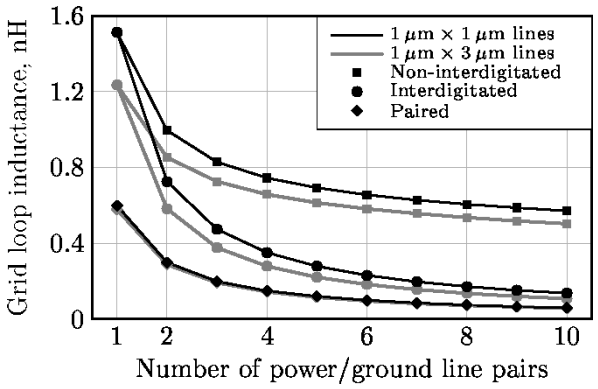

Fig. 7. Loop inductance of the power/ground grids as a function of the number of power/ground line pairs (at a 1-GHz signal frequency).

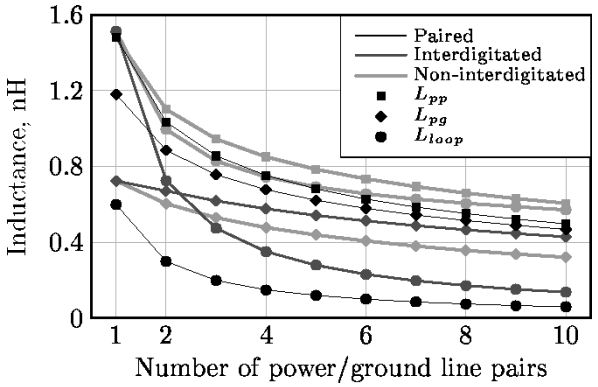

Fig. 8. Loop and partial inductance of the power/ground grids with 1 μm × 1 μm cross section lines (at a 1-GHz signal frequency).

line length is unimportant since at these high length to line pitch ratios the inductance scales nearly linearly with the line length, as discussed in Section X.

An analysis of these structures has been performed for two line cross sections, 1 μm × 1 μm and 1 μm × 3 μm. For each of these structures, the following characteristics have been determined: the partial self inductance of the power (forward current) and ground (return current) paths L_{pp} and L_{gg}, respectively, the power to ground path coupling L_{pg}, and the loop inductance L_{loop}. When determining the loop inductance, all of the ground lines at one end of the grid are short circuited to form a ground terminal, all of the power lines at the same end of the grid are short circuited to form a power terminal, and all of the lines at the other end of the grid are short circuited to complete the current loop. This configuration assumes that the current loop is completed on-chip. This assumption is valid for high frequency signals which are effectively terminated through the on-chip decoupling capacitance which provides a low impedance termination as compared to the inductive leads of the package. The on-chip inductance affects the signal integrity of the high frequency signals. If the current loop is completed on-chip, the current in the power lines is always antiparallel to the current in the ground lines.

The loop inductance of the three types of grid structures operating at 1 GHz is displayed in Fig. 7 as a function of the number of lines in the grid. The partial self and mutual inductance of the power and ground current paths is shown in Fig. 8 for grid structures with 1 μm × 1 μm cross section lines and in Fig. 8 for grids with 1 μm × 3 μm cross section lines. The inductance data for 1 GHz and 100 GHz are summarized in Table I. The data depicted in Figs. 7, 8, and 9 are discussed in the following three sections.

The signal lines surrounding the power grids are omitted from the analysis. This omission is justified by the following considerations. First, current returning through the signal lines instead of the power/ground network causes crosstalk noise on the lines. To minimize this undesirable effect, the circuits are designed in such a way that the majority of the return current flows through the power and ground lines. Second, the signal lines provide additional paths for the return current and only decrease the inductance of the power distribution network. The value of the grid inductance obtained in the absence of signal lines can therefore be considered as an upper bound.

VIII. Inductance Versus Line Width

The loop inductance of the grid depends relatively weakly on the line width. Grids with 1 μm × 3 μm cross section lines have a lower loop inductance than grids with 1 μm × 1 μm cross section lines. This decrease in inductance is dependent upon the grid type, as shown in Fig. 7. The largest decrease, approximately 21%, is observed in interdigitated grids. In noninterdigitated grids, the inductance decreases by approximately 12%. In paired grids, the decrease in inductance is limited to 3% to 4%.

This behavior can be explained in terms of the partial inductance, L_{pp} and L_{pg} [13]. Due to the symmetry of the power and

TABLE I
INDUCTIVE CHARACTERISTICS OF POWER/GROUND GRIDS WITH A 40-μm LINE PAIR PITCH OPERATING AT 1 GHz AND 100 GHz

# of P/G pairs	Line cross section (μm × μm)	L_{pp}, L_{gg} (nH)			L_{pg} (nH)			L_{loop} (nH)		
		N/int	Int	Paired	N/int	Int	Paired	N/int	Int	Paired
1 GHz										
1	1 × 1	1.481	1.481	1.481	0.724	0.724	1.181	1.513	1.513	0.599
1	1 × 3	1.342	1.342	1.342	0.725	0.725	1.053	1.235	1.235	0.579
2	1 × 1	1.102	1.035	1.035	0.604	0.671	0.886	0.996	0.726	0.299
2	1 × 3	1.031	0.963	0.966	0.604	0.672	0.822	0.853	0.582	0.288
3	1 × 1	0.945	0.856	0.857	0.530	0.619	0.757	0.829	0.474	0.199
3	1 × 3	0.894	0.807	0.810	0.531	0.618	0.714	0.726	0.377	0.192
4	1 × 1	0.851	0.753	0.753	0.478	0.577	0.678	0.745	0.351	0.149
4	1 × 3	0.809	0.714	0.717	0.479	0.575	0.645	0.658	0.279	0.144
5	1 × 1	0.785	0.682	0.682	0.439	0.542	0.622	0.693	0.279	0.120
5	1 × 3	0.748	0.649	0.652	0.440	0.539	0.594	0.614	0.221	0.115
6	1 × 1	0.735	0.628	0.629	0.407	0.513	0.579	0.656	0.231	0.100
6	1 × 3	0.700	0.600	0.602	0.409	0.509	0.555	0.582	0.183	0.096
7	1 × 1	0.694	0.586	0.587	0.380	0.488	0.544	0.628	0.197	0.085
7	1 × 3	0.661	0.561	0.563	0.383	0.483	0.522	0.557	0.156	0.082
8	1 × 1	0.660	0.552	0.552	0.357	0.466	0.515	0.606	0.172	0.075
8	1 × 3	0.629	0.529	0.531	0.361	0.461	0.495	0.536	0.136	0.072
9	1 × 1	0.631	0.523	0.523	0.338	0.446	0.490	0.588	0.152	0.066
9	1 × 3	0.601	0.502	0.504	0.342	0.441	0.472	0.518	0.120	0.064
10	1 × 1	0.606	0.497	0.498	0.321	0.429	0.468	0.571	0.137	0.060
10	1 × 3	0.577	0.478	0.480	0.326	0.424	0.451	0.503	0.108	0.057
100 GHz										
1	1 × 1	1.468	1.468	1.457	0.724	0.724	1.181	1.486	1.486	0.551
1	1 × 3	1.315	1.315	1.291	0.725	0.725	1.062	1.180	1.180	0.457
2	1 × 1	1.088	1.022	1.023	0.604	0.670	0.886	0.968	0.703	0.275
2	1 × 3	1.010	0.945	0.940	0.605	0.670	0.826	0.810	0.548	0.228
3	1 × 1	0.928	0.845	0.848	0.533	0.616	0.756	0.789	0.458	0.183
3	1 × 3	0.873	0.793	0.792	0.534	0.615	0.716	0.678	0.355	0.152
4	1 × 1	0.830	0.741	0.745	0.483	0.571	0.676	0.695	0.340	0.138
4	1 × 3	0.788	0.702	0.702	0.484	0.570	0.645	0.607	0.263	0.114
5	1 × 1	0.762	0.671	0.674	0.444	0.536	0.619	0.634	0.270	0.110
5	1 × 3	0.727	0.639	0.640	0.446	0.535	0.594	0.560	0.208	0.091
6	1 × 1	0.710	0.618	0.621	0.414	0.506	0.575	0.591	0.224	0.092
6	1 × 3	0.680	0.591	0.592	0.416	0.505	0.554	0.527	0.173	0.076
7	1 × 1	0.668	0.576	0.579	0.389	0.480	0.540	0.559	0.191	0.079
7	1 × 3	0.641	0.553	0.554	0.391	0.479	0.522	0.501	0.147	0.065
8	1 × 1	0.633	0.542	0.545	0.367	0.458	0.510	0.533	0.167	0.069
8	1 × 3	0.609	0.522	0.523	0.369	0.457	0.494	0.480	0.128	0.057
9	1 × 1	0.604	0.513	0.516	0.348	0.439	0.485	0.511	0.148	0.061
9	1 × 3	0.582	0.495	0.496	0.351	0.438	0.471	0.463	0.114	0.050
10	1 × 1	0.578	0.488	0.491	0.332	0.422	0.463	0.493	0.133	0.055
10	1 × 3	0.558	0.472	0.473	0.334	0.421	0.450	0.448	0.102	0.045

N/int — non-interdigitated grids, Int — interdigitated grids, Paired — paired grids, grid length — 1000 μm

ground paths, $L_{gg} = L_{pp}$, the relation of the loop inductance to the partial inductance (2) simplifies to

$$L_{\text{loop}} = L_{pp} + L_{gg} - 2L_{pg} = 2(L_{pp} - L_{pg}). \quad (4)$$

According to (4), L_{loop} increases with larger L_{pp} and decreases with larger L_{pg}. That is, decreasing the self inductance of the forward and return current paths forming the current loop decreases the loop inductance, while increasing the inductive coupling of the two paths decreases the loop inductance. The net change in the loop inductance depends, therefore, on the relative effect on L_{pp} and $L_{pg}$of increasing the line width in the structures of interest.

The self inductance of a single line is a weak function of the line cross-sectional dimensions, see (5) from [20]. This behavior

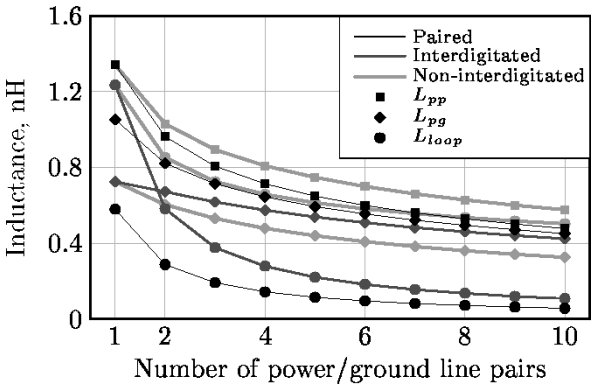

Fig. 9. Loop and partial inductance of the power/ground grids with 1 μm × 3 μm cross section lines (at a 1-GHz signal frequency).

is also true for the complex multi-conductor structures under investigation. Comparison of the data shown in Fig. 8 with the data shown in Fig. 9 demonstrates that changing the line cross section from 1 μm × 1 μm to 1 μm × 3 μm decreases L_{pp} by 4% to 6% in all of the structures under consideration.

The dependence of inductive coupling L_{pg} on the line width, however, depends on the grid type. In noninterdigitated and interdigitated grids, the line spacing is much larger than the line width and the coupling L_{pg} changes insignificantly with the line width. Therefore, the loop inductance $L_{\rm loop}$ in noninterdigitated and interdigitated grids decreases with line width primarily due to the decrease in self inductance of the forward and return current paths L_{pp} and L_{gg}.

In paired grids the line width is comparable to the line-to-line separation and the dependence of L_{pg} on the line width is nonnegligible: L_{pg} decreases by 4% to 6%, as quantified by comparison of the data shown in Fig. 8 with the data shown in Fig. 9. In paired grids, therefore, the grid inductance decreases more slowly with line width as compared with interdigitated and noninterdigitated grids, because a reduction in the self inductance of the current paths L_{pp} is significantly offset by a decrease in the inductive coupling of the paths L_{pg}.

IX. Dependence of Inductance on Grid Type

The grid inductance varies with the configuration of the grid. With the same number of power/ground lines, grids with alternating power and ground lines exhibit a lower inductance than noninterdigitated grids; this behavior is discussed in Section IX-A. The inductance of the paired grids is lower than the inductance of the interdigitated grids; this topic is discussed in Section IX-B.

A. Noninterdigitated Versus Interdigitated Grids

The difference in inductance between noninterdigitated and interdigitated grids increases with the number of lines, reaching an approximately 4.2 difference for ten power/ground line pairs for the case of a 1 μm × 1 μm cross section line, as shown in Fig. 7 ($\sim$4.7 difference for the case of a 1 μm × 3 μm cross section line). This difference is due to two factors.

First, in noninterdigitated grids the lines carrying current in the same direction (forming the forward or return current paths) are spread over half the width of the grid, while in interdigitated (and paired) grids both the forward and return paths are spread over the entire width of the grid. The smaller the separation between the lines, the greater the mutual inductive coupling between the lines and the partial self inductance of the forward and return paths, L_{pp} and L_{gg}, as described in Section VI. This trend is confirmed by the data shown in Figs. 8 and 9, where interdigitated grids have a lower L_{pp} as compared to noninterdigitated grids.

Second, each line in the interdigitated structures is surrounded with lines carrying current in the opposite direction, creating strong coupling between the forward and return currents and increasing the partial mutual inductance L_{pg}. Alternatively, in the noninterdigitated arrays [see Fig. 6(a)], all of the lines (except for the two lines in the middle of the array) are surrounded with lines carrying current in the same direction. The power-to-ground inductive coupling L_{pg} is therefore lower in noninterdigitated grids, as shown in Figs. 8 and 9.

In summary, the interdigitated grids exhibit a lower partial self inductance L_{pp} and a higher partial mutual inductance L_{pg} as compared to noninterdigitated grids [13]. The interdigitated grids, therefore, have a lower loop inductance $L_{\rm loop}$ as described by (4).

B. Paired Versus Interdigitated Grids

The loop inductance of paired grids is 2.3 times lower than the inductance of the interdigitated grids for the case of a 1 μm × 1 μm cross section line and is 1.9 times lower for the case of a 1 μm × 3 μm cross section line, as shown in Fig. 7. The reason for this difference is described as follows in terms of the partial inductance. The structure of the forward (and return) current path in a paired grid is identical to the structure of the forward path in an interdigitated grid (only the relative position of the forward and return current paths differs). The partial self inductance L_{pp} is therefore the same in paired and interdigitated grids; the two corresponding curves completely overlap in Figs. 8 and 9. The values of L_{pp} and L_{gg} for the two types of grids are equal within the accuracy of the analysis. In contrast, due to the immediate proximity of the forward and return current lines in the paired grids, the mutual coupling L_{pg} is higher as compared to the interdigitated grids, as shown in Figs. 8 and 9. Therefore, the difference in loop inductance between paired and interdigitated grids is caused by the difference in the mutual inductance [13].

Note that although the inductance of a power distribution network (i.e., the inductance of the power-ground current loop) in the case of paired power grids is lower as compared to interdigitated grids, the signal self inductance (i.e., the inductance of the signal to the power/ground loop) as well as the inductive coupling of the signal lines is higher. The separation of the power/ground line pairs in paired grids is double the separation of the power and ground lines in interdigitated grids. The current loops formed between the signal lines and the power and ground lines are therefore larger in the case of paired grids. Interdigitated grids also provide enhanced capacitive shielding for the signal lines, as each power/ground line has the same number of signal neighbors as a power/ground line pair. Thus, a tradeoff exists between power integrity and signal integrity in the design

of high speed power distribution networks. In many circuits, the signal integrity is of primary concern, making interdigitated grids the preferred choice.

X. Dependence of Inductance on Grid Dimensions

The variation of grid inductance with grid dimensions, such as the grid length and width (assuming that the width and pitch of the grid lines is maintained constant) is considered in this section. The dependence of the grid loop inductance on the number of lines in the grid (i.e., the grid width) is discussed in Section X-A. The dependence of the grid loop inductance on the length of the grid is discussed in Section X-B. The concept of sheet inductance is described in Section X-C. A technique for efficiently and accurately calculating the grid inductance is outlined in Section X-D. The inductive properties of multilayer grids are discussed in Section X-E.

A. Dependence of Inductance on Grid Width

Apart from a lower loop inductance, the paired and interdigitated grids have an additional desirable property as compared to noninterdigitated grids. The loop inductance of paired and interdigitated grids varies inversely linearly with the number of lines as shown in Fig. 7. That is, for example, the inductance of a grid with ten power/ground line pairs is half of the inductance of a grid with five power/ground line pairs, all other factors being the same. For paired grids, this inversely linear dependence is exact (i.e., any deviation is well within the accuracy of the inductance extracted by FastHenry). For interdigitated grids, the inversely linear dependence is exact within the extraction accuracy at high numbers of power/ground line pairs. As the number of line pairs is reduced to two or three, the accuracy deteriorates to 5% to 8% due to the "fringe" effect. The electrical environment of the lines at the edges of the grid, where a line has only one neighbor, is significantly different from the environment within the grid, where a line has two neighbors. The fringe effect is insignificant in paired grids because the electrical environment of a line is dominated by the pair neighbor, which is physically much closer as compared to other lines in the paired grid.

As discussed in Section VI, the inductance of conductors connected in parallel decreases slower than inversely linearly with the number of conductors if inductive coupling of the parallel conductors is present. The inversely linear decrease of inductance with the number of lines may seem to contradict the existence of significant inductive coupling among the lines in a grid. This effect can be explained by (4). While the partial self inductance of the power and ground paths L_{pp} and L_{gg} indeed decreases slowly with the number of lines, so does the power to ground coupling L_{pg}, as shown in Figs. 8 and 9. The nonlinear behavior of L_{pp} and the nonlinear behavior of L_{pg} effectively cancel each other [see (4)], resulting in a loop inductance with an approximately inversely linear dependence on the number of lines [14].

From a circuit analysis point of view this behavior can be explained as follows. Consider a paired grid. The coupling of a distant line to a power line in any power/ground pair is nearly the same as the coupling of the same distant line to a ground line in the same pair due to the close proximity of the power and ground lines within each power/ground pair. The coupling to the power line counteracts the coupling to the ground line. As a result, the two effects cancel each other. Applying the same argument in the opposite direction, the effect of coupling a specific line to a power line is canceled by the line coupling to the ground line immediately adjacent to the power line. Similar reasoning is applicable to interdigitated grids, however, due to the equidistant spacing between the lines, the degree of coupling cancellation is lower. The lower degree of coupling cancellation is the cause of the aforementioned "fringe" effect.

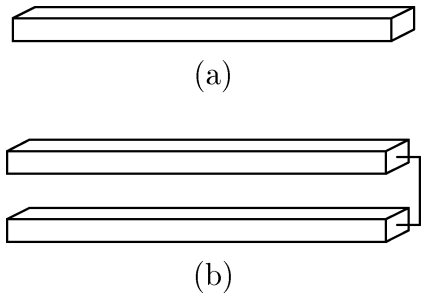

Fig. 10. Two structures under investigation to determine the dependence of inductance on the length of the structure. (a) A single straight line and (b) a complete current loop formed by two straight parallel lines.

B. Dependence of Inductance on Grid Length

The grid loop inductance is also found to increase linearly with grid length. The linear dependence of inductance on length is similar to the dependence of inductance on the number of lines [14].

The loop inductance of the grid increases essentially linearly with grid length, unlike the partial self inductance of a single line. The partial inductance of a straight line is a superlinear function of length. The partial self inductance of a rectangular line [see Fig. 10(a)] at low frequencies can be described by [20]

$$L_{\text{part}} = 0.2l\left(\ln\frac{2l}{T+W} + \frac{1}{2} - \ln\gamma\right)\ \mu\text{H} \qquad (5)$$

where T and W are the thickness and width of the line, and l is the length of the line. The $\ln\gamma$ term is a function of only the T/W ratio. This term is small as compared to the other terms (varying from 0 to 0.0025), and has a negligible effect on the variation of the inductance with length. This expression is an approximation, valid for $l \gg T + W$; a precise formula for round conductors can be found in [17]. This expression is a superlinear function of the line length l.

However, the loop inductance of a complete current loop formed by two parallel straight rectangular conductors (see Fig. 10(b)) is given by [20]

$$L_{\text{loop}} = 0.4l\left(\ln\frac{P}{H+W} + \frac{3}{2} - \ln\gamma + \ln k\right)\ \mu\text{H} \qquad (6)$$

where P is the distance between the center of the lines (the pitch) and $\ln k$ is a tabulated function of the H/W ratio. This simple expression is an approximation valid for long lines (i.e.,

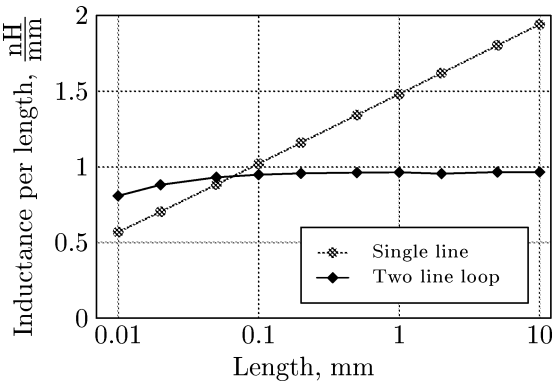

Fig. 11. Inductance per length versus line length for a single line (circles) and for a loop formed by two identical parallel lines. The line cross section is 1 μm $\times$ 1 μm.

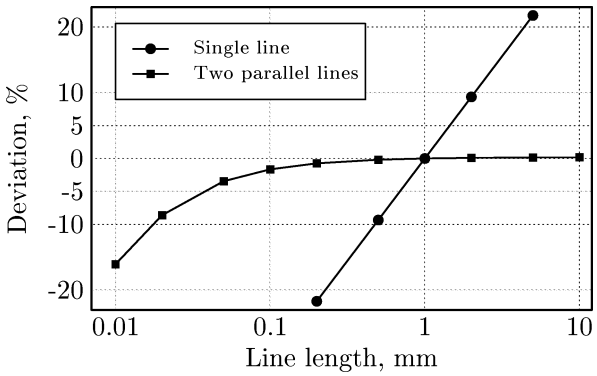

Fig. 12. Inductance per length versus line length in terms of the per cent difference from the inductance per length at a 1 mm length. The data is the same as shown in Fig. 11 but normalized to the value of inductance per length at 1 mm (0% deviation).

for $l \gg P$) and low frequencies (no skin or proximity effects). The expression is a linear function of the line length l.

To compare the dependence of inductance on length for both a single line and a complete loop and to assess the accuracy of the long line approximation assumed in (6), the partial inductance of a single line is analyzed along with the loop inductance of two identical parallel lines forming forward and return current paths. The cross section of the lines is 1 μm $\times$ 1 μm. The spacing between the lines in the complete loop is 4 μm. The length is varied from 10 μm to 10 mm.

The linearity of a function is difficult to visualize when the function argument spans three orders of magnitude (particularly when plotted in a semi-logarithmic coordinate system). The inductance per length, alternatively, is a convenient measure of the linearity of the inductance. The inductance per length (the inductance of the structure divided by the length of the structure) is independent of the length if the inductance is linear with length, and varies with length otherwise.

The inductance per length is therefore calculated for a single line and a two-line loop of various length. The results are illustrated in Fig. 11. The linearity of the data rather than the absolute magnitude of the data is of primary interest here. To facilitate the assessment of the inductance per length in relative terms, the data shown in Fig. 11 are recalculated as a per cent deviation from the reference value and are shown in Fig. 12. The inductance per length at a length of 1 mm is chosen as a reference. Thus, the inductance per length versus line length is plotted in Fig. 12 as a per cent deviation from the magnitude of the inductance per length at a line length of 1 mm. As shown in Fig. 12, the inductance per length of a single line changes significantly with length. The inductance per length of a complete loop is practically constant for a wide range of lengths (varying approximately 4% over the range from 50 μm to 10 000 μm). The inductance of a complete loop can, therefore, be considered linear when the length of a loop exceeds the loop width by approximately a factor of ten.

The linear dependence of grid inductance on the grid dimensions agrees well with recent work on power distribution grids in multi-chip modules (MCM) [2828]. A circuit model of a power distribution grid is heuristically constructed assuming a linear dependence of the inductance on the conductor length and includes inductive coupling only to the nearest neighbors. The impedance characteristics of MCM power distribution grids, as predicted by this model, agree well with experimental measurements [2828], confirming the validity of this approach.

C. Sheet Inductance of Power Grids

As has been discussed in this section, the inductance of grids with alternating power and ground lines is linearly dependent upon the grid length and number of lines. Furthermore, the grid inductance of interdigitated grids is relatively constant with frequency, as is described in Section XI. These properties of the grid inductance greatly simplify the procedure for evaluating the inductance of power distribution grids, permitting the efficient assessment of design tradeoffs.

The resistance of the grid increases linearly with grid length and decreases inversely linearly with grid width (i.e., the number of parallel lines). Therefore, the resistive properties of the grid can be conveniently described as a dimension independent grid sheet resistance $R_{\square}$, similar to the sheet resistance of an interconnect layer. The linear dependence of the grid inductance on the grid dimensions is similar to that of the grid resistance. As with resistance, it is convenient to express the inductance of a power grid as a dimension independent *grid sheet inductance* $L_{\square}$ (i.e., Henrys per square), rather than to characterize the grid inductance for a particular grid with specific dimensions. Thus,

$$L_{\square} = L_{\text{grid}} \cdot \frac{PN}{l} \tag{7}$$

where l is the grid length, P is the line (or line pair) pitch, and N is the number of lines (line pairs). This approach is analogous to the *plane* sheet inductance of two parallel power and ground planes (e.g., in a PCB stack), which depends only on the separation between the planes, not on the specific dimensions of the planes. Similarly, the grid sheet inductance reflects the overall structural characteristics of the grid (i.e., the line width and pitch) and is independent of the dimensions of a specific structure (i.e., the grid length and the number of lines in the grid). The sheet inductance is used as a dimension independent measure of the grid inductance in the discussion of power grid tradeoffs in Section XII.

D. Efficient Computation of Grid Inductance

The linear dependence of inductance on the grid length and width (i.e., the number of lines) has a convenient implication. The inductance of a large paired or interdigitated grid can be extrapolated with good accuracy from the inductance of a grid consisting of only a few power/ground pairs.

For an accurate extrapolation of the interdigitated grids, the line width and pitch of the original and extrapolated grids should be maintained the same. For example, for a grid consisting of $2N$ lines (i.e., N power-ground line pairs) of length l, width W, and pitch P, the inductance L_{2N} can be estimated as

$$L_{2N} \approx \frac{L_2}{N} \tag{8}$$

where L_2 is the inductance of a loop formed by two lines with the same dimensions and pitch. The inductance of a two-line loop L_2 can be calculated using (6). The power grid is considered to consist of uncoupled two-line loops. The accuracy of the approximation represented by (8) is about 10% for practical line geometries. Alternatively, the grid inductance L_{2N} can be approximated as

$$L_{2N} \approx L_4 \frac{2}{N} \tag{9}$$

where L_4 is the inductance of a power grid consisting of four lines of the original dimensions and pitch. A grid consisting of four lines can be considered as two coupled two-line loops connected in parallel. The loop inductance of a four-line grid can be efficiently calculated using (3) and (6). For practical geometries, a four-line approximation (9) offers an accuracy within 5% , as the coupling of the lines to nonneighbor lines is partially considered.

In paired grids, the effective inductive coupling among power/ground pairs is negligible and (8) is practically exact. The effective width of the current loop in paired grids is primarily determined by the separation between the power and ground lines within a pair. The spatial separation between pairs has (almost) no effect on the grid loop inductance. Expression (6) should be used with caution in estimating the inductance of adjacent power and ground lines. Expression (6) is accurate only for low frequencies and moderate W/T ratios; (6) does not describe proximity effects which take place in paired grids at high frequencies.

Alternatively, the grid sheet inductance $L_\square$ can be determined based on (8) and (9). For example, using (6) to determine the loop inductance of a line pair L_{pair}, the grid sheet inductance of a paired grid becomes

$$L_\square = L_{\text{pair}} \frac{P}{l} \approx 0.4P \left(\ln \frac{S}{H+W} + \frac{3}{2} \right) \frac{\mu\text{H}}{\square} \tag{10}$$

where P is the line pair pitch, and S is the separation between the line centers in the pair. The inductance of grids with the same line width and pitch is

$$L_{\text{grid}} = L_\square \cdot \frac{l}{PN}. \tag{11}$$

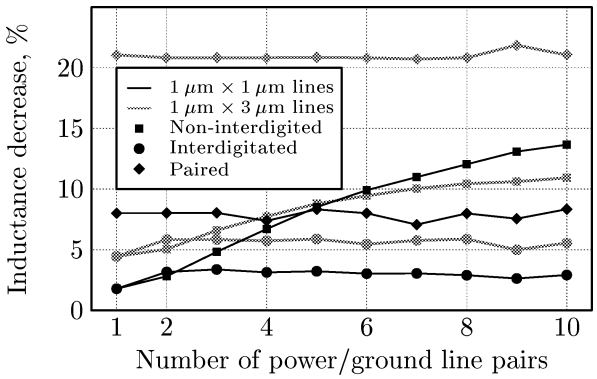

Fig. 13. Decrease in loop inductance with a change in frequency from 1 GHz to 100 GHz versus the number of P/G line pairs in the grid. The decrease is expressed as a per cent of the inductance at 1 GHz.

To summarize, the inductance of regular grids with alternating power and ground lines can be accurately estimated with analytic expressions.

E. Inductance of Multilayer Grids

On-chip power distribution networks are typically structured as a multilayer grid, i.e., a stack of several single-layer grids, each layer being orthogonal to the two neighboring layers. The inductive properties of these structures can be characterized based on the inductive properties of single-layer grids. The orthogonal lines have zero mutual partial inductance as there is no magnetic linkage. Orthogonal grids can therefore be evaluated independently. A multilayer grid can be considered to consist of two sets of layers, grid layers in one set being perpendicular to the layers in the other set. Grids in one of the directions only affect the grid inductance in this same direction, whereas grids in the perpendicular direction only affect the inductance in that direction. This behavior is analogous to the properties of grid resistance.

It can be shown that in most cases stacked grid layers have negligible magnetic coupling and behave as uncoupled inductors connected in parallel. However, the variation of multilayer grid inductance with frequency is more profound as compared to single layer grids due to current redistribution among the layers.

XI. Dependence of Inductance of Power Distribution Grids on Frequency

As mentioned in Section II, the circuit inductance decreases with frequency due to the skin effect, proximity effect, and the multipath current redistribution. The decrease in loop inductance for the three types of grid structures with 1 μm $\times$ 1 μm and 1 μm $\times$ 3 μm line cross sections operating at 100 GHz as compared to a frequency of 1 GHz is plotted in Fig. 13. Note that, as shown in Fig. 13, the inductance decreases with frequency. The difference between the high and low frequency loop inductance is less than 6% for paired grids with a 1 μm $\times$ 1 μm cross section and for interdigitated grids with both 1 μm $\times$ 1 μm and 1 μm $\times$ 3 μm cross sections. A change in inductance of this magnitude is insignificant for most digital applications since the circuit propagation delay is fairly insensitive to inductance as discussed in [27].

This relative independence of inductance with frequency is explained in the following way. In regular power grids with interdigitated power and ground lines (such as the interdigitated and paired grid structures discussed here), each line has the same resistance and inductance per length, and almost the same coupling to the rest of the grid (as discussed above in relation to the dependence of inductance on the number of lines). As a result, the distribution of current among grid lines at low frequencies (where the current flows through the path of lowest resistance) practically coincides with the current distribution at high frequencies (where the current flows through the path of lowest inductance) [15]. That is, the line resistance has a negligible effect on the distribution of current in the grid. Consequently, the decrease in inductance at high frequencies is caused by skin and proximity effects which only depend on the line size, spacing, and material resistivity. Such a decrease, as shown in Fig. 13, is typically insignificant. The grid inductance varies little with frequency unless several wide lines are placed in close proximity and carry very high frequency signals. This behavior is illustrated by the example of paired grids with wide 1 μm $\times$ 3 μm lines. In this case, the decrease in inductance is greater, approximately 22%, due to the proximity effect in adjacent wide lines.

In noninterdigitated grids, the decrease in loop inductance is limited to 11%, but increases with the number of lines in the grid. As the number of lines increases, the current distribution at low frequencies, uniform among the lines, changes at high frequencies, where the current crowds toward the central lines which provide the lowest inductance path.

XII. Inductance/Area/Resistance Tradeoffs

To investigate inductance tradeoffs in power distribution grids, the dependence of the grid inductance on line width is evaluated using FastHenry. Paired and interdigitated grids consisting of ten power/ground lines are investigated. A line length of 1000 μm and a line thickness of 1 μm are assumed. The minimum spacing between the lines S_0 is 0.5 μm. The line width W is varied from 0.5 μm to 5 μm.

Two tradeoff scenarios are considered in this section. The inductance versus resistance tradeoff under a constant grid area constraint in high performance power distribution grids is analyzed in Section XII-A. The inductance versus area tradeoff under a constant grid resistance constraint is analyzed in Section XII-B.

A. Inductance Versus Resistance Tradeoff Under a Constant Grid Area Constraint

In the first tradeoff scenario, the fraction of the metal layer area dedicated to the power grid, called the grid area ratio and denoted as A, is assumed fixed. The objective is to explore the tradeoff between grid inductance and resistance under the constraint of a constant area [16]. The area dedicated to the grid includes both the line width W and the minimum spacing S_0 necessary to isolate the power line from any neighboring lines; therefore, the grid area ratio can be expressed as $A = (W + S_0)/P$, where P is the line pitch.

The inductance of paired grids is virtually independent of the separation between the power/ground line pairs. The effective current loop area in paired grids is primarily determined by the line spacing within each power/ground pair, which is much smaller than the separation between the power/ground pairs [13]. Therefore, only paired grids with an area ratio of 0.2 (i.e., one fifth of the metal resources are allocated to the power and ground distribution) are considered here; the properties of paired grids with a different area ratio A (i.e., different P/G separation) can be linearly extrapolated. In contrast, the dependence of the inductance of the interdigitated grids on the grid line pitch is substantial, since the effective current loop area is strongly dependent upon the line pitch. Interdigitated grids with area ratios of 0.2 and 0.33 are analyzed here.

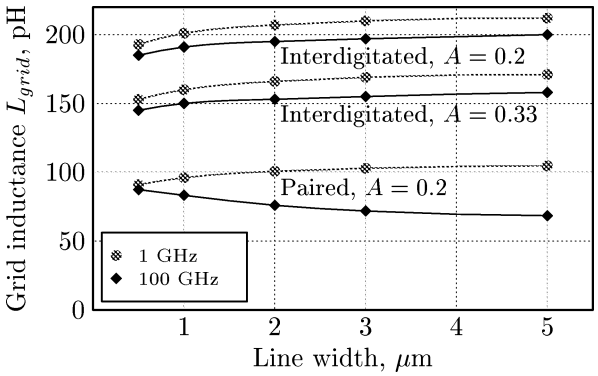

Fig. 14. The grid inductance versus line width under a constant grid area constraint for paired and interdigitated grids with ten P/G lines.

The grid inductance $L_{\rm grid}$ versus line width is shown in Fig. 14 for two signal frequencies: 1 GHz (the low frequency case) and 100 GHz (the high frequency case). The high frequency inductance is within 10% of the low frequency inductance for interdigitated grids, as mentioned previously. The large change in inductance for paired grids is due to the proximity effect in closely spaced, relatively wide lines.

With increasing line width W, the grid line pitch P (and, consequently, the grid width) increases accordingly so as to maintain the desired grid area ratio $A = (W+S_0)/P$. Therefore, the inductance of a grid with a specific line width cannot be directly compared to the inductance of a grid with a different line width due to the difference in the grid width. To perform a meaningful comparison of the grid inductance, the dimension specific data shown in Fig. 14 is converted to a dimension independent sheet inductance. The sheet inductance of a grid with a fixed area ratio A, $L_{\square}^{A}$, can be determined from $L_{\rm grid}$ through the following relationship:

$$L_{\square}^{A}(W) = L_{\rm grid}\,\frac{NP}{l} = L_{\rm grid}\,\frac{N}{l}\,\frac{W+S_0}{A} \qquad (12)$$

where N is the number of lines (line pairs), P is the line (line pair) pitch in an interdigitated (paired) grid, and l is the grid length. For each of the six $L_{\rm grid}$ data sets shown in Fig. 14, a correspondent $L_{\square}^{A}$ versus line width data set is plotted in Fig. 15. As illustrated in Fig. 15, the sheet inductance $L_{\square}^{A}$ increases with line width; this increase with line width can be approximated as a linear dependence with high accuracy.

The low frequency sheet resistance of a grid is $R_{\square} = \rho_{\square}(P/W)$. The grid resistance under a constant area ratio

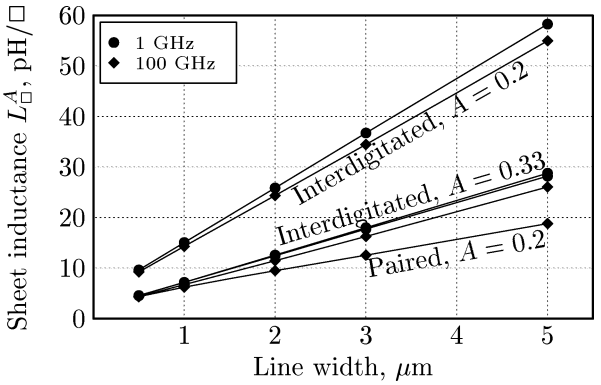

Fig. 15. The sheet inductance $L_{\square}^{A}$ versus line width under a constant grid area constraint.

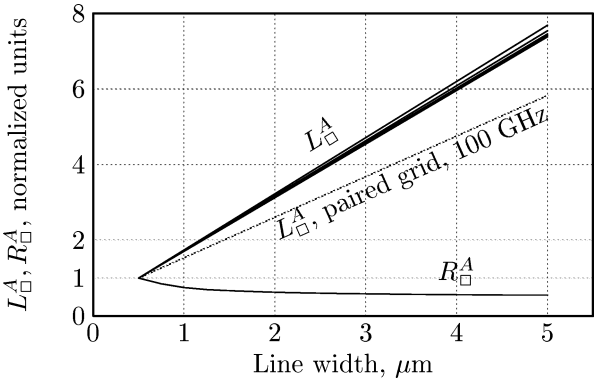

Fig. 16. Normalized sheet inductance and sheet resistance versus the width of the P/G line under a constant grid area constraint.

constraint, $A = (W + S_0)/P = \text{const}$, can be expressed as a function of only the line width W,

$$R_{\square}^{A} = \frac{\rho_{\square}}{A}\,\frac{W + S_0}{W}. \tag{13}$$

This expression shows that as the line width W increases from the minimum line width $W_{\min} = S_0$ ($(W + S_0)/W = 2$) to a large width ($W \gg S_0$, $(W + S_0)/W \simeq 1$), the resistance decreases twofold. An intuitive explanation of this result is that at the minimum line width $W_{\min} = S_0$, only half of the grid area used for power routing is filled with metal lines (the other half is used for line spacing) while for large widths $W \gg S_0$, almost all of the grid area is metal.

In order to better observe the relative dependence of the grid sheet inductance and resistance on the line width, $L_{\square}^{A}$ and $R_{\square}^{A}$ are plotted in Fig. 16 normalized to the respective values at a minimum line width of 0.5 μm (such that $L_{\square}^{A}$ and $R_{\square}^{A}$ are equal to one normalized unit at 0.5 μm). As shown in Fig. 16, five out of six $L_{\square}^{A}$ lines have a similar slope. These lines depict the inductance of a paired grid at 1 GHz and the inductance of two interdigitated grids ($A = 0.2$ and $A = 0.33$) at 1 GHz and 100 GHz. The line with a lower slope represents a paired grid at 100 GHz. This different behavior is due to pronounced proximity effects in closely placed wide lines with very high frequency signals.

The dependence of the grid sheet inductance on line width is virtually linear and can be accurately approximated by

$$L_{\square}^{A}(W) = L_{\square}^{A}(W_{\min}) \cdot \{1 + K \cdot (W - W_{\min})\} \tag{14}$$

where $L_{\square}^{A}(W_{\min})$ is the sheet inductance of the grid with a minimum line width and K is the slope of the lines shown in Fig. 16. Note that while $L_{\square}^{A}(W_{\min})$ depends on the grid type and area ratio (as illustrated in Fig. 15), the coefficient K is virtually independent of these parameters (with the exception of the special case of paired grids at 100 GHz).

The grid inductance increases with line width, as shown in Fig. 16. The inductance increases eightfold (sixfold for the special case of a paired grid at 100 GHz) for a tenfold increase in line width [16]. The grid resistance decreases nonlinearly with line width. As mentioned previously, this decrease in resistance is limited to a factor of two.

The inductance versus resistance tradeoff has an important implication in the case where at the minimum line width the peak power noise is determined by the resistive voltage drop IR, but at the maximum line width the inductive voltage drop $L(dI/dt)$ is dominant. As the line width decreases, the inductive $L(dI/dt)$ noise becomes smaller due to the lower grid inductance L while the resistive IR noise increases due to the greater grid resistance R, as shown in Fig. 16. Therefore, a minimum total power supply noise, $IR + L(dI/dt)$, exists at some target line width. The line width that produces the minimum noise depends upon the ratio and relative timing of the peak current demand I and the peak transient current demand dI/dt. The optimal line width is, therefore, application dependent. This tradeoff provides guidelines for choosing the width of the power grid lines that produces the minimum noise.

B. Inductance Versus Area Tradeoff Under a Constant Grid Resistance Constraint

In the second tradeoff scenario, the resistance of the power distribution grid is fixed (for example, by IR drop or electromigration constraints) [16]. The grid sheet resistance is

$$R_{\square} = \rho_{\square}\,\frac{P}{W} = \frac{\rho_{\square}}{M} = \text{const} \tag{15}$$

where $\rho_{\square}$ is the sheet resistivity of the metal layer and $M = W/P$ is the fraction of the area filled with power grid metal, henceforth called the metal ratio of the grid. The constant resistance $R_{\square}$ is equivalent to a constant grid metal ratio M. The constraint of a constant grid resistance is similar to that of a constant grid area except that the line spacings are not considered as a part of the grid area. The objective is to explore tradeoffs between the grid inductance and area under the constraint of a constant grid resistance. This analysis is conducted similarly to the analysis described in the previous subsection. The grid inductance L_{grid}^{R} versus line width is shown in Fig. 17. The corresponding sheet inductance $L_{\square}^{R}$ versus line width data set is plotted in Fig. 18. The normalized sheet inductance and grid area data, analogous to the data shown in Fig. 16, is depicted in Fig. 19.

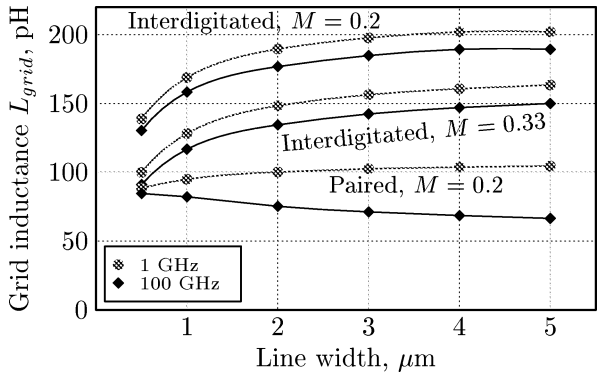

Fig. 17. The grid inductance versus line width under a constant grid resistance constraint for paired and interdigitated grids with ten P/G lines.

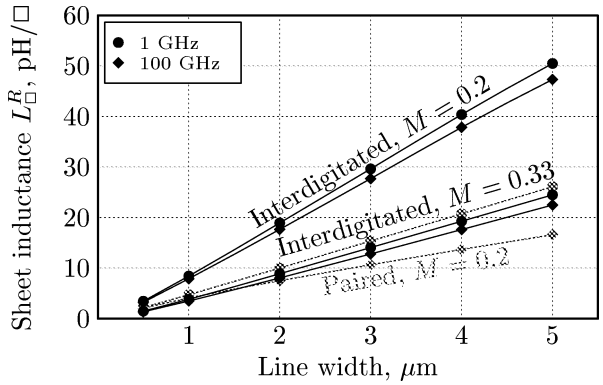

Fig. 18. The sheet inductance $L^R_\square$ versus line width under a constant grid resistance constraint.

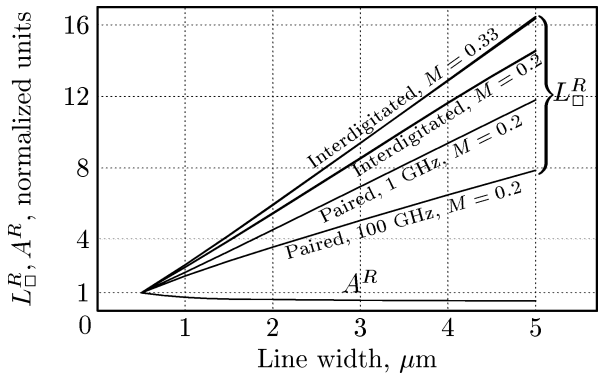

Fig. 19. Normalized sheet inductance $L^R_\square$ and the grid area ratio A^R versus the width of the P/G line under a constant grid resistance (i.e., constant grid metal ratio M) constraint.

As shown in Fig. 19, under a constant resistance constraint the grid inductance increases linearly with line width. Unlike in the first scenario, the slope of the inductance increase with line width varies with the grid type and grid metal ratio. Paired grids have the lowest slope and interdigitated grids with a metal ratio of 0.33 have the highest slope. The lower slope of the inductance increase with line width is preferable, as, under a target resistance constraint, a smaller area and/or a less inductive power network implementation can be realized. The slope of the inductance increase with line width is independent of frequency in interdigitated grids (the lines for 1 GHz and 100 GHz coincide and are not discernible in the figure), while in paired grids the slope decreases significantly at high frequencies (100 GHz) due to proximity effects. The inductance increase varies from eight to sixteen fold, depending on grid type and grid resistance (i.e., grid metal ratio), for a tenfold increase in line width. A reduction in the grid area is limited by a factor of two, similar to the decrease in resistance in the first tradeoff scenario.

XIII. Conclusion

The inductive characteristics of paired, interdigitated, and noninterdigitated power distribution grids are investigated in this paper. Paired grids are shown to have the lowest inductance as compared to interdigitated and noninterdigitated grids. The grid inductance is moderately dependent on the width of the power and ground lines. The inductance of grids with alternating power and ground lines is shown to vary linearly with grid length and to vary inversely linearly with the number of power/ground lines. Due to this linear dependence of grid inductance on the grid dimensions it is possible to express the inductive properties of the grids in a dimension independent form of sheet inductance. The inductance of the grids with alternating power and ground lines decreases relatively little with frequency; the decrease in inductance from 1 GHz to 100 GHz is less than 10% for most practical geometries. An efficient method for estimating the inductive characteristics of power distribution grids is proposed.

The inductance/area/resistance tradeoff in high performance power distribution grids is explored. Paired and interdigitated grids are investigated for two different tradeoff scenarios. In the first scenario, the inductance versus resistance tradeoff is investigated as the width of the grid lines is varied under a constant grid area constraint (including the necessary minimum spacing). In the second scenario, the inductance versus grid area tradeoff is investigated as the width of the grid lines is varied under a constant grid resistance constraint (i.e., constant metal area of the grid). The line width increases tenfold starting from a minimum width equal to the minimum line spacing. In both scenarios, the grid inductance increases linearly with line width, rising from eight to sixteen times for a tenfold increase in the line width. The grid resistance in the first scenario and the grid area in the second scenario decrease relatively slowly with line width. The decrease in grid resistance and grid area is limited to a factor of two in these two tradeoff scenarios.

This investigation provides guidelines for evaluating the interdependence of the inductance, area, and resistance in high performance power grids. These guidelines and criteria can be used to explore the design of high performance power distribution grids based upon application-specific slew rate, current, and power supply noise requirements.

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REFERENCES

[1] A. Deutsch *et al.*, "When are transmission-line effects important for on-chip interconnections?," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 1836–1846, Oct. 1997.

[2] Y. I. Ismail and E. G. Friedman, "Figures of merit to characterize the importance of on-chip inductance," *IEEE Trans. VLSI Syst.*, vol. 7, pp. 442–449, Dec. 1999.

[3] ——, *On-Chip Inductance in High Speed Integrated Circuits*. Norwell, MA: Kluwer Academic, 2001.

[4] M. Benoit, S. Taylor, D. Overhauser, and S. Rochel, "Power distribution in high-performance design," in *Proc. IEEE International Symposium on Low Power Electronics and Design*, Aug. 1998, pp. 274–278.

[5] L. C. Tsai, "A 1 GHz PA-RISC processor," in *Proc. IEEE International Solid-State Circuits Conference*, Feb. 2001, pp. 322–323.

[6] C. J. Anderson *et al.*, "Physical design of a fourth-generation POWER GHz microprocessor," in *Proc. IEEE International Solid-State Circuits Conference*, Feb. 2001, pp. 232–233.

[7] W. S. Song and L. A. Glasser, "Power distribution techniques for VLSI circuits," *IEEE J. Solid-State Circuits*, vol. SC-21, no. 1, pp. 150–156, Feb. 1986.

[8] L. Cao and J. P. Krusius, "A new power distribution strategy for area array bonded ICs and packages of future deep sub-micron ULSI," in *Proc. IEEE Electronic Components and Technology Conference*, June 1999, pp. 915–920.

[9] A. V. Mezhiba and E. G. Friedman, "Scaling trends of on-chip power distribution noise," in *Proc. ACM International Workshop on System Level Interconnect Prediction*, Apr. 2002, pp. 47–53.

[10] D. A. Priore, "Inductance on silicon for sub-micron CMOS VLSI," in *Proc. IEEE Symposium on VLSI Circuits*, May 1993, pp. 17–18.

[11] L.-R. Zheng and H. Tenhunen, "Effective power and ground distribution scheme for deep submicron high speed VLSI circuits," in *Proc. IEEE International Symposium on Circuits and Systems*, vol. 1, May 1999, pp. 537–540.

[12] K. Gala, V. Zolotov, R. Panda, B. Young, J. Wang, and D. Blaauw, "On-chip inductance modeling and analysis," in *Proc. IEEE/ACM Design Automation Conference*, June 2000, pp. 63–68.

[13] A. V. Mezhiba and E. G. Friedman, "Inductive characteristics of power distribution grids in high speed integrated circuits," in *Proc. IEEE International Symposium on Quality Electronic Design*, March 2002, pp. 316–321.

[14] ——, "Properties of on-chip inductive current loops," in *Proc. ACM Great Lake Symposium on Very Large Scale Integration*, Apr. 2002, pp. 12–17.

[15] ——, "Variation of inductance with frequency in high performance power distribution grids," in *Proc. IEEE International ASIC/SOC Conference*, Sept. 2002.

[16] ——, "Inductance/area/resistance tradeoffs in high performance power distribution grids," in *Proc. IEEE International Symposium on Circuits and Systems*, vol. I, May 2002, pp. 101–104.

[17] E. B. Rosa, "The self and mutual inductance of linear conductors," in *Bull. Nat. Bureau Standards*. Washington, DC: Government Printing Office, Jan. 1908, vol. 4, no. 2, pp. 301–344.

[18] E. B. Rosa and L. Cohen, "Formulæ and tables for the calculation of mutual and self-inductance," in *Bull. Nat. Bureau Standards*. Washington, DC: Government Printing Office, Aug. 1908, vol. 5, no. 1, pp. 1–132.

[19] E. B. Rosa and F. W. Grover, "Formulæ and tables for the calculation of mutual and self-inductance," in *Bull. Nat. Bureau Standards*. Washington, DC: Government Printing Office, Aug. 1912, vol. 8, no. 1, pp. 1–237.

[20] F. W. Grover, *Inductance Calculations: Working Formulas and Tables*. New York: Van Nostrand, 1946.

[21] A. E. Ruehli, "Inductance calculations in a complex integrated circuit environment," *IBM J. Res. Dev.*, vol. 16, no. 5, pp. 470–481, Sept. 1972.

[22] R. E. Matick, *Transmission Lines for Digital and Communication Networks*. New York: McGraw-Hill, 1969.

[23] M. Kamon, M. J. Tsuk, and J. White, "FastHenry: A multipole-accelerated 3-D inductance extraction program," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 1750–1758, Sept. 1994.

[24] D. Edelstein *et al.*, "Full copper wiring in a sub-0.25 μm CMOS ULSI technology," in *Proc. IEEE International Electron Device Meeting*, Dec. 1997, pp. 773–776.

[25] S. Venkatesan *et al.*, "A high performance 1.8 V 0.20 μm CMOS technology with copper metallization," in *Proc. IEEE International Electron Device Meeting*, Dec. 1997, pp. 769–772.

[26] Semiconductor Industry Association. (2000) International Technology Roadmap for Semiconductors, 2000 Update. [Online]. Available: http://public.itrs.net

[27] Y. I. Ismail and E. G. Friedman, "Sensitivity of interconnect delay to on-chip inductance," in *Proc. IEEE International Symposium on Circuits and Systems*, vol. 3, May 2000, pp. 403–406.

[28] Y. L. Low *et al.*, "Modeling and experimental verificatin of the interconnected mesh power system (IMPS) MCM topology," *IEEE Trans. Comp., Packag., Manufact. Technol.*, vol. 20, pp. 42–49, Feb. 1997.

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