# Simultaneous Switching Noise in On-Chip CMOS Power Distribution Networks

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*Abstract*—Simultaneous switching noise (SSN) has become an important issue in the design of the internal on-chip power distribution networks in current very large scale integration/ultra large scale integration (VLSI/ULSI) circuits. An inductive model is used to characterize the power supply rails when a transient current is generated by simultaneously switching the on-chip registers and logic gates in a synchronous CMOS VLSI/ULSI circuit. An analytical expression characterizing the SSN voltage is presented here based on a lumped inductive-resistive-capacitive $RLC$ model. The peak value of the SSN voltage based on this analytical expression is within 10% as compared to SPICE simulations. Design constraints at both the circuit and layout levels are also discussed based on minimizing the effects of the peak value of the SSN voltage.

*Index Terms*—Integrated circuit interconnection, on-chip inductance, power distribution network, simultaneous switching noise.

## I. INTRODUCTION

THE trend of next generation integrated circuit (IC) technology is toward higher speeds and densities. The total capacitive load associated with the internal circuitry is therefore increasing in both current and next generation very large scale integration (VLSI) circuits [1]–[3]. As the operating frequency increases, the average on-chip current required to charge (and discharge) these capacitances also increases, while the time during which the current being switched decreases. Therefore, a large change in the total on-chip current occurs within a short period of time.

The primary sources of the current surges are the input/output (I/O) drivers and the internal logic circuitry, particularly those gates that switch close in time to the clock edges. Because of the self-inductance of the off-chip bonding wires and the on-chip parasitic inductance inherent to the power supply rails, the fast current surges result in voltage fluctuations in the power supply network [4], which is called simultaneous switching noise (SSN) or delta-I noise.

Most existing research on SSN has concentrated on the transient power noise caused by the current through the inductive bonding wires at the I/O drivers [5]–[9]. However, SSN originating from the internal circuitry is becoming an important issue in the design of very deep submicrometer (VDSM) high-performance microprocessors [3], [10]. This increased importance can be attributed to fast clock rates, large on-chip switching activities, and large on-chip current, all of which are increas-
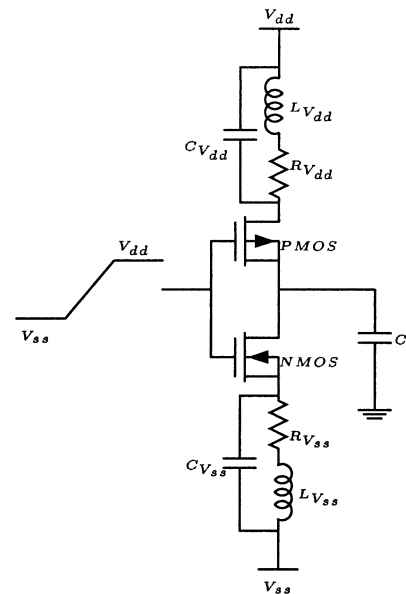
Fig. 1. An equivalent circuit for analyzing the SSN of an on-chip CMOS inverter.

ingly common characteristics of a VDSM synchronous integrated circuit.

For example, at gigahertz operating frequencies and high integration densities, power dissipation densities are expected to approach 20 W/cm$^2$[11], [12], a power density limit for an air-cooled packaged device. Such a power density is equivalent to 16.67 amperes of current for a 1.2 V power supply in a 0.1 $\mu$m CMOS technology. Assuming that the current is uniformly distributed along a 1-cm-wide and 1-$\mu$m-thick Al-Cu interconnect plane, the average current density is approximately 1.67 mA/$\mu$m$^2$. For a standard mesh structured power distribution network, the current density is even greater than 1.67 mA/$\mu$m$^2$. For a 1-mm-long power bus line with a parasitic inductance of 2 nH/cm [13], if the edge rate of the current signal is on the order of an overly conservative nanosecond, the amplitude of the $L\,di/dt$ noise is approximately 0.35 volts. This peak noise is not insignificant in VDSM CMOS circuits.

Therefore, on-chip SSN has become an important issue in VDSM integrated circuits. On-chip SSN affects the signal delay, creating delay uncertainty since the power supply level temporally changes the local drive current [14]. Furthermore, logic malfunctions may be created and excess power may be dissipated due to faulty switching if the power supply fluctuations are sufficiently large [15], [16]. On-chip SSN must therefore be controlled or minimized in high-performance integrated circuits.

Fig. 2.   SSN within a ground rail.



Fig. 3.   SSN voltage on the ground rail for a single switching logic gate with $L_{V_{ss}} = 2$ nH, $R_{V_{ss}} = 5 \; \Omega$, $C_{V_{ss}} = 0.1$ pF, $\tau_n = 29$ ps, and $\tau_r = 200$ ps.



Fig. 4.   SSN voltage on a ground rail for 500 simultaneously switching logic gates with $L_{V_{ss}} = 2$ nH, $R_{V_{ss}} = 5 \; \Omega$, $C_{V_{ss}} = 0.1$ pF, $\tau_n = 29$ ps, and $\tau_r = 200$ ps.
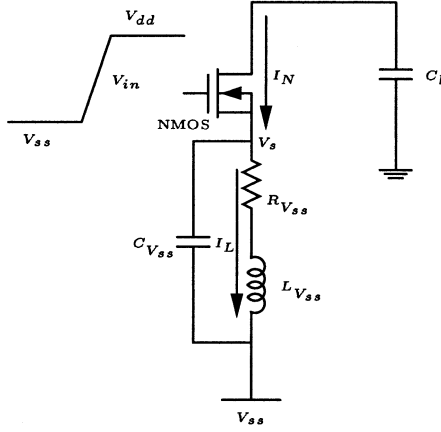
An analytical expression characterizing the on-chip SSN voltage is presented here based on a lumped $RLC$ model characterizing the on-chip power supply rails rather other a single inductor to model a bonding wire. The MOS transistors are characterized by the $n$th power law model [17], which is a more accurate device model than the Shichman–Hodges model for short-channel devices [18]. The SSN voltage predicted by the analytical expression is compared to SPICE. The waveform describing the SSN voltage is quite close to the waveform obtained from SPICE simulation. The peak value of the SSN is within 10% of SPICE.
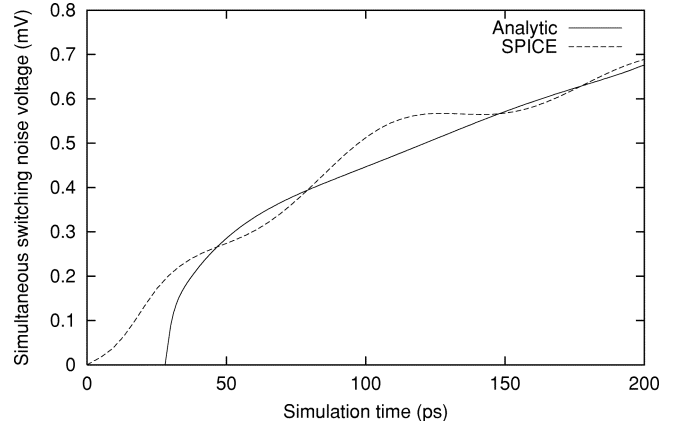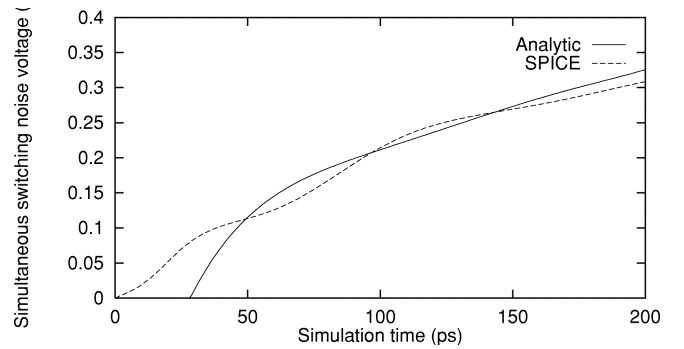
Circuit-level design constraints, such as the number of simultaneously switching logic gates connected to the same power supply rail, the drive current of the logic gates, the input transition time, and the magnitude of the power supply are related to the peak value of the SSN. For a specific parasitic inductive-resistive-capacitive $RLC$ impedance of the power supply rails, the analytical expressions presented here provide guidelines for designing the on-chip power distribution network.

An analytical expression of the on-chip SSN voltage is described in Section II. A discussion of the dependence of the on-chip SSN voltage on the load capacitance, and related circuit- and layout-level constraints are presented in Section III followed by some concluding remarks in Section IV.

## II. SIMULTANEOUS SWITCHING NOISE VOLTAGE

The power supply in high complexity CMOS circuits should provide sufficient current to support the average and peak power demand within all parts of an integrated circuit. An inductive, capacitive, and resistive model is used in this section to characterize the power supply rails when a transient current is generated by simultaneous switching of the on-chip registers and logic gates within a synchronous CMOS circuit. The short-channel MOS transistors are modeled as nonlinear devices and characterized by the $n$th power law model, which is more accurate than the alpha power law model in both the linear region and the saturation region [14].

A CMOS logic gate in this discussion is modeled as a CMOS inverter. The power supply rail is characterized by a lumped $RLC$ model. The input signal is assumed to be a fast ramp. The equivalent circuit depicted in Fig. 1 is used to characterize the SSN voltage on the power supply rails.

The current through the PMOS transistor with a rising input signal, i.e., the short-circuit current, is neglected in this discussion when determining the SSN voltage on a ground rail based on the assumption of a fast ramp input signal [19]. The equivalent circuit therefore simplifies to the circuit shown in Fig. 2. $L_{V_{ss}}$, $C_{V_{ss}}$, and $R_{V_{ss}}$ are the parasitic inductance, capacitance, and resistance of the ground rail, respectively. The input signal is

$$V_{in} = \frac{t}{\tau_r} V_{dd} \text{ for } 0 \leq t \leq \tau_r. \tag{1}$$

After the input voltage reaches $V_{TN}$, the NMOS transistor turns ON and begins to operate in the saturation region. It is assumed that the NMOS transistor remains in the saturation region before the input signal transition is completed.

The current through the NMOS transistor ($I_N$), the parasitic inductance ($I_L$), and the SSN voltage ($V_s$) are given, respectively, as

$$I_N = B_n (V_{in} - V_{TN} - V_s)^n \tag{2}$$

$$V_s = R_{V_{ss}} I_L + L_{V_{ss}} \frac{dI_L}{dt} \tag{3}$$
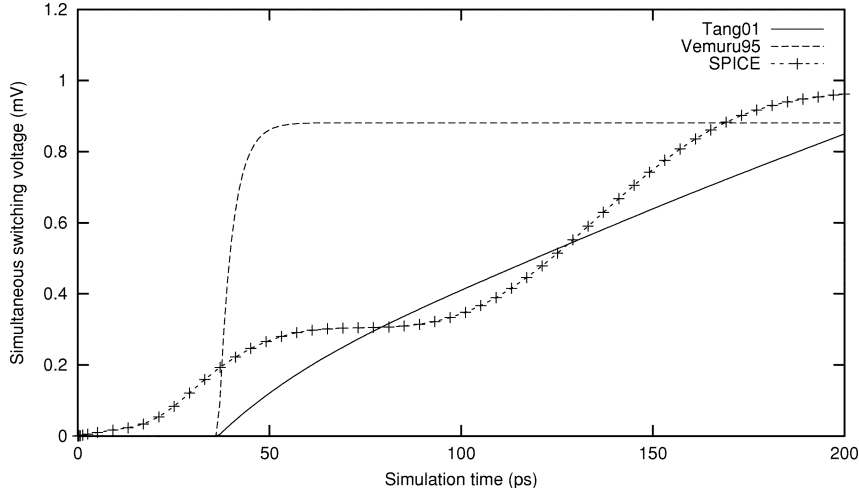
$$I_L = I_N - C_{V_{ss}} \frac{dV_s}{dt}. \tag{4}$$

Fig. 5. The simultaneous switching voltage on a power rail with $L_{V_{dd}} = 2$ nH, $R_{V_{dd}} = 5\ \Omega$, $C_{V_{dd}} = 0.2$ pF, $\tau_p = 39$ ps, and $\tau_r = 200$ ps.

Assuming that the magnitude of $V_s$ is small as compared to $V_{in} - V_{TN}$, $I_N$ can be approximated as

$$I_N \approx B_n(V_{in} - V_{TN})^n - \frac{dI_N}{dV_{GS}}V_s. \qquad (5)$$

Rewriting (5)

$$f_1 = \frac{dI_N}{dV_{GS}} = nB_n(V_{in} - V_{TN} - V_s)^{n-1}. \qquad (6)$$

$f_1$ is a function of $V_{GS}$, i.e., $V_{in}$ for the case of an inverter. In order to simplify the derivation, $f_1$ is approximated using $V_{in}$ equal to $0.5\ V_{dd}$.

Combining (4)–(6)

$$\begin{aligned}
L_{V_{ss}}C_{V_{ss}}&\frac{d^2V_s}{dt^2} + (R_{V_{ss}}C_{V_{ss}} + L_{V_{ss}}f_1)\frac{dV_s}{dt} \\
&+ (R_{V_{ss}}f_1 + 1)V_s \\
&\cong R_{V_{ss}}B_n(V_{in} - V_{TN})^n + L_{V_{ss}}\frac{d}{dt}[B_n(V_{in} - V_{TN})^n].
\end{aligned}$$
$$\qquad (7)$$

The first term on the left-hand side of (7) is neglected since the remaining two terms on the left-hand side of (7) dominate

$$\begin{aligned}
(R_{V_{ss}}C_{V_{ss}} &+ L_{V_{ss}}f_1)\frac{dV_s}{dt} + (R_{V_{ss}}f_1 + 1)V_s \\
&\cong R_{V_{ss}}B_nV_{dd}^n\left(\frac{t}{\tau_r} - \nu_n\right)^n + \frac{L_{V_{ss}}B_nV_{dd}^n}{\tau_r}\left(\frac{t}{\tau_r} - \nu_n\right)^{n-1}
\end{aligned}$$
$$\qquad (8)$$

where $\nu_n = V_{TN}/V_{dd}$. No closed-form solution of this differential equation exists due to the noninteger value of $n$ and $n - 1$. In order to derive an analytical expression for the differential equation, $(t/\tau_r - \nu_n)^n$ and $(t/\tau_r - \nu_n)^{n-1}$ are approximated by a polynomial expansion to the fifth order, where the average error is less than 3%

$$\begin{aligned}
\xi^n &\approx a_0 + a_1\xi + a_2\xi^2 + a_3\xi^3 + a_4\xi^4 + a_5\xi^5 \\
\xi^{n-1} &\approx b_0 + b_1\xi + b_2\xi^2 + b_3\xi^3 + b_4\xi^4 + b_5\xi^5
\end{aligned} \qquad (9)$$

where $\xi = t/\tau_r - \nu_n$. Note that $a_i$ and $b_i$ for $i = 0\ldots 5$ are independent of the input transition time $\tau_r$. The solution of the SSN voltage is

$$\begin{aligned}
V_s =&c_0(1 - e^{-(t-\tau_n)/\gamma\tau_r}) + c_1\xi + c_2\xi^2 + c_3\xi^3 + c_4\xi^4 \\
&+ c_5\xi^5 \text{ for } \tau_n \le t \le \tau_r
\end{aligned} \qquad (10)$$

where

$$\gamma = \frac{R_{V_{ss}}C_{V_{ss}} + L_{V_{ss}}f_1}{(R_{V_{ss}}f_1 + 1)\tau_r} \qquad (11)$$

$$\tau_n = \frac{V_{TN}}{V_{dd}}\tau_r = \nu_n\tau_r. \qquad (12)$$

These coefficients are

$$\begin{aligned}
c_0 =&A_0\gamma - A_1\gamma^2 + 2A_2\gamma^3 - 6A_3\gamma^4 + 24A_4\gamma^5 - 120A_5\gamma^6 \\
c_1 =&A_1\gamma - 2A_2\gamma^2 + 6A_3\gamma^3 - 24A_4\gamma^4 + 120A_5\gamma^5 \\
c_2 =&A_2\gamma - 3A_3\gamma^2 + 12A_4\gamma^3 - 60A_5\gamma^4 \\
c_3 =&A_3\gamma - 4A_4\gamma^2 + 20A_5\gamma^3 \\
c_4 =&A_4\gamma - 5A_5\gamma^2 \\
c_5 =&A_5\gamma.
\end{aligned} \qquad (13)$$

The $A_i$ for $i = 0\ldots 5$ are

$$A_i = \frac{R_{V_{ss}}B_nV_{dd}^n\tau_r}{R_{V_{ss}}C_{V_{ss}} + L_{V_{ss}}f_1}a_i + \frac{L_{V_{ss}}B_nV_{dd}^n}{R_{V_{ss}}C_{V_{ss}} + L_{V_{ss}}f_1}b_i \qquad (14)$$

where $a_i$ and $b_i$ are defined in (9). The SSN voltage reaches a maximum when the input voltage completes the transition, i.e., $t = \tau_r$

$$\begin{aligned}
V_{s,\max} =& c_0(1 - e^{-(\tau_r-\tau_n)/\gamma\tau_r}) + c_1\xi_r + c_2\xi_r^2 + c_3\xi_r^3 + c_4\xi_r^4 \\
&+ c_5\xi_r^5
\end{aligned} \qquad (15)$$

where $\xi_r = 1 - \nu_n$.

The SSN voltage on a ground rail as predicted by (10) is compared to SPICE in Fig. 3 for a single CMOS inverter with $W_n = 3.6\ \mu\text{m}$, $W_p = 7.2\ \mu\text{m}$, and $C_l = 1$ pF based on a $0.5\ \mu\text{m}$ CMOS technology. The solid line represents the analytical prediction and the dashed line represents the results from SPICE simulations. During the time period from $\tau_n$ to $\tau_r$, the analytical result agrees quite closely with SPICE (the error is less than 10%).

TABLE I
POLYNOMIAL EXPANSION COEFFICIENTS OF A 0.5 $\mu$m CMOS TECHNOLOGY

| Coef. | NMOS | | PMOS | |
|---|---|---|---|---|
| | $\xi^{n_n}$ | $\xi^{n_n-1}$ | $\xi^{n_p}$ | $\xi^{n_p-1}$ |
| 0th | -0.0023 | 0.2391 | -0.0008 | 0.0255 |
| 1st | 0.4132 | 3.9601 | 0.0777 | 2.2010 |
| 2nd | 1.4836 | -14.9465 | 1.4986 | -4.7503 |
| 3rd | -2.0667 | 31.7737 | -1.2056 | 9.0439 |
| 4th | 1.8168 | -32.4443 | 0.9537 | -8.8016 |
| 5th | -0.6502 | 12.5497 | -0.3262 | 3.3138 |



Fig. 6. The peak value of the SSN voltage with $L_{V_{ss}} = 2$ nH, $R_{V_{ss}} = 5$ $\Omega$, $C_{V_{ss}} = 0.1$ pF, and $\tau_r = 200$ ps.

This analysis is based on a single inverter. If $m$ simultaneously switching logic gates are connected to the same ground rail, the total SSN voltage can be obtained by substituting $mB_n$ for $B_n$ in (11) and (14). Note that all $c_i$ for $i = 0 \ldots 5$ are proportional to $m$, $1/\tau_r$, and $B_n$. Therefore, the SSN voltage increases with the number of simultaneous switching logic gates $m$, the input slew rate $1/\tau_r$, and the drive current of the logic gates $B_n$.

The analytical prediction of the SSN voltage for five hundred simultaneously switching CMOS inverters with $W_n = 3.6$ $\mu$m, $W_p = 7.2$ $\mu$m, and $C_l = 1$ pF is compared to SPICE in Fig. 4, exhibiting less than 7% error. During the time interval from $\tau_n$ to $\tau_r$, the analytical evaluation accurately models the results from SPICE simulations.

Similarly, the analytical expression for the SSN voltage on the power rail can be derived based on this same procedure. An estimate of the SSN voltage on the power rail based on the model presented in [8] is less accurate because an assumption that $n$ is close to one ($1 \leq n \leq 1.2$) is made. This assumption is appropriate for short-channel NMOS transistors, but the value of $n$ in a short-channel PMOS transistor is higher, typically in the range of 1.5 to 1.8 (it is 1.68 in the target 0.5 $\mu$m CMOS technology).

A comparison of the SSN voltage on the power rail is shown in Fig. 5. The effect of the carrier velocity saturation on a PMOS transistor is small as compared to an NMOS transistor. Therefore, the prediction based on the model presented in [8] cannot approximate the SSN voltage on the power rail as shown in Fig. 5. Note that the analytical expression presented here accurately predicts the SSN on the power rails. The coefficients for the polynomial expansion in (9) are listed in Table I with $n_n = 1.29$ and $n_p = 1.68$.

The peak value of the SSN as compared to SPICE is shown in Fig. 6 with $W_n = 1.8$ $\mu$m, $W_p = 3.6$ $\mu$m, and $C_l = 1.0$ pF. The dashed line represents the peak value of the predicted SSN based on the analytical expression described by (15). The dotted line describes the results derived from the SPICE simulations. The accuracy of the analytical prediction is within 10% as compared to SPICE. The peak SSN voltage based on (15) is compared to SPICE for different conditions, as illustrated in Tables II and III for both the ground and $V_{dd}$ rails, respectively, with $W_n = 1.8$ $\mu$m, $W_p = 3.6$ $\mu$m, and the input transition time $\tau_r = 200$ ps. Note that the maximum error of the analytical expression is within 10%.

## III. DISCUSSION
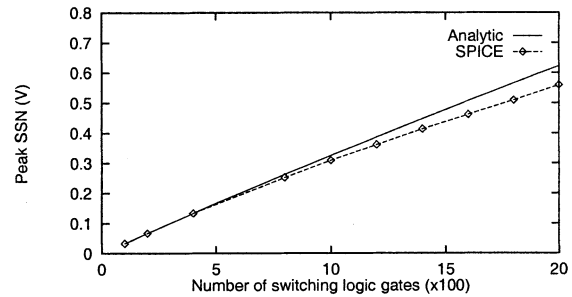
The dependence of the peak SSN voltage on the capacitive load is described in subsection $A$. Circuit- and layout-level constraints related to the peak SSN voltage are discussed in subsections $B$ and $C$, respectively.

### A. Capacitive Load

The NMOS transistor is assumed here to operate in the saturation region before the input transition is completed. This assumption depends upon the input transition time, the capacitive load, and the device transconductance. Vemuru notes in [8] that the peak value of the SSN voltage depends on the capacitive load.

The time when the NMOS transistor leaves the saturation region $\tau_{\text{sat}}$ is

$$\tau_{\text{sat}} = \frac{C_l}{B_n V_{dd}^n}(V_{dd} - V_{DSAT}) + \frac{\nu_n + n}{1 + n}\tau_r \qquad (16)$$

where $V_{DSAT} = K(V_{dd} - V_{TN})^m$ is the drain-to-source saturation voltage. If $\tau_{\text{sat}} \geq \tau_r$, the assumption that the NMOS transistor operates solely within the saturation region before the input transition is completed is appropriate. This constraint can be expressed as

$$C_l \geq \frac{(1 - \nu_n)B_n V_{dd}^n}{(1 + n)(V_{dd} - V_{DSAT})}\tau_r. \qquad (17)$$

The dependence of the peak SSN voltage on the load capacitance is shown in Fig. 7 with $W_n = 3.6$ $\mu$m and $W_p = 7.2$ $\mu$m. The right side of the vertical dashed line $C_l$, $i.e.$, Region II, satisfies the constraint defined by (17). The horizontal dashed line represents the analytically predicted peak simultaneous switching voltage. The accuracy of the analytical expression in Region II is within 10%. Therefore, if the load capacitance and the input transition time satisfy the constraint defined by (17), the analytical prediction accurately estimates the peak SSN voltage.

### B. Circuit-Level Constraints

The SSN voltage should be less than a target $V_c$ for a circuit to operate properly. Circuit design parameters, such as the input transition time $\tau_r$, the drive current of each logic gate $B_n$, and the number of simultaneously switching logic gates connected to the same power supply rail $m$, can be determined based on

$$V_{s,\text{max}}(m, B_n, \tau_r) \leq V_c \qquad (18)$$

where $V_{s,\text{max}}$ is defined in (15).

TABLE II
COMPARISON OF PEAK SSN VOLTAGE ON THE GROUND RAILS, NUM IS THE NUMBER OF SIMULTANEOUSLY SWICHING LOGIC GATES

| Power Rail | | | Number of switching logic gates | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| R | L | C | Peak SSN (V) ($m = 500$) | | | Peak SSN (V) ($m = 1000$) | | | Peak SSN (V) ($m = 1500$) | | |
| ($\Omega$) | (nH) | (pF) | Analytic | SPICE | $\delta$ (%) | Analytic | SPICE | $\delta$ (%) | Analytic | SPICE | $\delta$ (%) |
| 2.0 | 1.0 | 0.1 | 0.0802 | 0.0762 | 5.2 | 0.159 | 0.150 | 6.0 | 0.236 | 0.218 | 8.2 |
| | | 0.2 | 0.0802 | 0.0806 | 0.5 | 0.159 | 0.152 | 4.6 | 0.236 | 0.219 | 7.7 |
| | | 0.3 | 0.0801 | 0.0790 | 0.3 | 0.159 | 0.151 | 5.3 | 0.235 | 0.217 | 8.2 |
| | 2.0 | 0.1 | 0.143 | 0.141 | 1.4 | 0.282 | 0.265 | 6.4 | 0.417 | 0.381 | 9.4 |
| | | 0.2 | 0.143 | 0.137 | 4.3 | 0.282 | 0.263 | 7.2 | 0.417 | 0.380 | 9.7 |
| | | 0.3 | 0.142 | 0.138 | 2.9 | 0.281 | 0.260 | 8.0 | 0.415 | 0.378 | 9.8 |
| | 4.0 | 0.1 | 0.267 | 0.256 | 4.3 | 0.522 | 0.490 | 6.5 | 0.760 | 0.697 | 9.0 |
| | | 0.2 | 0.267 | 0.252 | 5.9 | 0.522 | 0.500 | 4.4 | 0.766 | 0.710 | 3.6 |
| | | 0.3 | 0.267 | 0.286 | 6.6 | 0.521 | 0.530 | 1.7 | 0.765 | 0.742 | 3.5 |
| 5.0 | 1.0 | 0.1 | 0.104 | 0.102 | 1.9 | 0.206 | 0.197 | 4.6 | 0.300 | 0.284 | 5.6 |
| | | 0.2 | 0.104 | 0.106 | 1.8 | 0.206 | 0.199 | 3.5 | 0.300 | 0.283 | 6.0 |
| | | 0.3 | 0.104 | 0.104 | 0.0 | 0.206 | 0.198 | 4.0 | 0.300 | 0.282 | 6.3 |
| | 2.0 | 0.1 | 0.167 | 0.165 | 1.2 | 0.320 | 0.310 | 3.2 | 0.470 | 0.438 | 7.3 |
| | | 0.2 | 0.167 | 0.162 | 3.1 | 0.320 | 0.308 | 3.9 | 0.470 | 0.436 | 7.7 |
| | | 0.3 | 0.166 | 0.153 | 8.5 | 0.319 | 0.302 | 5.6 | 0.469 | 0.434 | 8.0 |
| | 4.0 | 0.1 | 0.288 | 0.278 | 3.6 | 0.560 | 0.526 | 6.4 | 0.810 | 0.750 | 8.0 |
| | | 0.2 | 0.288 | 0.281 | 2.5 | 0.560 | 0.534 | 4.8 | 0.810 | 0.752 | 7.7 |
| | | 0.3 | 0.287 | 0.308 | 6.5 | 0.559 | 0.567 | 0.1 | 0.810 | 0.790 | 2.5 |
| Maximum error (%) | | | 8.5 | | | 8.0 | | | 9.8 | | |
| Average error (%) | | | 3.4 | | | 4.7 | | | 7.1 | | |

TABLE III
COMPARISON OF PEAK SSN VOLTAGE ON THE $V_{dd}$ RAILS, NUM IS THE NUMBER OF SIMULTANEOUSLY SWICHING LOGIC GATES

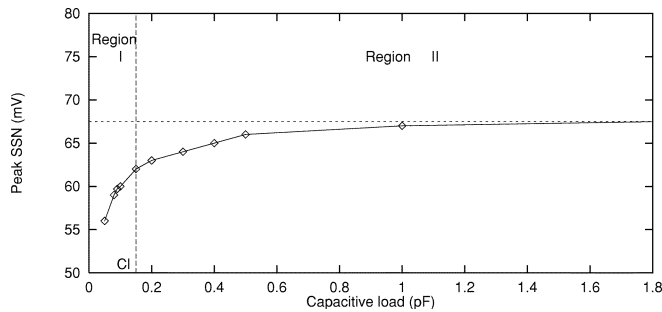| Power Rail | | | Number of switching logic gates | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| R | L | C | Peak SSN (V) ($m = 500$) | | | Peak SSN (V) ($m = 1000$) | | | Peak SSN (V) ($m = 1500$) | | |
| ($\Omega$) | (nH) | (pF) | Analytic | SPICE | $\delta$ (%) | Analytic | SPICE | $\delta$ (%) | Analytic | SPICE | $\delta$ (%) |
| 2.0 | 1.0 | 0.1 | 4.890 | 4.89 | 0.0 | 4.778 | 4.78 | 0.0 | 4.672 | 4.68 | 0.1 |
| | | 0.2 | 4.890 | 4.89 | 0.0 | 4.778 | 4.79 | 0.1 | 4.670 | 4.68 | 0.1 |
| | | 0.3 | 4.890 | 4.89 | 0.0 | 4.776 | 4.79 | 0.1 | 4.670 | 4.67 | 0.0 |
| | 2.0 | 0.1 | 4.794 | 4.81 | 0.3 | 4.599 | 4.63 | 0.6 | 4.412 | 4.47 | 1.3 |
| | | 0.2 | 4.793 | 4.79 | 0.1 | 4.598 | 4.61 | 0.4 | 4.412 | 4.47 | 1.3 |
| | | 0.3 | 4.794 | 4.79 | 0.1 | 4.600 | 4.61 | 0.1 | 4.410 | 4.46 | 1.3 |
| | 4.0 | 0.1 | 4.604 | 4.62 | 0.3 | 4.261 | 4.35 | 2.0 | 3.995 | 4.14 | 3.6 |
| | | 0.2 | 4.604 | 4.63 | 0.4 | 4.260 | 4.36 | 2.0 | 3.994 | 4.13 | 3.6 |
| | | 0.3 | 4.603 | 4.62 | 0.3 | 4.262 | 4.34 | 2.1 | 3.990 | 4.13 | 3.5 |
| 5.0 | 1.0 | 0.1 | 4.861 | 4.86 | 0.0 | 4.728 | 4.73 | 0.2 | 4.601 | 4.62 | 0.4 |
| | | 0.2 | 4.860 | 4.86 | 0.0 | 4.726 | 4.73 | 0.2 | 4.600 | 4.62 | 0.4 |
| | | 0.3 | 4.860 | 4.87 | 0.0 | 4.726 | 4.74 | 0.3 | 4.600 | 4.61 | 0.4 |
| | 2.0 | 0.1 | 4.770 | 4.78 | 0.2 | 4.554 | 4.59 | 0.8 | 4.351 | 4.42 | 1.6 |
| | | 0.2 | 4.771 | 4.78 | 0.2 | 4.552 | 4.59 | 0.8 | 4.350 | 4.41 | 1.5 |
| | | 0.3 | 4.770 | 4.76 | 0.2 | 4.552 | 4.58 | 0.8 | 4.350 | 4.42 | 1.6 |
| | 4.0 | 0.1 | 4.692 | 4.61 | 1.8 | 4.224 | 4.32 | 2.3 | 3.900 | 4.10 | 9.2 |
| | | 0.2 | 4.690 | 4.61 | 1.7 | 4.220 | 4.32 | 2.3 | 3.905 | 4.11 | 9.3 |
| | | 0.3 | 4.690 | 4.60 | 1.7 | 4.220 | 4.31 | 2.1 | 3.905 | 4.12 | 9.3 |
| Maximum error (%) | | | 1.8 | | | 2.3 | | | 9.3 | | |
| Average error (%) | | | 0.4 | | | 1.0 | | | 2.8 | | |



Fig. 7. Dependence of the peak SSN voltage on the load capacitance with $\tau_r = 200$ ps.

For example, the maximum number of simultaneously switching logic gates connected to the same power supply rail can be determined based on this constraint. Assume that $V_c = V_{TN} = 0.75$ V. The maximum number of switching logic gates for different conditions is shown in Fig. 8. $C1$ is the condition of $\tau_r = 200$ ps and $W_n = 3.6$ $\mu$m, $C2$ is the condition of $\tau_r = 400$ ps and $W_n = 3.6$ $\mu$m, and $C3$ is the condition of $\tau_r = 200$ ps and $W_n = 1.8$ $\mu$m. $N1 = 1200$, $N2 = 2000$, and $N3 = 2300$ are the maximum number of switching logic gates for each case, respectively.

The on-chip SSN voltage results from the parasitic inductance of the power rails and the large current surges within a short period of time. Therefore, the peak SSN voltage increases as the input transition time decreases. The constraint of the input transition time is shown in Fig. 9 for different number of simultaneously switching gates, e.g., 1000, 1500, and 2000 with $L_{V_{ss}} = 2$ nH, $R_{V_{ss}} = 5$ $\Omega$, $C_{V_{ss}} = 0.1$ pF, and $W_n = 1.8$ $\mu$m.

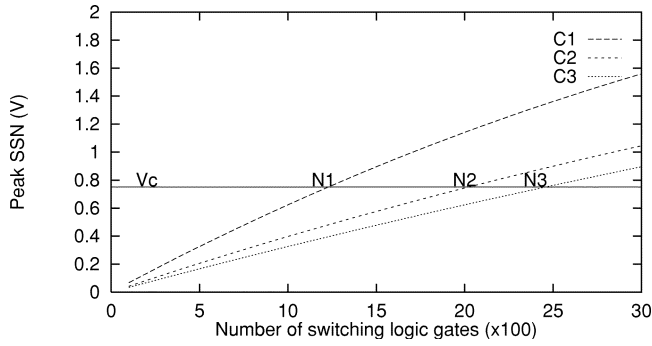Fig. 8. The maximum number of simultaneously switching logic gates with $L_{V_{ss}} = 2$ nH, $R_{V_{ss}} = 5$ $\Omega$, and $C_{V_{ss}} = 0.1$ pF. $V_c$ is the voltage target, $C1$: $\tau_r = 200$ ps, $W_n = 3.6$ $\mu$m, $C2$: $\tau_r = 400$ ps, $W_n = 3.6$ $\mu$m, and $C3$: $\tau_r = 200$ ps, $W_n = 1.8$ $\mu$m.
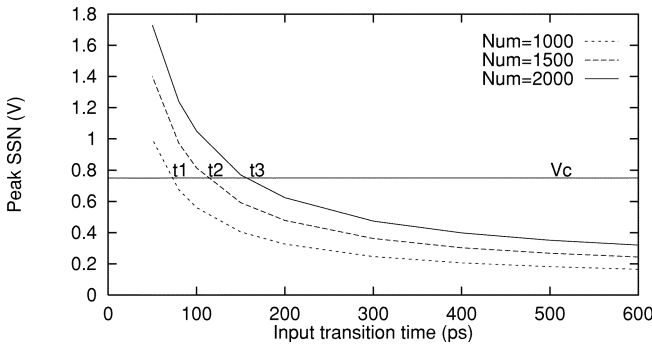


Fig. 9. Peak SSN as a function of the input transition time. Note the limiting constraints on the input transition time for different number of simultaneously switching gates, Num $= 1000$, $1500$, and $2000$.

$t1 = 85$ ps, $t2 = 115$ ps, and $t3 = 180$ ps are the limits of the input transition times for each condition, respectively. If the number of simultaneously switching logic gates increases, the input slew rate $(1/\tau_r)$ should be decreased in order to decrease the maximum SSN voltage. The peak noise values for different input transition times with $L_{V_{ss}} = 1$ nH, $R_{V_{ss}} = 5$ $\Omega$, and $C_{V_{ss}} = 0.1$ pF are listed in Table IV, note that for a very short input transition time, i.e., 20 ps, the analytical model still provides an accurate estimation of the peak noise. The analytical error is within 8% as listed in Table IV.

Also note that the SSN voltage is proportional to the $n$th power of the supply voltage ($V_{dd}^n$). Therefore, the normalized simultaneous switching voltage $V_s/V_{dd}$ is proportional to the ($n-$1th) power of the supply voltage ($V_{dd}^{n-1}$), permitting the supply voltage to be reduced in order to decrease the SSN voltage. The dashed line shown in Fig. 10 represents the normalized peak value of the SSN voltage $V_{s,\max}/V_{dd}$ and the solid line represents the absolute value of the peak SSN.

### C. Layout-Level Constraints

The peak SSN can be controlled by reducing the parasitic inductance of the power supply rails. The parasitic inductance $L$, resistance $R$, and capacitance $C$ of the power supply rails can be determined from the physical geometries of the layout, i.e., the width ($w$), thickness ($h$), length ($l$), and spacing ($s$) of the power supply rails.

$$V_{s,\max}(R, L, C) = V_{s,\max}(w, h, l, s) \leq V_c. \tag{19}$$

TABLE IV
PEAK SSN FOR SHORT INPUT TRANSITION TIMES

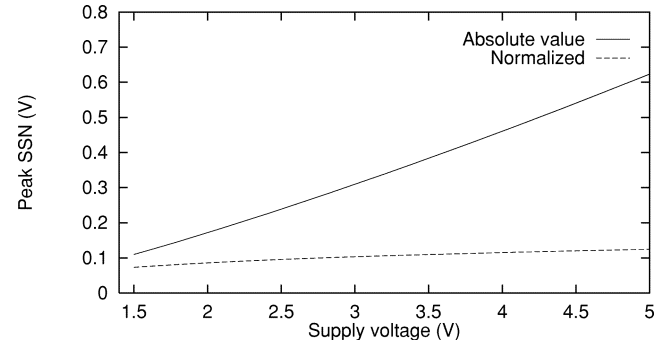| Transition time | $m = 500$ | | | $m = 1000$ | | |
|---|---|---|---|---|---|---|
| $\tau$ (ps) | SPICE (V) | Analytic (V) | Error (%) | SPICE (V) | Analytic (V) | Error (%) |
| 150 | 0.123 | 0.125 | 1.6 | 0.230 | 0.246 | 6.96 |
| 100 | 0.166 | 0.166 | <1.0 | 0.3155 | 0.325 | 3.17 |
| 80 | 0.194 | 0.917 | 1.55 | 0.371 | 0.384 | 3.50 |
| 50 | 0.312 | 0.288 | 7.69 | 0.570 | 0.559 | 1.93 |
| 20 | 0.715 | 0.658 | 7.97 | 1.17 | 1.18 | 0.85 |
| Maximum error (%) | | | | 7.97 | | |
| Average error (%) | | | | 3.54 | | |



Fig. 10. Dependence of the peak value of the SSN on the power supply with $m = 10$, $L_{V_{ss}} = 2$ nH, $R_{V_{ss}} = 5$ $\Omega$, $C_{V_{ss}} = 0.1$ pF, and $\tau_r = 200$ ps.
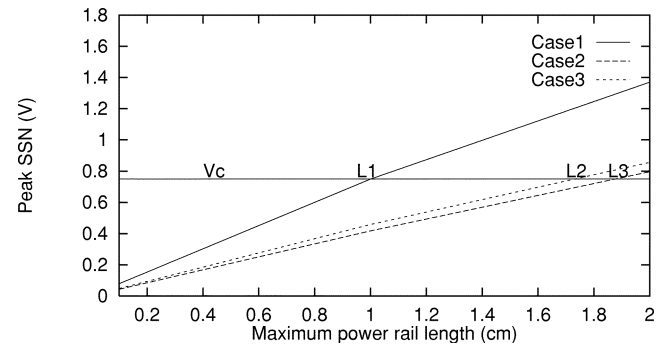


Fig. 11. Peak SSN as a function of the length of the power rails. Note the limiting constraints on the length of the power rails with 1500 simultaneously switching logic gates. Case 1: $L_{V_{ss}} = 2$ nH/cm, $R_{V_{ss}} = 1$ $\Omega$/cm, and $C_{V_{ss}} = 0.1$ pF/cm, Case 2: $L_{V_{ss}} = 1$ nH/cm, $R_{V_{ss}} = 2$ $\Omega$/cm, and $C_{V_{ss}} = 0.1$ pF/cm, and Case 3: $L_{V_{ss}} = 1$ nH/cm, $R_{V_{ss}} = 4$ $\Omega$/cm, and $C_{V_{ss}} = 0.1$ pF/cm.

Extraction of the parasitic $RLC$ impedance of the on-chip interconnect is currently an important research topic [20]–[22]. However, if compact models characterizing the parasitic impedance of the power supply rails are available, guidelines such as presented in (19) for designing the on-chip power distribution network can be developed. By combining both of the constraints represented by (18) and (19), the peak SSN voltage for a circuit to operate properly can be determined.

The parasitic inductance of the power rails is proportional to the length of the power rails. Even though the dependence of the parasitic inductance on $w$, $h$, and $s$ are not available, the length of the power rail can be determined based on the parasitic impedance per unit length. The constraint of the power rail length is shown in Fig. 11 for different conditions assuming 1500 simultaneously switching logic gates. $l1 = 0.98$ cm, $l2 =$

1.87 cm, and $l3 = 1.74$ cm are the length limits for each condition in this case, respectively.

## IV. CONCLUSION

An analytical expression characterizing the SSN voltage in VDSM CMOS circuits is presented in this paper. This expression provides a method for evaluating SSN voltage at the system level. The analytically derived waveform characterizing the on-chip SSN voltage is quite close to SPICE. The predicted peak on-chip SSN voltage based on the analytical expression is within 10% as compared to SPICE. Circuit- and layout-level design constraints for the power distribution network have also been briefly discussed.

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