Power Characteristics of Inductive Interconnect

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***Abstract*—The width of an interconnect line affects the total power consumed by a circuit. The effect of wire sizing on the power characteristics of an inductive interconnect line is presented in this paper. The matching condition between the driver and the load affects the power consumption since the short-circuit power dissipation may decrease and the dynamic power will increase with wider lines. A tradeoff, therefore, exists between short-circuit and dynamic power in inductive interconnects. The short-circuit power increases with wider linewidths only if the line is underdriven. The power characteristics of inductive interconnects therefore may have a great influence on wire sizing optimization techniques. An analytic solution of the transition time of a signal propagating along an inductive interconnect with an error of less than 15% is presented. The solution is useful in wire sizing synthesis techniques to decrease the overall power dissipation. The optimum linewidth that minimizes the total transient power dissipation is determined. An analytic solution for the optimum width with an error of less than 6% is presented. For a specific set of line parameters and resistivities, a reduction in power approaching 80% is achieved as compared to the minimum wire width. Considering the driver size in the design process, the optimum wire and driver size that minimizes the total transient power is also determined.**

***Index Terms*—Characteristic impedance, dynamic power, inductive interconnect, short-circuit power, transient power dissipation, underdamped systems.**

I. Introduction

With the decrease in feature size of CMOS integrated circuits, interconnect design has become an important issue in high speed, high complexity integrated circuits (IC). With increasing signal frequencies and the corresponding decrease in signal transition times, the interconnect impedance can behave inductively [1], increasing the on-chip noise. Furthermore, considering inductance within the design process increases the computational complexity of IC synthesis and analysis tools. However, inductive behavior can also be exploited. As shown in [2], a properly designed inductive line can reduce the total power dissipation of high speed clock distribution networks. Furthermore, on-chip inductance may affect certain design techniques such as repeater insertion [3], [4]. Clock distribution networks can dissipate a large portion of the total power dissipated within a synchronous IC, ranging from 25% to as high as 70% [5]–[7]. The technique proposed here can be used to reduce the overall power being dissipated by long nets such as a high speed clock distribution network.

On-chip interconnect now dominates the circuit delay and power dissipation characteristics of high performance ICs. Interconnect design has, therefore, become an important issue in the IC design process. Many algorithms have been proposed to determine the optimum wire size that minimizes a target cost function. Some of these algorithms address reliability issues by reducing clock skew. Most of the previous work concentrate on minimizing delay [8]–[13]. Simultaneous driver and wire sizing is presented in [13]–[15] as an efficient technique to design an optimum interconnect network with minimum propagation delay.

The work described in [14] and [15] considers power dissipation as a cost function in the delay optimization process. The power minimization criterion used in these previous techniques [14], [15] minimizes the interconnect and gate area in order to reduce the capacitance of both the passive interconnects and active gates, thereby reducing dynamic power. The dynamic power dissipated in the load capacitance represents a large portion of the total transient power dissipated in a digital circuit. As shown in [2], however, the short-circuit power of some digital circuits may exceed the dynamic power. As described in [2], on-chip inductance can improve circuit speed while reducing the short-circuit power dissipation. Wire sizing can increase the inductive behavior of the signal, possibly lowering the total power dissipated by a circuit. The interconnect inductance should, therefore, be included in the power minimization process.

Buffers and repeaters are widely used in interconnect networks (e.g., clock distribution networks) for different design objectives (e.g., reducing delay or clock skew). Wider wires are used in [2] to reduce power dissipation while neglecting the effect of the line driver on the signal characteristics. It is shown in this paper that this technique may, in certain cases, actually increase power dissipation. The width of the interconnect also affects other impedance parameters which can change the signal characteristics, leading to nonoptimal circuits.

As interconnect inductance becomes important, specific wire sizing optimization algorithms have been enhanced that consider RLC impedance models [16]–[19]. Previous studies in wire and driver sizing do not consider changes in the signal characteristics accompanied with a change in the line impedance characteristics. The interconnect impedance characteristics are more sensitive to wire size in long, inductive interconnects. The research described in [17] considers line inductance, however, the optimization criteria minimize delay using an unrealistic inductance model and do not consider power dissipation. The work described in [20]–[22] considers dynamic power dissipation while ignoring the short-circuit power of the load gate. The work described in [14], [15] considers power dissipation while

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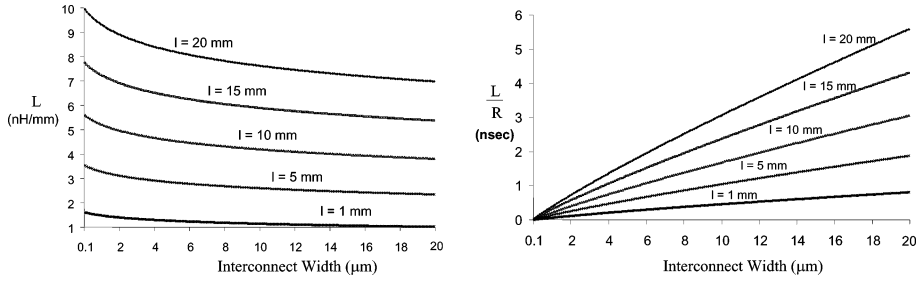

Fig. 1. Inductive interconnect characteristics versus width for different lengths (a) self-inductance and (b) inductive time constant.

ignoring the inductive behavior of the interconnect and, therefore, the effect of line inductance on the power characteristics.

In this paper, the power characteristics of an inductive interconnect are presented. No repeaters are assumed along the line. Repeaters can be used to reduce the signal propagation delay. Inserting repeaters, however, is not always practical. Furthermore, repeaters dissipate power and increase the area of the circuit. The power characteristics of a long, inductive interconnect driven by a repeater system are described in [23]. In this paper, the effect of sizing an inductive interconnect on the signal characteristics is described. It is shown that the signal characteristics of an inductive interconnect line are sensitive to changes in the linewidth. As the short-circuit power depends directly on the signal transition time, the effect of sizing an inductive interconnect line on the signal transition time is discussed.

An analytic solution for the transition time at the far end of a long inductive interconnect is provided. These results are used to determine an analytic solution for the width of an inductive interconnect line that minimizes the total transient power dissipation. A tradeoff between short-circuit and dynamic power in inductive interconnect is introduced.

The line driver has a significant effect on the signal and power dissipation characteristics. It is shown in this paper that simultaneous sizing of the driver and the line is important to minimize the total power dissipation. An analytic solution for the simultaneous driver and wire sizing problem that minimizes the total transient power dissipation assuming an RLC line is presented. The paper is organized as follows. In Section II, the transient power characteristics of an inductive interconnect line are discussed and a power optimization criterion is formulated. The signal behavior at the far end of an inductive line is described in Section III. The effect of line material and length on the signal characteristics of an inductive line is discussed in Section IV. In Section V, circuit simulations are used to demonstrate the accuracy of the analytic solutions for the transition time and the optimum linewidth. Additional results are provided that compare the power of an optimally sized line for different interconnect materials and lengths. Some conclusions are discussed in Section VI.

II. Transient Power Characterization

The transient power characteristics of inductive interconnect are discussed in this section. The research described in [2] uses the concept of wire sizing to reduce the total transient power dissipated by a clock distribution network, but does not provide an analytic solution to determine the optimum interconnect width. The change in circuit behavior that occurs when the width of the line is increased is also ignored in [2]. The matching response between the line and the driver plays an important role in the transient power dissipation as discussed in Section III. In [2], the driver size is also not considered as a design variable.

Issues that affect wire sizing are discussed in this section. The effects of wire sizing on the line impedance characteristics are discussed in Section II-A. In Section II-B, the tradeoff between dynamic and short-circuit power dissipation in inductive interconnect is described. Transient power optimization criteria are presented in Section II-C.

A. Effect of Wire Sizing on Interconnect Line Impedance Characteristics

Neglecting the dielectric losses of the line, a lossy transmission line can be represented by the line resistance R, inductance L, and capacitance C, all per unit length. R is expressed in terms of the line dimensions

$$R = \frac{\rho}{W_{\rm INT}\, T} \tag{1}$$

where ρ, T, and $W_{\rm INT}$ are the line resistivity, thickness, and width, respectively. C is expressed in terms of the line dimensions for different line structures in [31]. Note that C increases with the linewidth, which increases the dynamic power P_{1d}.

An expression for the line inductance requires information characterizing the current return paths. For an interconnect shielded by two ground lines, a closed form expression for the line inductance in terms of the line dimensions and the separation between the line and the ground lines is obtained from [32]. This shielded structure is commonly used in high speed clock distribution networks [33]–[37] and many global interconnects. For a fixed separation between the signal and shield line, the total line inductance primarily depends on the self-inductance of the line. The line self-inductance decreases monotonically with increasing linewidth. The line inductance decreases with increasing linewidth, as shown in Fig. 1(a).

The ratio L/R characterizes the significance of the line inductance [3]. For different line lengths, this ratio increases with wider lines as shown in Fig. 1(b). The reduction in line resistance is greater than the reduction in line inductance. An increase in the ratio L/R and the interconnect capacitance affects the transition time as described in Section III.

Not only the line dimensions but also the switching frequency increase the importance of considering the line inductance. A

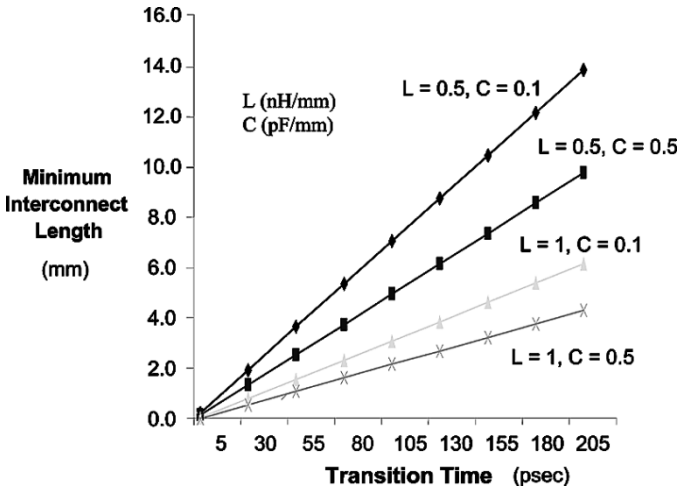

Fig. 2. Lower limit on the interconnect length above which the line inductance should be considered.

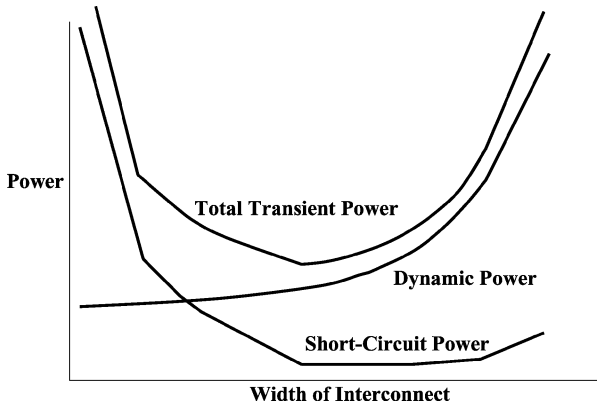

Fig. 3. Dynamic, short-circuit, and total transient power as a function of the interconnect linewidth.

higher clock frequency typically implies shorter signal transition times. Shorter transition times increase the number of on-chip interconnects that behave inductively. As shown in [1], for line lengths $l > t_r/\sqrt{LC}$ where t_r is the signal transition time, the inductance of the line should be considered in the interconnect model.

The limit on the interconnect length that produces inductive behavior is shown in Fig. 2. If the interconnect is longer than this limit, the line inductance should be considered in the line model [1]. For shorter signal transition times, the limit decreases for any value of line capacitance and inductance per unit length (as shown in Fig. 2). This characteristic increases the number of interconnect lines which behave inductively and increases the importance of line inductance to accurately characterize the signal behavior.

B. Transient Power of Inductive Lines

The power dissipation is affected by a change in linewidth as described in this section. A tradeoff exists between dynamic and short-circuit power in sizing inductive interconnect. The dependence of the power dissipation on the interconnect width is illustrated in Fig. 3 [24]–[26]. As the line inductance-to-resistance ratio increases, the short-circuit power decreases with

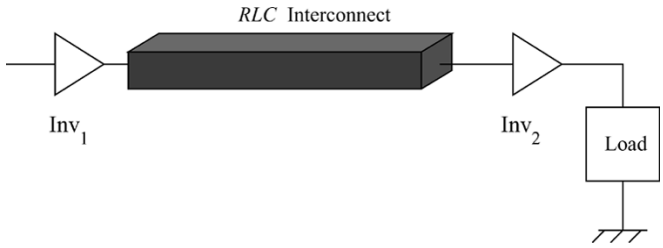

Fig. 4. CMOS gates connected by an RLC interconnect line.

wider interconnect. If the interconnect exceeds a certain width, the short-circuit power increases. The dynamic power increases with linewidth as the line capacitance increases. As shown in Fig. 3, an optimum interconnect width at which the total transient power is a minimum exists for overdriven lines. This tradeoff does not occur if the line is underdriven, as described in Section III.

For the circuit shown in Fig. 4, a long interconnect line between two CMOS inverters can be modeled as a lossy transmission line. A change in the linewidth primarily affects the dynamic power P_{1d} of Inv_1, and the short-circuit power $P_{2\mathrm{sc}}$ of Inv_2. The dynamic power of Inv_2 depends on the load capacitance, and is not affected by the wire size. The change in the short-circuit power of Inv_1 is negligible, assuming a fixed signal transition time at the input of Inv_1. For a large driver driving a long line (large capacitive load), the short-circuit power of the driver is only about 2% of the total power dissipation of the driver. For a change in the linewidth from 0.1 to 20 μm, the dynamic power of the driver increases by 400%, while the reduction in short-circuit power is less than 10%.

P_{1d} can be described as $P_{1d} = fV_{dd}^2 C_1$, where f is the operating frequency, C_1 is the total capacitance driven by Inv_1, and V_{dd} is the supply voltage. The dynamic power dissipated by a lossy transmission line equals the dynamic power dissipated by the total capacitance of the line [27]. The short-circuit power dissipated within the load gate $P_{2\mathrm{sc}}$ is directly proportional to the input signal transition time, which is the signal transition time at the far end of an interconnect line. Regardless of the load characteristics, $P_{2\mathrm{sc}}$ can be represented as

$$P_{2\mathrm{sc}} = G(V_{\mathrm{dd}}, V_t, K, C_L)\ \tau_0\ f \tag{2}$$

where τ_0 is the transition time of the input signal at the load gate, and $G(V_{\mathrm{dd}}, V_t, K, C_L)$ is a function of V_{dd}, threshold voltage V_t, transconductance K of the load gate, and capacitive load C_L. Different techniques have been developed to characterize G under different load models. The general form of (2) is valid whether the load is modeled as a capacitive load [28], a lossless transmission line [29], or a lossy transmission line [30]. G is also a function of τ_0; however, the dependence of G on τ_0 is small.

Only C_1 and τ_0 are affected by a change in the linewidth. Changing the linewidth has a significant effect on the transition time as described in Section III.

C. Transient Power Optimization Criteria

Criteria for optimizing the interconnect width to minimize the transient power dissipation is presented in this section.

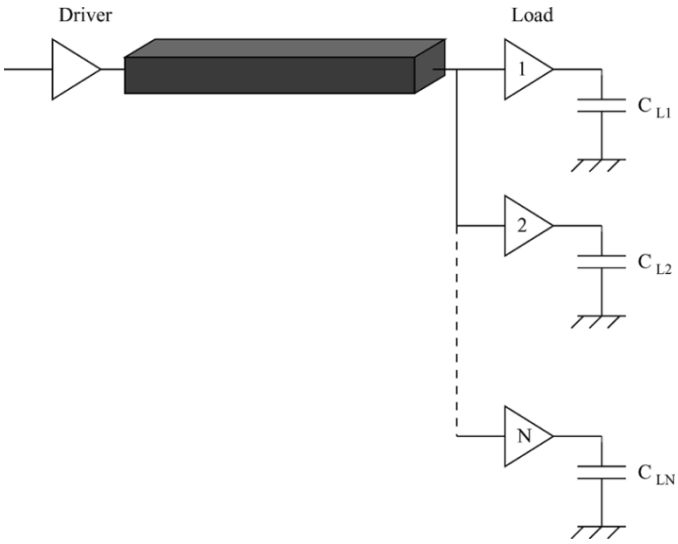

Fig. 5. Inverter driving N logic gates.

The tradeoff between the primary transient power dissipation components (short-circuit and dynamic) suggests an optimum linewidth at which the total transient power dissipation is minimum.

Previous research in wire sizing has not considered the change in short-circuit power with a change in the linewidth. The short-circuit power has not been considered as a part of the optimization process. A change in the line impedance characteristics affects the power dissipation of the circuit (specifically, the short-circuit power). Ignoring the interconnect matching characteristics between the driver and load may therefore lead to a nonoptimal solution (dissipating excessive power).

The effective output impedance of the driver also plays an important role in the matching response and total transient power dissipation. Two complementary effects occur. As the driver size increases, the transition time of the output signal decreases and, consequently, the short-circuit power dissipated by the load gate decreases. Simultaneously, the input capacitance of the driver gate increases since a larger inverter is used to drive the load, increasing the power required to charge the gate capacitance. The total transient power can be expressed in terms of two design parameters, the interconnect width and the driver size.

For an inverter driving N gates, as shown in Fig. 5, the total transient power dissipation $P_{\text{tdrive}}(W_{\text{INT}}, W_n)$ is a function of the linewidth W_{INT} and the nMOS transistor width W_n which represents the driver size (assuming a symmetric CMOS inverter as the driver)

$$P_{\text{tdrive}}(W_{\text{INT}}, W_n) = P_{1d}(W_{\text{INT}}) + N\,P_{2\text{sc}}(W_{\text{INT}}, W_n) + P_{\text{driver}}(W_n) \quad (3)$$

where $P_{\text{driver}}(W_n)$ is the dynamic power required to charge the gate capacitance of the driver

$$P_{\text{driver}}(W_n) = f\,V_{\text{dd}}^2 C_{\text{driver}} W_n \quad (4)$$

$$C_{\text{driver}} = \alpha\left(1 + \frac{\mu_n}{\mu_p}\right) L_n C_{\text{ox}} \quad (5)$$

where μ_n/μ_p is the electron to hole mobility ratio, L_n is the feature size, C_{ox} is the gate oxide capacitance per unit area, and α is a constant characterizing the effective gate capacitance during different regions of operation.

The dynamic power of the driving inverter $P_{1d}(W_{\text{INT}})$ is a function of the interconnect width

$$P_{1d}(W_{\text{INT}}) = f V_{\text{dd}}^2 C_1(W_{\text{INT}}) \quad (6)$$

where

$$C_1(W_{\text{INT}}) = N C_{2g} + C_{\text{INT}}(W_{\text{INT}}) \quad (7)$$

C_{2g} is the gate capacitance of the load inverter, and $C_{\text{INT}}(W_{\text{INT}})$ is the total interconnect capacitance which is a function of the interconnect width.

To achieve the global minimum for the transient power dissipation, the wire and driver size are simultaneously determined. Differentiating (3) with respect to W_{INT} and W_n and equating each expression to zero, two nonlinear equations in W_{INT} and W_n are obtained

$$\frac{\partial P_{\text{tdrive}}}{\partial W_{\text{INT}}} = f V_{\text{dd}}^2 \frac{\partial C_{\text{INT}}}{\partial W_{\text{INT}}} + \frac{NfG}{0.8}\left(\frac{\partial t_{10\%}}{\partial W_{\text{INT}}} - \frac{\partial t_{90\%}}{\partial W_{\text{INT}}}\right) = 0 \quad (8)$$

$$\frac{\partial P_{\text{tdrive}}}{\partial W_n} = \frac{NfG}{0.8}\left(\frac{\partial t_{10\%}}{\partial W_n} - \frac{\partial t_{90\%}}{\partial W_n}\right) + \alpha\left(1 + \frac{\mu_n}{\mu_p}\right) L_n C_{\text{ox}} = 0 \quad (9)$$

where $\partial t_{10\%}/\partial W_{\text{INT}}$, $\partial t_{90\%}/\partial W_{\text{INT}}$, $\partial t_{10\%}/\partial W_n$, and $\partial t_{90\%}/\partial W_n$ are described in the Appendix and $\partial C_{\text{INT}}/\partial W_{\text{INT}}$ is obtained from [31].

Numerical techniques are used to solve these two expressions. The two equations are solved simultaneously to determine the optimum solution. Using specific technology parameters, an analytic solution is compared to simulation results in Section V-B. In Section III, a change in the interconnect impedance characteristics, which directly affects the short-circuit power, is described.

III. Transition Time for a Signal at the Far End of an RLC Interconnect Line

From Section II-B, the short-circuit power is linearly dependent upon the input signal transition time. The effect of the wire size on the line impedance matching characteristics and the transition time is described in this section.

Wire-sizing techniques to date have not considered the line-matching characteristics as the linewidth changes. For inductive interconnect, the matching response plays an important role in the signal characteristics. It is shown in this section that, for an underdriven line, the transition time increases as the line becomes wider. An analytic solution of the signal transition time at the far end of an interconnect line is presented in Section III-A. The effect of wire sizing on the line-matching characteristics and transition time is described in Section III-B.

A. Analytic Solution for the Transition Time

An analytic solution for the signal transition time at the far end of an inductive interconnect line is presented. The signal is

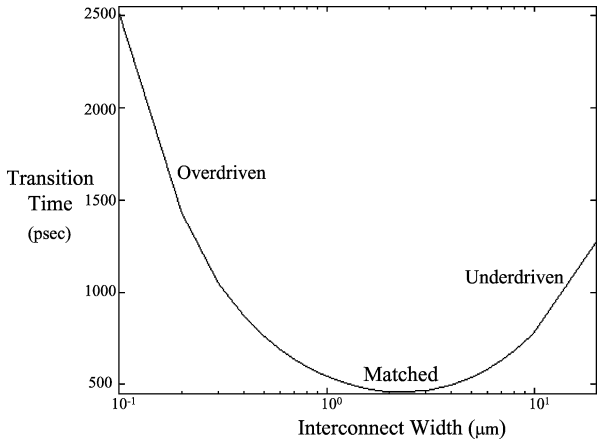

Fig. 6. Transition time as a function of interconnect width for different impedance matching conditions. Note the minimum transition time at the ideally matched condition.

assumed in this solution to behave as a ramp signal as the signal transitions from high-to-low. After the pMOS transistor of the driving inverter turns off, an expression for the signal at the far end of the line is

$$V(t) = V_c(\tau_{\rm pOFF})\, e^{-\alpha_n (t-\tau_{\rm pOFF})} \tag{10}$$

where $\tau_{\rm pOFF}$ is the time at which the pMOS transistor of the driver turns off, and α_n is a constant that depends upon R, C, L, and the transistor characteristics of the driver such as the transconductance, mobility, and threshold voltage. $V_c(\tau_{p\rm OFF})$ is the voltage across the load capacitance at $\tau_{\rm pOFF}$. A derivation of this relation is presented in the Appendix . The transition time is expressed by $\tau_0 = (t_{10\%} - t_{90\%})/0.8$, where $t_{10\%}$ and $t_{90\%}$ are the times at which the signal reaches 10% and 90% of the final value, respectively.

The transition time based on this analytic solution is shown in Fig. 6. The change in the matching condition between the driver and the load which leads to this shape is described in Section IV. As the linewidth increases, the signal transition time decreases until a minimum transition time is reached. The signal transition time increases after exceeding a certain linewidth. The transition time based on this analytic solution is compared to SPICE in Section V-A.

B. Dependence of Line Characteristics on Interconnect Width

Increasing the inductance-to-resistance ratio of the line by widening the line changes the matching characteristics. For linewidths at which the line inductance dominates the line resistance, the matching condition plays an important role in the signal characteristics. For an inductive environment, the matching condition between the driver and the load affects both the power and speed characteristics as shown in Section V.

To better understand the signal behavior in terms of the interconnect width, an equivalent circuit of an inverter driving an inductive interconnect line is shown in Fig. 7(a). The characteristic impedance of a lossy line can be described by the well known formula, $Z_{\rm lossy} = \sqrt{R + jwL/jwC}$. Different approximations have been made to estimate $Z_{\rm lossy}$ in terms of the per unit length parameters [45]–[47]. A general form of $Z_{\rm lossy}$ is $Z_0 + g\,R$ where g is a constant which depends on the line parameters. At the end of the high-to-low input transition, the nMOS transistor is off. With the input low, the inverter can be modeled as an ideal voltage source with a variable output resistance $R_{\rm tr}$ as shown in Fig. 7(b).

At small interconnect widths, the characteristic line impedance is large as compared to the equivalent output resistance of the transistor. Thus, the line is overdriven (the underdamped condition). $Z_{\rm lossy}$ decreases with increasing linewidth. The line remains underdamped until $Z_{\rm lossy}$ equals $R_{\rm tr}$. A further increase in the linewidth underdrives the line as $Z_{\rm lossy}$ becomes less than $R_{\rm tr}$ [48]. As the linewidth is increased, the line driving condition changes from overdriven to matched to underdriven.

Increasing the linewidth makes an overdriven line behave more inductively. The resistance decreases linearly with a linear increase in width while the inductance decreases sublinearly [32]. As described in [2], the line approaches a lossless condition, where the attenuation constant approaches zero at large linewidths. This effect further reduces the signal transition time. As the linewidth increases, $Z_{\rm lossy}$ decreases until the line impedance matches the driver impedance. At this width, the transition time is minimum as shown in Fig. 6. A further increase in the width underdrives the line. At these widths, the capacitance begins to dominate the line impedance. With wider lines, the line becomes highly capacitive which increases the transition time, thereby increasing the short-circuit power dissipated in the load gate. For an overdriven line, the short-circuit power dissipation changes with linewidth as shown in Fig. 3. For an underdriven line, however, an increase in the linewidth increases the short-circuit power. If the line is underdriven, the line should be as thin as possible to minimize the total transient power by decreasing both the dynamic and the short-circuit power.

A CMOS inverter driving a capacitive load of 250 fF through a 5-mm-long interconnect line is chosen to demonstrate the signal behavior. Twenty RLC distributed impedance elements are used to model the interconnect line. The input signal $V_{\rm in}$ is a ramp signal with a 100 psec transition time. The signal V_c across the load capacitance is illustrated by the waveforms depicted in Fig. 8. In Fig. 8(a), the line is thin. The line inductance does not affect the signal waveform as the resistance dominates. As the linewidth increases, overshoots and undershoots appear in the waveform. As shown in Fig. 8(b), the line inductance affects the signal characteristics and the signal transition time decreases (the overdriven condition). A further increase in the width matches the load with the driver and the overshoots disappear [see Fig. 8(c)]. The signal transition time is minimum at this condition. As the wire is widened, some steps start to appear in the waveform (the underdriven condition) and the transition time increases [see Fig. 8(d)–(f)].

IV. Signal Transition Time Characteristics

In this section, the signal characteristics at the far end of an inductive interconnect line for different line parameters are presented. The line parameters have an effect on the characteristics of the signal propagating along the line. Different

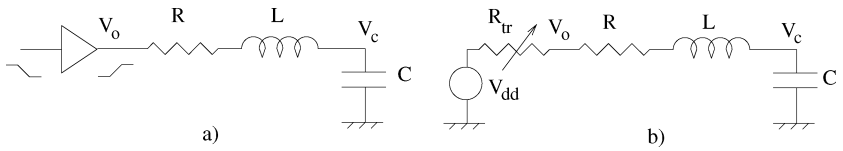

Fig. 7. An inverter driving an RLC interconnect line (a) circuit diagram and (b) equivalent circuit of inverter at the end of the high-to-low input transition.

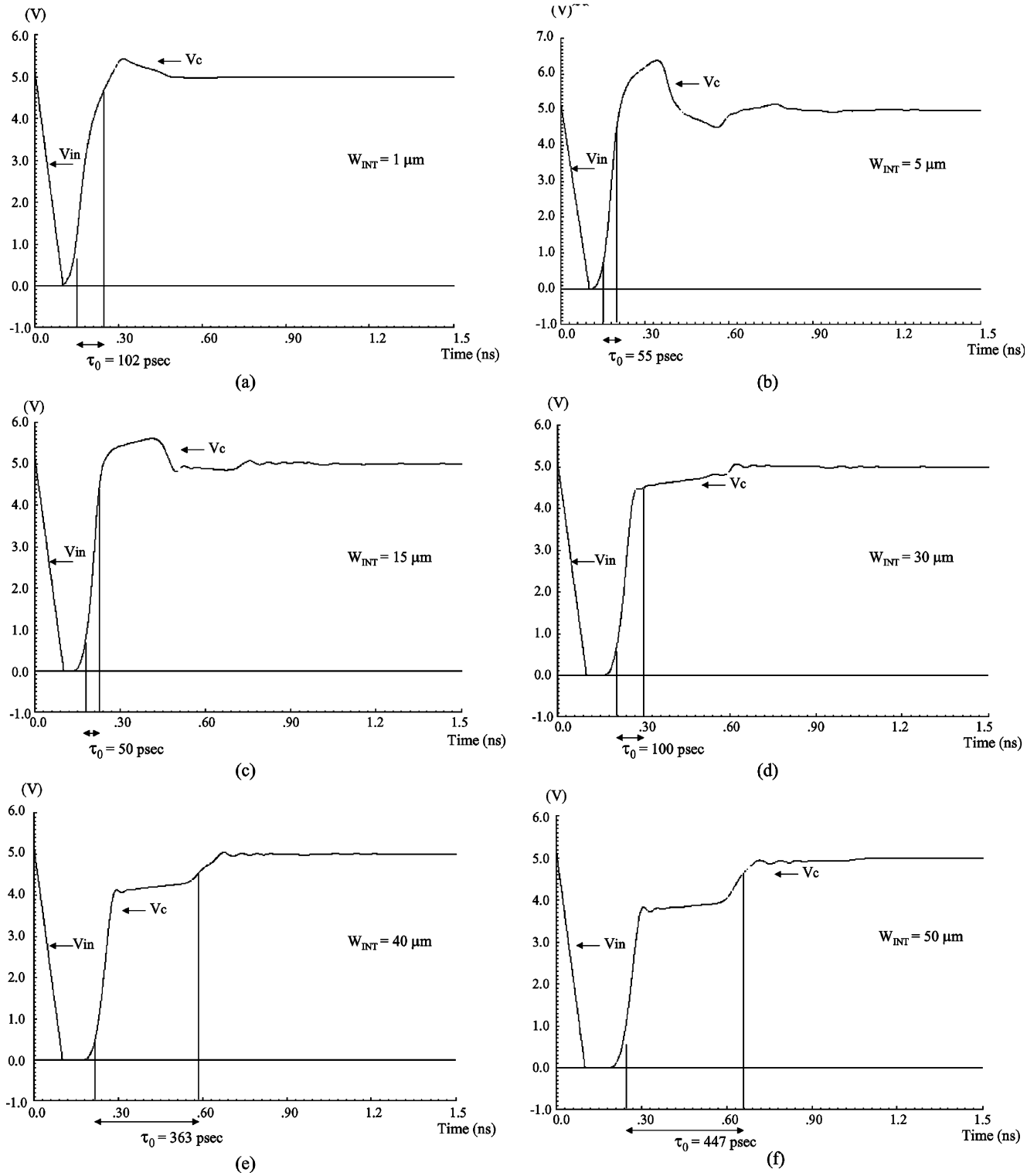

Fig. 8. Output waveform at the far end of a long interconnect line driven by an inverter with different linewidths. (a) Resistive. (b) Overdriven (inductive). (c) Matched. (d) Underdriven (inductive). (e) Underdriven. (f) Underdriven.

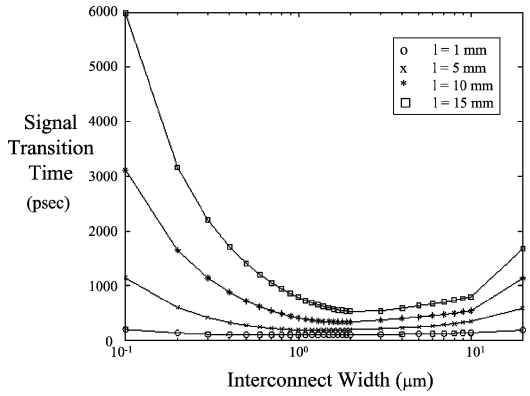

Fig. 9. Signal transition time versus interconnect width for different line lengths.

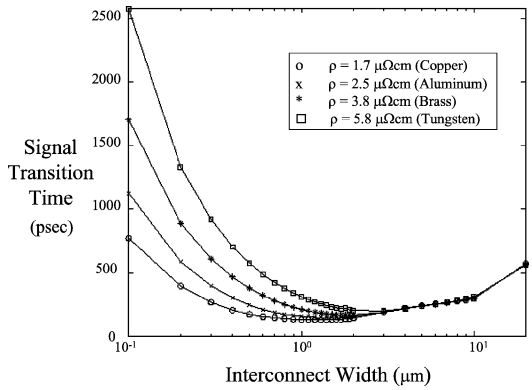

Fig. 10. Signal transition time versus interconnect width for different materials (i.e., resistivities).

interconnect lines with different line lengths and materials are discussed. The sensitivity of the signal characteristics to changes in the linewidth varies for different line lengths as described in Section IV-A. In Section IV-B, the effect of different line materials (and, therefore, resistivities) on the signal behavior is reviewed.

A. Effect of Interconnect Length

As the interconnect line becomes more inductive, the change in the line impedance characteristics becomes more significant with changing linewidth. Different interconnect line lengths are examined using Cadence SPICE. The lines are modeled by twenty distributed RLC impedance elements. The signal transition time at the far end of the line with a load capacitance of 250 fF is shown in Fig. 9. For a short line, the change in the signal transition time is less significant, as the line is not significantly inductive. As the interconnect becomes longer, increasing the inductive behavior, the signal characteristics become more sensitive to changes in the linewidth. This effect places additional emphasis on determining the optimum linewidth in longer lines that minimize the total transient power dissipation.

B. Effect of Interconnect Resistivity

Different interconnect line materials have different resistivities. An increase in the line inductance-to-resistance ratio associated with an increase in the width makes the signal characteristics more sensitive to the matching condition between the driver and the line. Simulations are used to examine different interconnect lines with different line materials.

As shown in Fig. 10, for wider lines the line resistivity has no effect on the signal characteristics. After exceeding a specific linewidth (e.g., 3 μm in the specified example), the signal transition time is the same for all line resistivities. For wide lines, the losses along the line are negligible, however, the signal transition time increases. This behavior shows that the increase in the transition time is caused by a change in the matching characteristics and is not due to signal degradation due to resistive losses. When the line inductance dominates the line resistance, the matching characteristics have a more significant effect on the signal behavior.

TABLE I
SIMULATION AND ANALYTIC TRANSITION TIMES OF A SIGNAL AT THE FAR END OF AN INDUCTIVE INTERCONNECT LINE

$W_{INT}(\mu m)$	$R_t\,(\Omega)$	L_t (nH)	C_p (fF)	τ_0		Error (%)
				Spice	Analytic	
0.1	1250	9.62	628.10	2386.25	2510.71	5.22
0.2	625.00	9.53	652.02	1349.13	1431.80	6.13
0.3	416.67	9.45	670.56	999.88	1050.92	5.11
0.4	312.50	9.37	686.80	826.25	870.73	5.38
0.5	250.00	9.30	701.72	725.00	761.57	5.04
0.6	208.33	9.24	715.80	657.50	688.53	4.72
0.7	178.57	9.18	729.27	614.00	636.50	3.66
0.8	156.25	9.12	742.30	582.44	597.86	2.65
0.9	138.89	9.07	754.98	559.66	568.38	1.56
1	125.00	9.02	767.38	543.03	545.54	0.46
1.1	113.64	8.97	779.56	531.04	528.12	-0.55
1.2	104.17	8.92	791.55	521.84	513.78	-1.54
1.3	96.15	8.88	803.37	515.50	501.13	-2.79
1.4	89.29	8.83	815.06	511.04	490.85	-3.95
1.5	83.33	8.79	826.63	508.09	482.50	-5.04
1.6	78.13	8.75	838.10	506.38	475.75	-6.05
1.7	73.53	8.72	849.47	505.63	470.36	-6.97
1.8	69.44	8.68	860.76	505.69	466.11	-7.83
1.9	65.79	8.65	871.98	506.44	462.86	-8.61
2	62.50	8.61	883.13	507.73	460.45	-9.31
3	41.67	8.32	991.97	537.98	465.83	-13.41
4	31.25	8.10	1097.83	581.59	497.43	-14.47
5	25.00	7.92	1202.00	629.75	538.98	-14.41
6	20.83	7.76	1305.00	678.75	584.86	-13.83
7	17.86	7.63	1407.40	729.79	632.80	-13.29
8	15.63	7.51	1509.10	782.50	681.79	-12.87
9	13.89	7.41	1610.00	835.13	731.34	-12.43
10	12.50	7.31	1711.30	886.04	781.18	-11.83
20	6.25	6.67	2709.85	1411.56	1273.64	-9.77
Maximum Error						14.47
Average Error						7.2

V. SIMULATION RESULTS

Some simulation results are presented in this section to verify the analytic expressions described in Section II. In Section V-A, the accuracy of the analytic solution for the signal transition time at the far end of an inductive interconnect is examined. The expression for the total transient power dissipation is evaluated in Section V-B. In Section V-C, the effects of interconnect resistivity and length on reducing power dissipation is verified.

A. Transition Time

The analytic solution presented in Section III-A is compared with SPICE in this section. A 0.24 μm CMOS inverter with $W_n = 15\,\mu$m and $W_p = 30\,\mu$m is assumed. As listed in Table I,

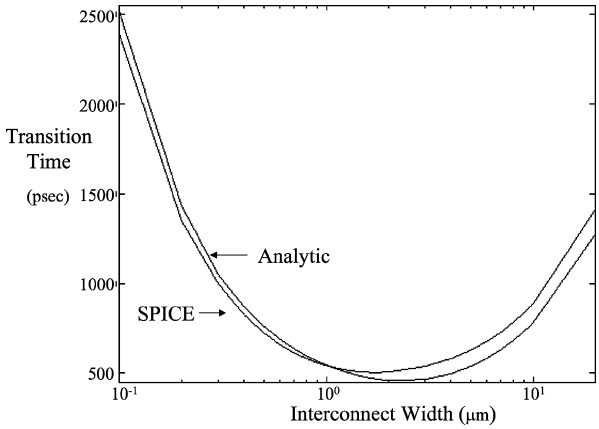

Fig. 11. Analytic solution of the transition time as compared with SPICE for different linewidths.

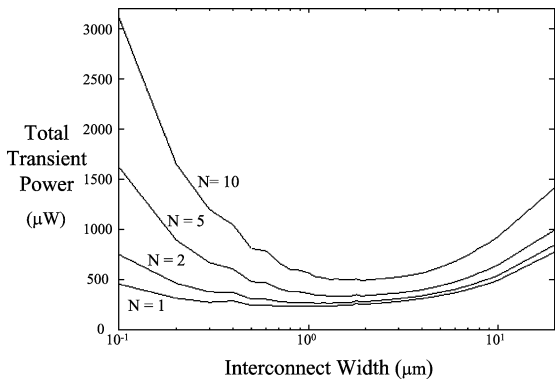

Fig. 12. Total transient power dissipation for an inverter driving N logic gates as determined by SPICE.

the transition time is determined from (10) and compared with SPICE. The linewidth is varied from 0.1 to 20 μm. The maximum error in the analytic solution as compared to SPICE is less than 15% and typically is around 7%. The transition time based on this solution is compared to SPICE in Fig. 11.

B. Minimizing the Transient Power

The transient power components can be expressed in terms of the linewidth. A criterion for determining the interconnect width that minimizes the total transient power is applied in this section to a simple example circuit and compared with SPICE.

Using closed form expressions for the line impedance parameters in terms of the linewidth, the transition time $\tau_0(W_{\rm INT}, W_n)$ as a function of W_n and $W_{\rm INT}$ is obtained. From (8) and (9), the short-circuit power of the load inverter $P_{\rm 2sc}(W_{\rm INT}, W_n)$ can be expressed in terms of the design parameters to obtain an analytic solution for the optimum width so as to minimize power.

For a specific driver size, the total simulated power dissipation for N =1, 2, 5, and 10 is shown in Fig. 12. As the number of load gates increases, the total short-circuit power dissipation over a practical range of interconnect widths increases. Determining the optimum width becomes more efficient, since the dynamic power can be traded off with the short-circuit power.

A comparison between the analytic solution and simulation is listed in Table II. The number of load gates is provided in the first column. The effect of applying the optimization criterion on the signal propagation delay is also determined. The optimum interconnect width obtained from the analytic solution and simulation is listed in the second and third columns, respectively. A numerical method is used to solve (8). The error between the analytic solution and SPICE for the target range of values is less than 6%. The optimum width for minimum power is compared with the optimum width for minimum delay. The per cent increase in signal propagation delay, when the optimum width for minimum power is used, is listed in the last column of the table. The maximum per cent increase in the propagation delay is about 21%.

TABLE II
SIMULATION AND ANALYTIC RESULTS OF THE OPTIMUM WIDTH WITH DIFFERENT LOADS

Number of Loads N	$W_{INT_{optimum}}$ (μm)		Error (%)	Increase in the delay from minimum value (%)
	Analytic	SPICE		
1	0.51	0.50	+2.0	21.0
2	0.72	0.70	+2.0	10.8
5	1.06	1.00	+6.0	5.2
10	1.34	1.30	+3.1	4.2

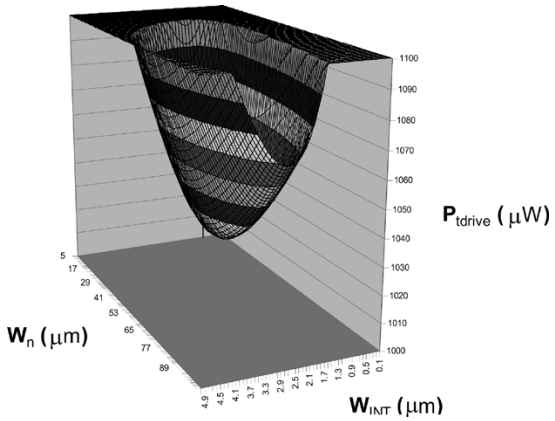

Fig. 13. Total power dissipation with different wire and driver sizes. The number of load gates N is 10. Note that the minimum power occurs at $W_n = 57$ μm and $W_{\rm INT} = 2.8$ μm.

For $N = 10$, the total transient power dissipation of a symmetric driver is shown in Fig. 13. Considering the driver size as a design variable, a different local minimum for the transient power dissipation exists for each driver size. Furthermore, for each linewidth, a minimum transient power dissipation also exists at a specific driver size. A global minimum for the transient power is obtained by simultaneously solving (8) and (9) to determine the optimum value for each design variable. For the example circuit shown in Fig. 5, the global minimum power of 942 μW is achieved at $W_{\rm INT} = 2.8$ μm and $W_n = 57$ μm. The reduction in power dissipation is 28%. Rather than minimizing the total transient power, an expression for the propagation delay [3] is used to minimize the power-delay product. The global minimum power-delay product of 91.4 μW ns is achieved at $W_{\rm INT} = 2.0$ μm and $W_n = 54$ μm.

C. Effects of Interconnect Resistivity and Length on Transient Power Dissipation

The proposed criteria for interconnect width optimization is applied to different target circuits. The total transient power dis-

TABLE III
POWER REDUCTION FOR DIFFERENT LINE PARAMETERS

Resistivity ρ $\mu\Omega\,cm$	Total Transient Power Dissipation (μW)				
	Resistive Line (l = 1 mm)				
	Optimum	Thin	Reduction	Wide	Reduction
1.7 (Copper)	583	817	28.6%	808	27.8%
2.5 (Aluminum)	606	976	37.8%	813	25.4%
	Inductive Line (l = 5 mm)				
1.7 (Copper)	1121	3563	68.5%	1931	41.9%
2.5 (Aluminum)	1236	5592	77.9%	1973	37.4%

sipation is obtained using three different interconnect widths; thin, optimum, and wide. Different case studies show the importance of the optimization process for reducing power. The optimum width is obtained for two line lengths, $l = 1$ mm (more resistive) and 5 mm (more inductive). For short (resistive) lines, the signal characteristics are not particularly sensitive to the linewidth. The optimum width, however, achieves a greater power reduction in more inductive lines.

Using the optimum width rather than the minimum width constrained by the technology, the total power dissipation is decreased by reducing the short-circuit power. As listed in Table III, the optimum width of a copper line reduces the total transient power by 68.5% for $l = 5$ mm as compared to 28.6% for $l = 1$ mm. For aluminum, a reduction of 77.9% (for $\mathrm{l} = 5$ mm) is achieved as compared to 37.8% (for $\mathrm{l} = 1$ mm). The more inductive the interconnect, the more sensitive the power dissipation is to a change in the linewidth (and the signal characteristics). Wire width optimization is, therefore, more effective for longer, more inductive lines.

A ten-times wide-line is used rather than the optimum line. The optimum width reduces the total power dissipation as compared to a wide line. A reduction occurs in both transient power components (short-circuit and dynamic). The per cent reduction in power is listed in the last column of Table III. For both line lengths, the reduction in copper interconnect is higher than the reduction in aluminum interconnect. For $l = 5$ mm, the per cent reduction in power is 27.8% for copper interconnect as compared to 25.4% for aluminum interconnect. A reduction in copper interconnect of 41.9% is obtained versus 37.4% in aluminum interconnect for $l = 1$ mm. This result is nonintuitive as the line resistance is higher for aluminum and both lines have the same capacitance and inductance. The absolute value of the power dissipation is actually higher for aluminum interconnect than for copper interconnect. The inductance-to-resistance ratio L/R of the copper interconnect is higher, increasing the importance of the optimum width for less resistive (highly inductive) lines. Alternatively, for thin lines, the line resistance has a greater effect on the signal characteristics. The reduction in power is higher for aluminum interconnect than for copper interconnect (note the reduction in Table III).

VI. CONCLUSION

It is shown in this paper that the power characteristics of inductive interconnects may greatly influence wire sizing optimization techniques. Increasing the interconnect width can decrease the total transient power since the short-circuit power becomes smaller in inductive interconnect. A tradeoff, therefore, exists between dynamic and short-circuit power in choosing the width of inductive interconnects. This tradeoff is not significant in resistive lines as the signal characteristics are less sensitive to the line dimensions. The short-circuit power of an overdriven interconnect line decreases with linewidth, while the dynamic power increases. When the line exceeds the matched condition, not only the dynamic power but also the short-circuit power increases with increasing linewidth. Interconnect optimization criteria should consider changes in the matching characteristics between the line and the driver to achieve optimum circuit performance.

The matching condition between the driver and the load has an important effect on the line impedance characteristics. If the line is overdriven, the short-circuit power decreases with increasing linewidth. When the line exceeds the matched condition, the short-circuit power increases with increasing linewidth (and signal transition time). To achieve lower transient power dissipation, the minimum linewidth should be used if the line is underdriven. For a long inductive interconnect line, an optimum interconnect width exists that minimizes the total transient power dissipation.

An analytic solution of the signal transition time at the far end of an inductive interconnect line is presented and exhibits an error of less than 15%. The solution can be used to optimize the power dissipated by high speed CMOS circuits. An analytic solution is presented for determining this optimum width. This solution has high accuracy, producing an error of less than 6%. The optimum linewidth is more effective in reducing the total transient power as the line becomes longer. With aluminum interconnect, the power is reduced by about 80% and 37% as compared to thin and wide wires, respectively. For copper interconnect, the power is reduced by 68% and 42% for the same conditions. Greater power reduction is achieved for optimally sized lines with higher resistivity interconnect as compared to minimum width lines. The optimum interconnect width depends upon both the driver size and the size of the load. With this solution, the optimum driver and wire size that dissipate the minimum transient power can be simultaneously determined.

APPENDIX
TRANSITION TIME FOR A SIGNAL AT THE FAR END OF AN INDUCTIVE INTERCONNECT

To determine an analytic solution for the signal transition time at the far end of an inductive interconnect, a lumped RLC model of the interconnect impedance is assumed. A lumped RLC model is widely used as a simple reduced order model for inductive interconnects [1], [30], [38]–[43]. The total line resistance, capacitance, and inductance are $R_t = Rl$, $C_t = Cl$, and $L_t = Ll$, respectively, where l is the line length. Adding the gate capacitance C_g to the line capacitance, the total load capacitance is $C_p = C_t + C_g$. The input ramp signal is

$$V_{\mathrm{in}}(t) = \begin{cases} \frac{t}{\tau_r} V_{\mathrm{dd}}, & \text{for } 0 \le t \le \tau_r \\ V_{\mathrm{dd}}, & \text{for } t > \tau_r \end{cases} \tag{11}$$

where τ_r is the transition time of the input signal. The line is assumed to be driven by a CMOS inverter. For the case where the transition time of the input and output signals is comparable, the operation of a CMOS inverter can be divided into four regions as listed in Table IV. Some of these regions can be of short duration or not occur, but in the general case, all of these regions

TABLE IV
DIFFERENT REGIONS OF OPERATION FOR A CMOS INVERTER WITH A RAMP INPUT SIGNAL FOR COMPARABLE INPUT AND OUTPUT SIGNAL TRANSITIONS AFTER THE INPUT SIGNAL EXCEEDS THE THRESHOLD VOLTAGE OF THE NMOS TRANSISTOR ($V_{\rm in} > V_{\rm tn}$)

Region	Condition		NMOS	PMOS
I	$V_{dd} - \lvert V_{tp}\rvert > V_{in} \geq V_{tn}$	$V_o > V_{in} + \lvert V_{tp}\rvert$	Saturation	Triode
II		$V_o > V_{in}$ - V_{tn}	Saturation	Saturation
III		$V_o \leq V_{in}$ - V_{tn}	Triode	Saturation
IV	$V_{in} \geq V_{dd} - \lvert V_{tp}\rvert$		Triode	Cut-off

may exist. When $V_{\rm in}$ transitions from low-to-high, the pMOS transistor initially operates in the triode region, then enters the saturation region. When the input signal reaches $V_{\rm dd} - |V_{tp}|$, the pMOS transistor turns off, and the charge on the capacitive load discharges through the nMOS transistor. The nMOS transistor initially operates in the saturation region, then moves into the triode region.

The pMOS and nMOS transistors can be modeled by the equivalent resistances $R_p = 1/\gamma_p$ and $R_n = 1/\gamma_n$, respectively. According to the $n_{\rm th}$-power law MOSFET model [44], γ_p is

$$\gamma_p = \alpha_p K_p(|V_{\rm gsp} - V_{tp}|)^{m_p} \tag{12}$$

where K_p and m_p control the triode region characteristics of the transistor, α_p is a constant between one and two which represents the dependence of the MOSFET equivalent resistance on the drain-to-source voltage $V_{\rm ds}$, and $V_{\rm gs}$ is the gate-to-source voltage of the transistor. p and n connote the *P*-channel and *N*-channel transistor, respectively.

In region I, after $V_{\rm in}$ exceeds the nMOS transistor threshold voltage $V_{\rm tn}$, the saturation current of the nMOS transistor is

$$I_{nI}(t) = B_n(V_{\rm in}(t) - V_{\rm tn})^{n_n}, \quad \text{for } t \geq \tau_{n\rm ON} \tag{13}$$

where B_n and n_n describe the saturation region characteristics of the nMOS transistor and $\tau_{n\rm ON}$ is given by $V_{\rm dd}(\tau_r/V_{\rm tn})$. At the output node of the driver, the KCL and KVL equations are

$$I_p + I_l = I_n \tag{14}$$

$$V_o = V_c - V_r - V_l \tag{15}$$

respectively, where V_o is the voltage at the output node and V_r, V_l, and V_c are the voltages across the resistance, inductance, and capacitance, given by (16)–(18), respectively. I_p, I_n, and I_l are the currents through the pMOS transistor, the nMOS transistor, and the load capacitor, respectively

$$V_r(t) = I_l(t)\, R_t \tag{16}$$

$$V_l(t) = L_t \frac{dI_l(t)}{dt} \tag{17}$$

$$V_c(t) = -\frac{1}{C_p}\int I_l(t). \tag{18}$$

In region I, I_p, I_l, and V_c are given by (19)–(21), respectively

$$I_{pI}(t) = \gamma_p(V_{\rm dd} - V_o), \tag{19}$$

$$I_{lI}(t) = A + B\,t + D_1\, e^{-\alpha_{p1}\,t} + D_2\, e^{-\alpha_{p2}\,t} \tag{20}$$

$$V_{cI}(t) = V_{\rm dd} - \frac{1}{C_p}\left[A\,t + B\,\frac{t^2}{2} + D_1\,(1 - e^{-\alpha_{p1}\,t}) + D_2\,(1 - e^{-\alpha_{p2}\,t})\right] \tag{21}$$

where A, B, D, E, α_{p1}, and α_{p2} are constants given by

$$A = -(D_1 + D_2),\ B = q\,C_p\,L_t$$

$$D_1 = q\,e^{\beta\alpha_{p1}}\,\frac{1}{\alpha_{p1}^2(\alpha_{p2} - \alpha_{p1})}$$

$$D_2 = q\,e^{\beta\alpha_{p2}}\,\frac{1}{\alpha_{p2}^2(\alpha_{p1} - \alpha_{p2})}$$

$$\alpha_{p1} = \frac{\frac{1+R_t\gamma_p}{L_t\gamma_p} + \sqrt{\left(\frac{1+R_t\gamma_p}{L_t\gamma_p}\right)^2 - \frac{4}{L_tC_p}}}{2}$$

$$\alpha_{p2} = \frac{\frac{1+R_t\gamma_p}{L_t\gamma_p} - \sqrt{\left(\frac{1+R_t\gamma_p}{L_t\gamma_p}\right)^2 - \frac{4}{L_tC_p}}}{2}$$

$\beta = \tau_r\, V_{\rm tn}/V_{\rm dd}$, and $q = (n_n)!(V_{\rm dd}/\tau_r)^{n_n}$.

Region II starts when $V_o(t)$ reaches $V_{\rm in} + |V_{\rm tp}|$. In this region, the pMOS transistor is saturated. The output voltage in this region can be determined using a Newton-Raphson iteration. $V_c(\tau_{\rm psat})$ is determined by (21), where $\tau_{\rm psat}$ is the initial time of this region. Since both transistors have the same drain voltage, the second region of operation in which both transistors are saturated is quite short, permitting the change in V_c during this region to be neglected.

During region III, the nMOS transistor operates in the triode region, and the pMOS transistor is saturated. Expressions for $I_l(t)$ and $V_c(t)$ are similarly obtained as in region I, and are given by (22) and (23), respectively

$$I_{\rm lIII}(t) = A_1 + B_1\,t + E_1\,e^{-\alpha_{n1}t} + E_2 e^{-\alpha_{n2}t} \tag{22}$$

$$V_{\rm cIII}(t) = V_c(\tau_{\rm psat}) - \frac{1}{C_p}\int_{\tau_{\rm psat}}^{t} I_{\rm lIII}(t)\,dt \tag{23}$$

where A_1, B_1, E_1, and E_2 are constants given by

$$A_1 = I_{\rm lIII}(\tau_{\rm psat}) - (B_1\tau_{\rm psat} + E_1 e^{-\alpha_{n1}\tau_{\rm psat}} + E_2 e^{-\alpha_{n2}\tau_{\rm psat}})$$

$$B_1 = -2\,C_p\,\frac{b}{\gamma_n},$$

$$E_1 = \frac{\alpha_{n1}^2\gamma_n V_{\rm oIII}(\tau_{\rm psat}) - 2b - a^2b\alpha_{n1}^2 - 2ab\alpha_{n1}}{\alpha_{n1}^2(\alpha_{n2} - \alpha_{n1})\gamma_n L_t}$$

$$E_2 = \frac{\alpha_{n2}^2\gamma_n V_{\rm oIII}(\tau_{\rm psat}) - 2b - a^2b\alpha_{n2}^2 - 2ab\alpha_{n2}}{\alpha_{n2}^2(\alpha_{n1} - \alpha_{n2})\gamma_n L_t}$$

$$\alpha_{n1} = \frac{\frac{1+R_t\gamma_n}{L_t\gamma_n} + \sqrt{\left(\frac{1+R_t\gamma_n}{L_t\gamma_n}\right)^2 - \frac{4}{L_tC_p}}}{2}$$

$$\alpha_{n2} = \frac{\frac{1+R_t\gamma_n}{L_t\gamma_n} - \sqrt{\left(\frac{1+R_t\gamma_n}{L_t\gamma_n}\right)^2 - \frac{4}{L_tC_p}}}{2}$$

$$b = B_p\left(\frac{V_{\rm dd}}{\tau_r}\right)^{n_p}$$

$$a = \frac{(V_{\rm dd} - V_{tp})\tau_r}{V_{\rm dd}}$$

$$\gamma_n = \alpha_n K_n(V_{gsn} - V_{tn})^{m_n}.$$

K_n and m_n control the triode region characteristics of the nMOS transistor, B_p and n_p are parameters that determine the

characteristics of the saturation region of a pMOS transistor, and α_n is similar to α_p for an nMOS transistor.

Once $V_{\rm in}$ reaches $V_{\rm dd} - |V_{tp}|$, the pMOS transistor turns off, initiating region IV. The time at which this region begins is $\tau_{\rm pOFF} = (V_{\rm dd} - |V_{tp}|)\tau_r / V_{\rm dd}$, where $V_o(\tau_{\rm pOFF})$ is obtained from (15). After the pMOS transistor turns off, the pMOS transistor continues to operate in the triode region. An expression for $V_c(t)$ in this region is

$$V_{\rm cIV}(t) = V_c(\tau_{\rm pOFF}) e^{-\alpha_{n2}(t-\tau_{\rm pOFF})}. \tag{24}$$

The transition time is expressed by $\tau_0 = (t_{10\%} - t_{90\%})/0.8$, where $t_{10\%}$ and $t_{90\%}$ are the times at which the signal reaches 10% and 90% of the final value, respectively.

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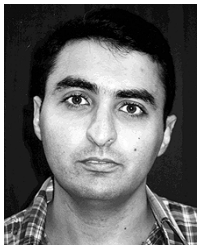

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