Impedance Characteristics of Power Distribution Grids in Nanoscale Integrated Circuits

Andrey V. Mezhiba and Eby G. Friedman, *Fellow, IEEE*

***Abstract*—The essential design characteristic of nanoscale integrated circuits is increased interconnect complexity. Conductors at different levels of the interconnect hierarchy have highly different physical and, consequently, electrical characteristics. These interconnect lines also exhibit inductive behavior due to enhanced switching speed of nanoscale devices, making interconnect design and analysis difficult. The design of robust and area efficient power distribution networks for high-speed integrated circuits has therefore become a challenging task. The impedance characteristics of multilayer power distribution grids and the relevant design implications are the subject of this paper. The power distribution network spans many layers of interconnect with disparate electrical properties. Unlike single-layer grids, the electrical characteristics of multilayer grids vary significantly with frequency. As the frequency increases, a large share of the current flow is transfered from the low-resistance upper layers to the low-inductance lower layers. The inductance of a multilayer grid therefore decreases with frequency, while the resistance increases with frequency. The lower layers of multilayer power grids provide a low-inductance current path, significantly reducing the grid impedance at high frequencies. Multilayer power distribution grids extend to the lower interconnect layers, exhibiting superior high-frequency impedance characteristics as compared to power distribution grids built exclusively within the upper, low-resistance metal layers. A significant share of metal resources to distribute the global power should therefore be allocated to the lower metal layers. An analytic model is also presented to determine the impedance characteristics of a multilayer grid from the inductive and resistive properties of the comprising individual grid layers.**

***Index Terms*—Inductance, power distribution networks.**

I. Introduction

THE FEATURE size of integrated circuits has aggressively been reduced in the pursuit of improved speed, power, and cost characteristics. Semiconductor technologies with feature sizes of several tens of nanometers are currently in development. Future nanometer scale circuits will contain more than a billion transistors and operate at clock speeds well over 10 GHz [1]. Distributing robust and reliable power and ground levels in such a high-speed, high-complexity environment, is a challenging task [2].

The challenge of designing the power distribution networks stems from two trends. The requirements placed on the on-chip power distribution networks will become more stringent in the nanoscale regime. The power supply current per circuit area and the slew rate of the current transients will increase significantly in the nanometer technology nodes. The high currents cause large ohmic IR voltage drops and the fast current transients cause large inductive $L(di/dt)$ voltage drops (ΔI noise) in power distribution networks. Furthermore, the aggressive application of low-power design techniques to limit the power consumption of high-complexity integrated circuits will aggravate the power distribution constraints. Clock and power gating significantly increase cycle-to-cycle variations in the power current, exacerbating the ΔI noise. Power supply levels are reduced, decreasing noise margins. To maintain the local supply voltage within specified design margins, the effective impedance of the power distribution networks (as seen from the power terminals of the circuit elements) should be decreased with each technology generation.

Another facet is the interconnect complexity of nanoscale circuits. The number of on-chip metal levels will be increased to satisfy the greater connectivity requirements of billion transistor circuits. High-performance circuits employ flip-chip packaging with dense I/O area arrays, effectively extending the on-chip interconnect stack with several metal layers in the package. With switching times of active nanoscale devices below a picosecond, the frequency spectrum of the power current transients drawn by the on-chip circuits will extend beyond 100 GHz. On-chip interconnect lines will exhibit profound inductive behavior at these frequencies, further exacerbating the complexity of the design task. Analysis of inductive interconnect is difficult due to the increased range of interconnect coupling. The inductive voltage drop across the on-chip power and ground lines will therefore become significant.

Decoupling capacitors are an effective technique to reduce impedance of power distribution networks operating at high frequencies. The efficacy of decoupling capacitors depends on the impedance of the conductors connecting the capacitors to the power load and the power source. Optimal allocation of on-chip decoupling capacitance depends on the impedance characteristics of the interconnect. Robust and area efficient design of multilayer power distribution grids therefore require a thorough understanding of the impedance properties of the power distributing interconnect structures.

Power distribution networks in high-performance digital ICs are commonly structured as a multilayer grid, as shown in Fig. 1.

Manuscript received December 12, 2002; revised November 14, 2003. This research was supported in part by the Semiconductor Research Corporation under Contract 2003-TJ-1068, the Defense Advanced Research Projects Agency/ITO under AFRL Contract F29601-00-K-0182, the National Science Foundation under Contract CCR-0304574, the Fulbright Program under Grant 87481764, grants from the New York State Office of Science, Technology and Academic Research to the Center for Advanced Technology—Electronic Imaging Systems and to the Microelectronics Design Center, and by grants from Xerox Corporation, IBM Corporation, Intel Corporation, Lucent Technologies Corporation, and Eastman Kodak Company.

The authors are with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY 14627 USA (e-mail: mav@ece.rochester.edu; friedman@ece.rochester.edu).

Digital Object Identifier 10.1109/TVLSI.2004.836304

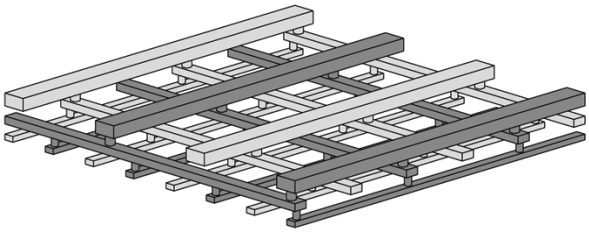

Fig. 1. Multilayer power distribution grid. The ground lines are light grey; the power lines are dark grey.

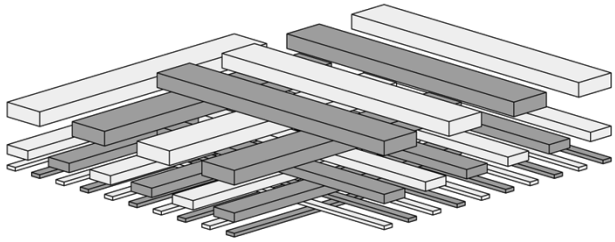

Fig. 2. Multilayer grid consists of two stacks of layers. The lines in each stack are parallel to each other. The layers in one stack determine the resistive and inductive characteristics of the multilayer grid in the direction of the lines in that stack, while the layers in the other stack determine the impedance characteristics in the orthogonal direction.

The impedance characteristics of these multilayer grids are the subject of this paper.

The paper is organized as follows. Existing work on the electrical properties of power distribution grids is reviewed in Section II. The electrical properties of multilayer power distribution grids are discussed in Section III. A case study of a two-layer power grid is presented in Section IV. The design implications of the impedance properties of multilayer grids are discussed in Section V. The conclusions are summarized in Section VI.

II. Background

On-chip power distribution grids have traditionally been considered as resistive networks [3]. The inductance of the on-chip power distribution networks has been neglected because the network inductance has been dominated by the parasitic inductance of the package pins, traces, and bond wires. This situation has changed due to the higher switching speeds of integrated circuits [4], [5] and the lower inductance of advanced flip-chip packaging. Priore noted in [6] that replacing wide power and ground lines with narrower interdigitated power and ground lines reduces the self inductance of the supply network. He also suggested an approximate expression for the time constant of the response of a power supply network to a step input signal. Zheng and Tenhunen [7] proposed replacing the wide power and ground lines with an array of interdigitated narrow power and ground lines, decreasing the characteristic impedance of the power grid.

The inductive properties of single-layer power grids have been described by the authors in [8] and [9]. In grid layers with alternating power and ground lines, long distance inductive coupling is greatly diminished due to cancellation, turning inductive coupling into, effectively, a local phenomenon. The grid inductance, therefore, behaves similarly to the grid resistance: increases linearly with grid length and decreases inversely linearly with grid width (i.e., the number of lines in the grid). The electrical properties of power distribution grids can therefore be conveniently expressed by a dimension-independent sheet resistance $R_{\square}$ and sheet inductance $L_{\square}$ [9], [10]. The inductance of the power grid layers can therefore be efficiently estimated using simple models comprised of a few interconnect lines.

Area–inductance–resistance tradeoffs in single-layer power distribution grids have also been investigated [9], [10]. The sheet inductance of power distribution grids is shown to increase linearly with line width under two different tradeoff scenarios. Under the constraint of constant grid area, a tradeoff exists between the grid inductance and resistance. Under the constraint of a constant grid resistance, the grid inductance can be traded off against grid area.

The variation of inductance with frequency in single layer power grids has been characterized [11], [12]. This variation is relatively moderate, typically less than 10% of the low-frequency inductance. An exception from this behavior are power grids with closely spaced power and ground lines where the inductance variation with frequency is greater due to significant proximity effects.

Power distribution grids in modern integrated circuits typically consist of many grid layers, spanning an entire stack of interconnect layers. The objective of the present investigation is to characterize the electrical properties of these multilayer grids, advancing the existing work beyond individual grid layers. Preliminary results of this work have been published in [13].

III. Electrical Properties of Multilayer Grids

A circuit model of multilayer power distribution grids is developed in this section. The impedance characteristics of multilayer grids are determined based on this model. The impedance characteristics of individual layers of multilayer power distribution grids are discussed in Section III-A. The variation with frequency of the impedance characteristics of several grid layers forming a multilayer grid is analyzed in Section III-B.

A. Impedance Characteristics of Individual Grid Layers

The power and ground lines within each layer of a multilayer power distribution grids are orthogonal to the lines in the adjacent layers. Orthogonal lines have zero mutual partial inductance as there is no magnetic linkage [14]. Orthogonal grid layers can therefore be evaluated independently. A multilayer grid can be considered to consist of two stacks of layers, with all of the lines in each stack parallel to each other, as shown in Fig. 2. Grid lines in one stack are orthogonal to the lines in the other stack. Grid layers in each stack only affect the grid inductance in the direction of the lines in the stack. This behavior is analogous to the properties of the grid resistance. The problem of characterizing a multilayer grid is thereby reduced to determining the impedance characteristics of a stack of several individual grid layers with lines in the same direction.

The power and ground lines in power distribution grids are connected to the lines in the adjacent layers through vias. The vias (or clusters of vias) are distributed along a power line at a pitch equal to the power line pitch in the adjacent layer. The line

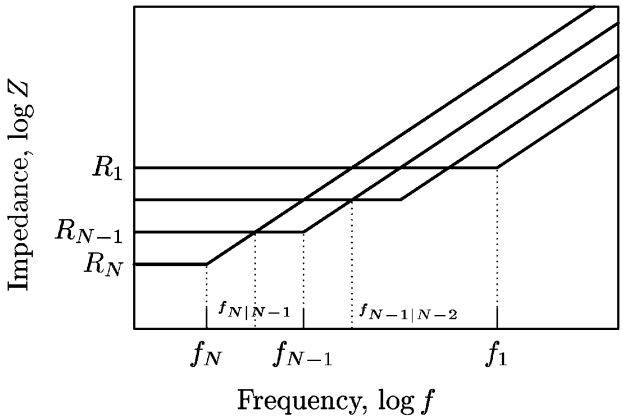

Fig. 3. Impedance of the individual grid layers comprising a multilayer grid.

pitch is much larger than the via length. The inductance and resistance of the two close parallel power lines in different metal layers are, therefore, much larger than the resistance and inductance of the connecting vias. The effect of vias on the resistance and inductance of a power grid is therefore negligible. This property is a direct consequence of the characteristic that the distance of the lateral current distribution in power grids (hundreds or thousands of micrometers) is much larger than the distance of the vertical current distribution (several micrometers). The power current is distributed among the metal layers over a distance comparable to a line pitch. The power and ground lines are effectively connected in parallel.

Each layer of a typical multilayer power distribution grid has significantly different electrical properties. Lines in the upper layers tend to be thick and wide, forming a low-resistance global-power distribution grid. Lines in the lower layers tend to be thinner, narrower, and have a smaller pitch. The lower the metal layer, the smaller the metal thickness, width, and pitch. The upper grid layers therefore have a relatively high inductance and low resistance, whereas the lower layers have a relatively low inductance and high resistance [10]. The lower the layer, the higher the resistance and the lower the inductance. In those circuits employing flip-chip packaging with a high-density area array of I/O contacts, the interconnect layers in the package are tightly coupled to the on-chip interconnect, effectively extending the on-chip interconnect hierarchy. The difference in the electrical properties across the interconnect hierarchy is particularly significant in nanoscale circuits. While the cross sectional dimensions of local on-chip lines are measured in tens of nanometers, the dimensions of package lines are of the order of tens of micrometers. The three orders of magnitude difference in dimensions translates to six orders of magnitude difference in resistance (proportional to the cross sectional area of the grid lines) and to three orders of magnitude difference in inductance (proportional to the grid line density).

The variation with frequency of the impedance of each layer in a grid stack comprised of N grid layers is schematically shown in Fig. 3. The layers are numbered from 1 (the lowest layer) to N (the uppermost layer). The grid layer resistance decreases with layer number $R_1 > R_2 > \cdots > R_N$, and the inductance increases with layer number $L_1 < L_2 < \cdots < L_N$. At low frequencies, the uppermost layer has the lowest impedance as the layer with the lowest resistance. This layer, however, has

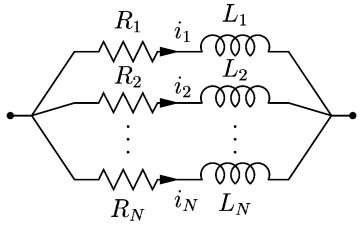

Fig. 4. Equivalent circuit of a stack of N grid layers.

the highest inductance and, consequently, the lowest transition frequency $f_N = (1/2\pi)(R_N)/(L_N)$, as compared to the other layers (see Fig. 3). The transition frequency is the frequency at which the impedance of the grid layer changes in character from resistive to inductive. At this frequency, the inductive impedance of a grid layer is equal to the resistive impedance (neglecting skin and proximity effects), i.e., $R_N = 2\pi f_N L_N$. The grid impedance increases linearly with frequency above f_N. The lowest grid layer has the highest resistance and the lowest inductance; therefore, this layer has the highest transition frequency f_1. As the inductance of the upper layers is higher than the lower layers, the impedance of an upper layer exceeds the impedance of any lower layer above a certain frequency. For example, the impedance of the uppermost layer $R_N + \omega L_N \approx \omega L_N$ equals the magnitude of the next layer impedance $R_{N-1} + \omega L_{N-1} \approx R_{N-1}$ and exceeds the impedance of the second layer above frequency $f_{N|N-1} = (1/2\pi)(R_{N-1})/(L_N)$, as shown in Fig. 3. Similarly, the impedance of layer k exceeds the impedance of a lower layer $l, k > l$, at $f_{k|l} = (1/2\pi)(R_l)/(L_k)$.

B. Impedance Characteristics of Multilayer Grids

An entire stack of grid layers cannot be accurately described by a single RL circuit due to the aforementioned differences among the electrical properties of the individual grid layers. A stack of multiple grid layers can, however, be modeled by several parallel RL branches, each branch characterizing the electrical properties of one of the comprising grid layers, as shown in Fig. 4.

Due to the difference in the electrical properties of the individual layers, the magnitude of the current in each grid layer varies significantly with frequency. At low frequencies, the low resistance uppermost layer is the path of lowest impedance, as shown in Fig. 3. The uppermost layer has the greatest effect on the low frequency resistance and inductance of the grid stack, as the largest share of the overall current flows through this layer. As the frequency increases to $f_{N|N-1} = (1/2\pi)(R_{N-1})/(L_N)$ and higher, the impedance of the uppermost layer ωL_N exceeds the impedance of the second uppermost layer R_{N-1}, as shown in Fig. 3. The second uppermost layer, therefore, carries the largest share of the overall current and most affects the inductance and resistance within this frequency range. As the frequency exceeds $f_{N-1|N-2} = (1/2\pi)(R_{N-2})/(L_{N-1})$, the next layer in the stack becomes the path of least impedance and so on. The process continues until at very high frequencies the lowest layer carries most of the overall current.

As the frequencies increase, the majority of the overall current is progressively transferred from the layers of low

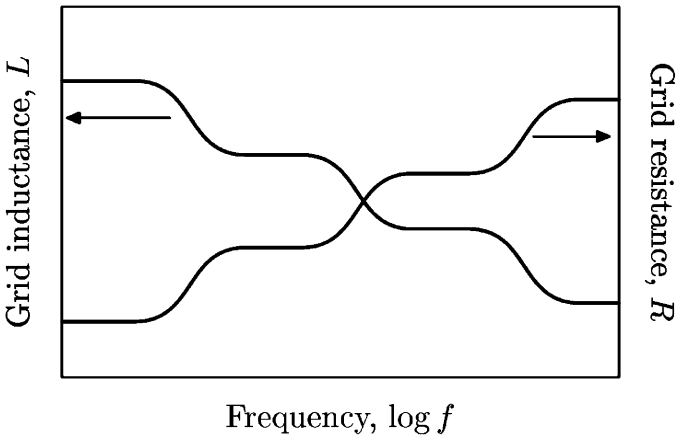

Fig. 5. Variation of the grid inductance and resistance of a multilayer stack with frequency. As the signal frequency increases, the current flow shifts to the high resistance, low inductance layers, decreasing the inductance and increasing the resistance of the grid.

resistance and high inductance to the layers of high resistance and low inductance. The overall grid inductance, therefore, decreases with frequency and the overall grid resistance increases with frequency. A qualitative plot of the variation of the grid inductance and resistance with frequency is shown in Fig. 5. At low frequency, all of the layers exhibit a purely resistive behavior and the current is partitioned among the layers according to the resistance of each layer. The share i_k of the overall current flowing through layer k is

$$i_k = \frac{I_k}{\sum_{n=1}^{N} I_n} = \frac{\prod_{n\neq k} R_n}{\sum_{m=1}^{N} \prod_{n\neq m} R_n}. \tag{1}$$

Note that $i_1 < i_2 < \cdots < i_N$ as $R_1 > R_2 > \cdots > R_N$. The resistance of a multilayer grid R_0^{LF} at low frequency is, therefore, determined by the parallel connection of all of the individual layer resistances

$$R_0^{\mathrm{LF}} = R_1 \| R_2 \| \ldots \| R_N = \frac{\prod_{n=1}^{N} R_n}{\sum_{m=1}^{N} \prod_{n\neq m} R_n}. \tag{2}$$

The low-frequency inductance of a multilayer grid L_0^{LF} is, however

$$L_0^{\mathrm{LF}} = L_1 i_1^2 + L_2 i_2^2 + \cdots + L_N i_N^2 \approx L_N \tag{3}$$

due to $L_N > L_k$ and $i_N > i_k$ for any $k \neq N$.

At very high frequencies, the resistance and inductance exchange roles. All of the grid layers exhibit a purely inductive behavior and the current is partitioned among the layers according to the inductance of each layer. The share of the overall current flowing through layer k is

$$i_k = \frac{I_k}{\sum_{n=1}^{N} I_n} = \frac{\prod_{n\neq k} L_n}{\sum_{m=1}^{N} \prod_{n\neq m} L_n}. \tag{4}$$

The relation among the currents of each layer is reversed as compared to the low frequency case: $i_1 > i_2 > \cdots > i_N$. The inductance of a multilayer grid at high frequency L_0^{HF} is

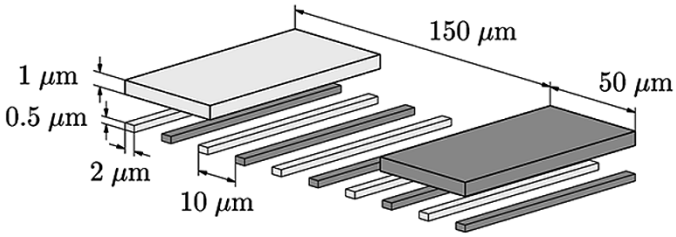

Fig. 6. General view of a two layer grid. The ground lines are white colored, the power lines are grey colored.

determined by the parallel connection of the individual layer inductances

$$L_0^{\mathrm{HF}} = L_1 \| L_2 \| \ldots \| L_N = \frac{\prod_{n=1}^{N} L_n}{\sum_{m=1}^{N} \prod_{n\neq m} L_n}. \tag{5}$$

The high-frequency resistance of a multilayer grid R_0^{HF} is

$$R_0^{\mathrm{HF}} = R_1 i_1^2 + R_2 i_2^2 + \cdots + R_N i_N^2 \approx R_1 \tag{6}$$

due to $R_1 > R_k$ and $i_1 > i_k$ for any $k \neq 1$.

The grid resistance and inductance vary with frequency between these limiting low- and high-frequency cases. If the difference in the electrical properties of the layers is sufficiently high, the variation of the grid inductance and resistance with frequency has a staircase-like shape, as shown in Fig. 5. As the frequency increases, the grid layers consecutively serve as the primary current path, dominating the overall grid impedance within a specific frequency range.

IV. Case Study of a Two-Layer Grid

The electrical properties of a two layer grid are evaluated in this section to quantitatively illustrate the concepts described in Section III. The grid parameters are described in Fig. 6.

The analysis approach used to determine the electrical characteristics of a grid structure is described in Section IV-A. Magnetic coupling between grid layers is discussed in Section IV-B. The inductive characteristics of a two-layer grid are discussed in Section IV-C. The resistive characteristics of a two layer grid are discussed in Section IV-C. The impedance characteristics of a two-layer grid are summarized in Section IV-E.

A. Simulation Setup

The inductance extraction program FastHenry [15] is used to explore the inductive properties of grid structures. FastHenry efficiently calculates the frequency dependent impedance $R(\omega) + j\omega L(\omega)$ of complex three-dimensional interconnect structures under a quasi-magnetostatic approximation. In the analysis, the lines are split into multiple filaments to account for skin and proximity effects, as discussed in Section II. A conductivity of $58\ \mathrm{S}/\mu\mathrm{m} \simeq (1.72\mu\Omega \cdot \mathrm{cm})^{-1}$ is used in the analysis where an advanced process with copper interconnect is assumed [1].

When determining the loop inductance, all of the ground lines at one end of the grid are short circuited to form a ground terminal, and all of the power lines at the same end of the grid are short circuited to form a power terminal. All of the lines at the other end of the grid are short circuited to complete the current loop. This configuration assumes that the power current loop is

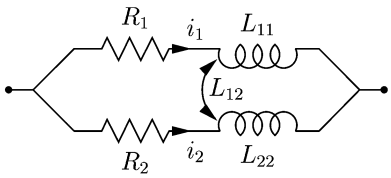

Fig. 7. Equivalent circuit diagram of a two-layer grid.

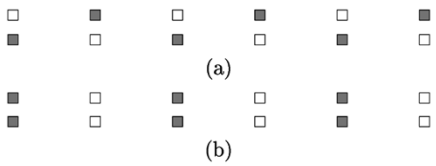

Fig. 8. Alignment of two layers with the same line pitch in a two-layer grid resulting in the minimum and maximum grid inductance. The ground lines are white colored; the power lines are grey colored. (a) The configuration with the minimum grid inductance: ground lines of one layer are aligned with the power lines of the other layer. (b) The configuration with the maximum grid inductance: the ground lines of both layers are aligned with each other.

completed on-chip. This assumption is valid for high-frequency signals that are effectively terminated through the on-chip decoupling capacitance, which acts as a low-impedance termination as compared to the inductive off-chip leads of the package. If the current loop is completed on-chip, the current in the power lines and the current in the ground lines always flow in opposite directions.

B. Inductive Coupling Between Grid Layers

An equivalent circuit diagram of a two layer power distribution grid is shown in Fig. 7. The partial mutual inductance between the lines in the two grid layers is significant as compared to the partial self inductance of the lines. Therefore, the two grid layers are, in general, magnetically coupled, as indicated in Fig. 7. It can be shown, however, that for practical geometries, magnetic coupling is significant only in interdigitated grids under specific conditions.

The specific conditions are that the line pitch in both layers is the same and the separation between the two layers is smaller than the line pitch. The two layers with the same line pitch are spatially correlated, i.e., the relative position of the lines in the two layers is repeated throughout the structure. The net inductance of such grids depends upon the mutual alignment of the two grid layers. For example, consider a two-layer grid with each layer consisting of interdigitated power and ground lines with a 1 μm $\times$ 1 μm cross section on an 8-μm pitch, as in the cross section shown in Fig. 8. The separation between the layers is 4 μm. The variation of the sheet inductance of this two-layer grid structure as a function of the physical offset between the two layers is shown in Fig. 9.

At 1 GHz, each of the layers has a loop inductance of 16.5 pH/□. The inductance of two identical parallel coupled inductors is

$$L_{1\|2} = \frac{L_{11}L_{22} - L_{12}^2}{L_{11} + L_{22} - 2L_{12}} = \frac{L_{11} + L_{12}}{2}. \qquad (7)$$

In the case of zero coupling between the two grid layers, the net inductance of the two-layer grid is approximately $16.5\,\mathrm{pH}/2 = 8.25\ \mathrm{pH}/\square$ since the two grids are in parallel. If the ground lines in the top layer are placed immediately over the power lines of the bottom layer, as shown in Fig. 8(a), a close return path for the power lines is provided as compared to the neighboring ground lines of the bottom layer. The magnetic coupling between the two grid layers is negative in this case, resulting in a net inductance of 6.5 pH/□ for the two-layer grid (which is lower than the uncoupled case of 8.25 pH/□) in agreement with (7). A two layer interdigitated grid effectively becomes a paired grid, as shown in Fig. 8(a). (Rather than equidistant line spacing, in paired grids the lines are placed in close power-ground line pairs [8].) If, alternatively, the ground lines of the top layer are aligned with the ground lines of the bottom layer, as shown in Fig. 8(b), the magnetic coupling between the two layers is positive and the net inductance of the two-layer grid is 9.9 pH/□, higher than the uncoupled case, also in agreement with (7). As the offset between the grid layers changes between these two limits, the total inductance varies from a minimum of 6.5 pH/□ to a maximum of 9.9 pH/□, passing a point where the effective coupling between the two layers is zero and the total inductance is 8.25 pH/□. The inductance at a 100-GHz signal frequency closely tracks this behavior at low frequencies.

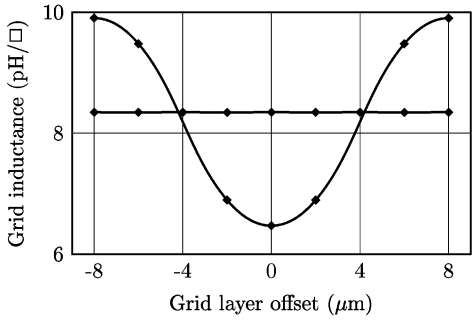

Fig. 9. Inductance of a two-layer grid versus the physical offset between the two layers. The inductance of the grid with matched line pitch of the layers (black line) depends on the layer offset. (The low-inductance alignment shown in Fig. 8(a) is chosen as the zero offset.)

If the layer separation is greater than the line pitch in either of the two layers, the net coupling from the lines in one layer to the lines in the other layer is insignificant. Coupling to the power lines is nearly cancelled by the coupling to the ground lines, carrying the current in the opposite direction. This coupling cancellation is analogous to the cancellation of the long distance coupling within the same grid layer [8]. This cancellation also explains why two grid layers are effectively uncoupled if one of the layers is a paired grid. The power to ground line separation in a paired grid is smaller than the separation between two metallization layers with the same grid line direction.

It is possible to demonstrate that in the case where the line pitch is not matched, as shown in Fig. 10, the layer coupling is effectively cancelled, and the grid inductance is independent of the layer alignment, as shown in Fig. 9. Metallization layers in integrated circuits typically are of different thickness, line width, and line spacing. Therefore, unless intentionally designed otherwise, different grid layers typically have a different line pitch and can be considered uncoupled, as has been implicitly assumed in Section III.

Fig. 10. Cross section of a two-layer grid with the line pitch of the upper layer a fractional multiple $(5/4$ in the case shown) of the line pitch in the bottom layer. Both effects illustrated in Fig. 8 occur at different locations (circled). The ground lines are white colored, the power lines are grey colored.

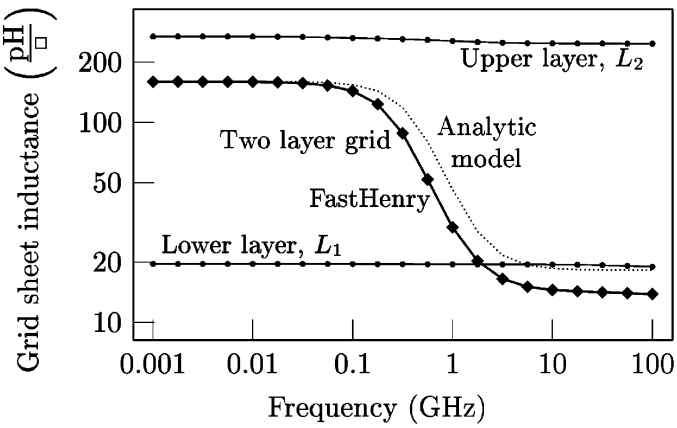

Fig. 11. Inductance of a two-layer grid versus signal frequency. Both FastHenry data (solid line) and the analytic model data (dotted line) are shown. The individual inductance of the two comprising grid layers is shown for comparison (FastHenry data).

C. Inductive Characteristics of a Two-Layer Grid

The variation of the sheet inductance with signal frequency in the two-layer grid is shown in Fig. 11. Note that the inductance of the individual grid layers, also shown in Fig. 11, is virtually constant with frequency [8], [11]. The sheet inductance of the upper layer L_2 is 268 pH/□ at 1 MHz (247 pH/□ at 100 GHz). The sheet inductance of the bottom layer L_1 is 19.6 pH/□ at 1 MHz (19 pH/□ at 100 GHz). The inductance of the bottom grid layer is approximately 15 times lower than the inductance of the upper grid layer. This difference in inductance is primarily due to the difference in the line density of the layers. The line density of the bottom layer is 15 times higher, as determined by the line pitch of the layers $(150/10 = 15)$. The inductance of a single line is relatively insensitive to the aspect ratio of the line cross section. The inductance of a two-layer grid, however, varies significantly with signal frequency due to current redistribution, as discussed in Section III.

The inductive characteristics of a two-layer grid can also be analytically determined based on the simple model shown in Fig. 7. Assuming $L_{12} = 0$ as discussed in Section IV-B, the loop inductance of a two layer grid is

$$L_0 = \frac{L_1(R_2^2 + \omega^2 L_1 L_2) + L_2(R_1^2 + \omega^2 L_1 L_2)}{(R_1 + R_2)^2 + \omega^2 (L_1 + L_2)^2}. \quad (8)$$

At high frequencies, where the resistance of the grid layers has no influence on the current distribution between the layers, the grid inductance described by (8) asymptotically approaches the inductance of two ideal parallel inductors

$$L_0^{\mathrm{HF}} = \frac{L_1 L_2}{L_1 + L_2} = \frac{268 \times 19.6\ \mathrm{pH/\square}}{268 + 19.6} = 18.3\ \mathrm{pH/\square} \quad (9)$$

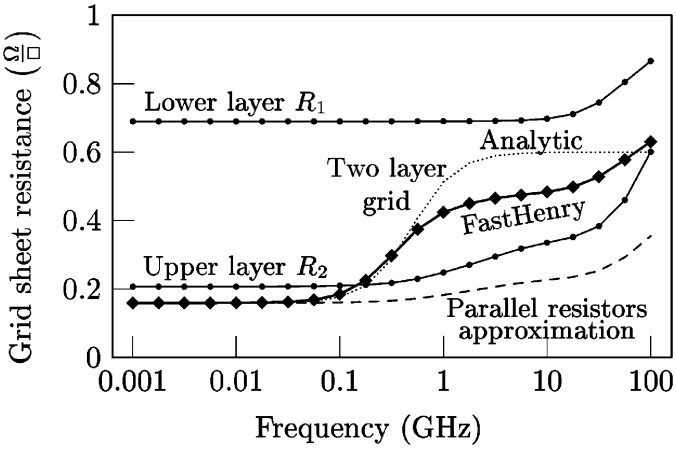

Fig. 12. Resistance of a two-layer grid versus signal frequency. The individual resistance of the two comprising grid layers and the parallel resistance of the individual layer resistances are shown for comparison.

in agreement with (5). At low frequencies, the grid inductance described by (8) approaches the low-frequency limit of the grid inductance

$$L_0^{\mathrm{LF}} = L_1 \left(\frac{R_2}{R_1 + R_2}\right)^2 + L_2 \left(\frac{R_1}{R_1 + R_2}\right)^2 \quad (10)$$

$$= 19.6\ \mathrm{pH/\square} \left(\frac{0.21}{0.69 + 0.21}\right)^2 + 268\ \mathrm{pH/\square} \left(\frac{0.69}{0.69 + 0.21}\right)^2 = 160\ \mathrm{pH/\square} \quad (11)$$

in agreement with (3).

The variation of the grid inductance with frequency according to the analytic model described by (8) is also illustrated in Fig. 11 by the dotted line. The analytic model satisfactorily describes the variation of grid inductance with frequency. The discrepancy between the analytic and FastHenry data at high frequencies is due to proximity effects which are not captured by the model shown in Fig. 7.

D. Resistive Characteristics of a Two-Layer Grid

The resistance of the two individual grid layers R_1 and R_2 and the resistance of the combined two-layer grid R_0 are shown in Fig. 12. The resistance of the individual grid layers remains constant up to high frequencies. The resistance of the upper layer begins to moderately increase from approximately 0.5 GHz due to significant proximity effects in very wide lines. The resistance of both layers sharply increase above approximately 20 GHz due to significant skin effect. Note that the resistance of the grid comprised of the two layers exhibits significantly greater variation with frequency than either individual layer.

Similar to the grid inductance, the resistive characteristics of a two layer grid can be analytically determined from the properties of the comprising grid layers

$$R_0 = \frac{R_1\left(R_1 R_2 + \omega^2 L_2^2\right) + R_2\left(R_1 R_2 + \omega^2 L_1^2\right)}{(R_1 + R_2)^2 + \omega^2 (L_1 + L_2)^2}. \quad (12)$$

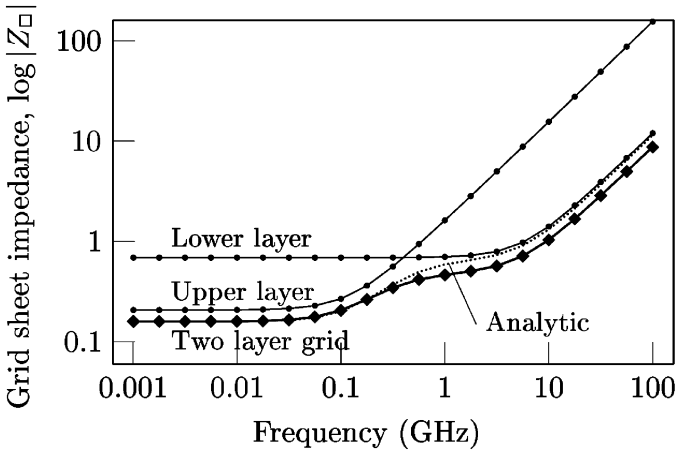

Fig. 13. Impedance magnitude of a two-layer grid versus signal frequency. Both the extracted (solid line) and analytic (dotted line) data are shown. The impedance of the two comprising grid layers is also shown.

The grid resistance versus frequency data based on the analytic model described by (12) is shown in Fig. 12 by the dotted line. The analytic solution describes well the general character of the resistance variation with frequency. At low frequencies, the resistance of the two-layer grid approaches the parallel resistance of two grid layers

$$R_0^{\mathrm{LF}} = R_1 \,||\, R_2 = \frac{R_1 R_2}{R_1 + R_2} = \frac{0.69 \times 0.21\ \Omega/\square}{0.69 + 0.21} = 0.16\ \Omega/\square \tag{13}$$

in agreement with (2). The high-frequency grid resistance asymptotically approaches

$$R_0^{\mathrm{HF}} = R_1 \left(\frac{L_2}{L_1 + L_2}\right)^2 + R_2 \left(\frac{L_1}{L_1 + L_2}\right)^2 \tag{14}$$

$$= 0.69\ \Omega/\square \left(\frac{268}{19.6 + 268}\right)^2 + 0.21\ \Omega/\square \left(\frac{19.6}{19.6 + 268}\right)^2 = 0.6\ \Omega/\square \tag{15}$$

in agreement with (6). This analytically calculated high-frequency resistance overestimates the FastHenry extracted resistance of 0.48 $\Omega/\square$ (at 10 GHz). The discrepancy is due to pronounced proximity and skin effects at high frequencies.

E. Variation of Impedance With Frequency in a Two-Layer Grid

Having determined the variation with frequency of the resistance and inductance in the previous sections, it is possible to characterize the frequency dependent impedance characteristics of a two-layer grid. The magnitude of the impedance calculated from the analytic models (8) and (12) is shown in Fig. 13 by the dotted line. Low-frequency values of the individual layer inductance, L_1 and L_2, and resistance, R_1, and R_2, are used in the analytic model. The impedance magnitude based on FastHenry extracted data is shown by the solid line. The extracted impedance of the individual grid layers is also shown for comparison. Note that the impedance characteristics of the individual layers shown in Fig. 13 bear close resemblance to the schematic graph shown in Fig. 3.

As discussed in Section III, the low-resistance upper grid dominates the impedance characteristics at low frequencies, while the low-inductance lower grid determines the impedance characteristics at high frequencies. The analytic model satisfactorily describes the frequency dependent impedance characteristics. The discrepancy between the analytic and extracted data at high frequencies is due to overestimation of the high-frequency inductance by the analytic model, as shown in Fig. 11.

V. Design Implications

The variation with frequency of the electrical properties of a multilayer grid has several design implications. Modeling the resistance of a multilayer grid as a parallel connection of individual layer resistances underestimates the high-frequency resistance of the grid. The parallel resistance model, therefore, underestimates the resistive IR voltage drops during fast current transients. Representing the multilayer grid inductance by the individual layer inductances connected in parallel is accurate only at very high frequencies. At lower frequencies, this model underestimates the grid inductance. Relatively low inductance and high resistance at high frequencies increase the damping factor of the power-distribution grid (proportional to $R/\sqrt{L}$), thereby preventing resonant oscillations in power distribution networks at high frequencies. Conversely, resonant oscillations are more likely at lower frequencies, where the inductance is relatively high and the resistance is low.

Multilayer grids with different grid layer impedance characteristics are well suited to distribute power in high speed integrated circuits. At low frequencies, where the grid impedance is dominated by the resistance, most of the current flows through the less resistive upper grid layers, decreasing the grid impedance. At high frequencies, where the grid impedance is dominated by the inductance, most of the current flows through the low-inductance lower layers. Over the entire frequency range, the current flow changes so as to minimize the impedance of the grid. These properties of multilayer power distribution grids support the design of power distribution networks with low impedance across a wide-frequency range, necessary in high-performance nanoscale integrated circuits.

The inductive properties of the interconnect changes the metal allocation strategy for global power distribution grids. In circuits based on resistance-only models, all of the metal area for the global power distribution is allocated in the upper layers with the lowest line resistance. The power interconnect in the lower metal layers connects the circuits to the global power grid and typically does not form continuous power grids. In multilayer grids, however, significant metal resources are required to form continuous grids in the lower metal layers. This difference is a direct consequence of the inductive behavior of interconnect at high frequencies. A significant fraction of the high density lower metal layers should be used to lower the high-frequency impedance of the power grid. In this manner, the frequency range of the grid impedance is extended to match the increased switching speeds of scaled nanometer transistors.

Redistribution of the grid current toward the lower layers at high frequencies increases the current density in the power and ground lines in the lower grid layers, degrading the elec-

tromigration reliability of the power distribution grid. The significance of these effects will increase as the frequency of the current delivered through the on-chip power distribution grid increases with higher operating speeds. An analysis of these effects is, therefore, necessary to ensure the integrity of high-speed nanoscale integrated circuits.

VI. Conclusion

Power distribution grids in nanoscale integrated circuits span many layers of interconnect with highly different electrical characteristics. The electrical characteristics of multilayer power-distribution grids are investigated in this paper. The upper metal layers comprised of thicker and wider lines have low resistance and high inductance; the lower metal layers comprised of thinner and narrower lines have relatively high resistance and low inductance. Inductive coupling between grid layers is shown to be insignificant in typical power distribution grids. Due to this difference in electrical properties, the impedance characteristics of multilayer grids vary significantly with frequency. As signal frequencies increase, the majority of the current flow shifts from the lower resistance upper layers to the lower inductance lower layers. The inductance of a multilayer grid, therefore, decreases with frequency, while the resistance increases with frequency. Thus, current distribution among the grid layers changes with frequency, minimizing the overall impedance of the power grid. This property of multilayer grids facilitates the design of low-noise power distribution networks in high-speed integrated circuits. A model to analytically determine the electrical properties of a multilayer grid from the inductive and resistive properties of the comprising grid layers is also described.

The implications of these electrical characteristics on the design of power distribution grids in high-speed nanoscale circuits are also discussed. The inductive behavior of interconnect lines at high frequency significantly changes the strategy for allocating power distribution interconnect resources among the layers of the interconnect stack. Formation of a dense and continuous power distribution grid in the lower metal layers is essential to lower the impedance of the power distribution grids at high frequencies. It is therefore imperative that the impedance characteristics of multilayer power distribution grids be carefully considered in the design of high speed nanoscale integrated circuits.

References

[1] *International Technology Roadmap for Semiconductors, 2002 Update*, 2002. Semiconductor Industry Association.

[2] A. V. Mezhiba and E. G. Friedman, *Power Distribution Networks in High Speed Integrated Circuits*. Norwell, MA: Kluwer, 2004.

[3] W. S. Song and L. A. Glasser, "Power distribution techniques for VLSI circuits," *IEEE J. Solid-State Circuits*, vol. SC-21, pp. 150–156, Feb. 1986.

[4] A. V. Mezhiba and E. G. Friedman, "Scaling trends of on-chip power distribution noise," in *Proc. ACM Int. Workshop System-Level Interconnect Prediction*, Apr. 2002, pp. 47–53.

[5] ——, "Scaling trends of on-chip power distribution noise," *IEEE Trans. VLSI Syst.*, vol. 12, pp. 386–394, Apr..

[6] D. A. Priore, "Inductance on silicon for sub-micron CMOS VLSI," in *Proc. IEEE Symp. VLSI Circuits*, May 1993, pp. 17–18.

[7] L.-R. Zheng and H. Tenhunen, "Effective power and ground distribution scheme for deep subrnicron high speed VLSI circuits," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. I, May 1999, pp. 537–540.

[8] A. V. Mezhiba and E. G. Friedman, "Inductive characteristics of power distribution grids in high speed integrated circuits," in *IEEE Int. Symp. Quality Electronic Design*, Mar. 2002, pp. 316–321.

[9] ——, "Inductive characteristics of power distribution grids in high speed integrated circuits," *IEEE Trans. VLSI Syst.*, vol. 10, pp. 762–776, Dec. 2002.

[10] ——, "Inductance/area/resistance tradeoffs in high performance power distribution grids," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. I, May 2002, pp. 101–104.

[11] ——, "Variation of inductance with frequency in high performance power distribution grids," in *IEEE Int. ASIC/SOC Conf.*, Sept. 2002, pp. 421–425.

[12] ——, "Frequency characteristics of high speed power distribution grids," *Analog Integrated Circuits Signal Processing*, vol. 35, no. 2/3, pp. 207–214, May/June 2003.

[13] ——, "Electrical characteristics of multilayer power distribution grids," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 5, May 2003, pp. 473–476.

[14] A. E. Ruehli, "Inductance calculations in a complex integrated circuit environment," *IBM J. Res. Develop.*, vol. 16, no. 5, pp. 470–481, Sept. 1972.

[15] M. Kamon, M. J. Tsuk, and J. White, "FastHenry: A multipole-accelerated 3-D inductance extraction program," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 1750–1758, Sept. 1994.

Andrey V. Mezhiba received the B.S. degree and Diploma with the M.S. degree in physics from the Moscow Institute of Physics and Technology, Russia, in 1994 and 1996, respectively, and recently received the Ph.D. degree in electrical and computer engineering at the University of Rochester, Rochester, NY, under the direction of Prof. Eby G. Friedman.

His research interests are in the areas of noise, signal integrity, and interconnect design, including on-chip inductive effects and the design of power distribution networks.

Eby G. Friedman (S'78–M'89–SM'90–F'00) received the B.S. degree from Lafayette College, Easton, PA, in 1979, and the M.S. and Ph.D. degrees from the University of California, Irvine, in electrical engineering, in 1981 and 1989, respectively.

From 1979 to 1991, he was with Hughes Aircraft Company, rising to the position of manager of the Signal Processing Design and Test Department, responsible for the design and test of high-performance digital and analog ICs. He has been with the Department of Electrical and Computer Engineering at the University of Rochester since 1991, where he is a Distinguished Professor, the Director of the High Performance VLSI/IC Design and Analysis Laboratory, and the Director of the Center for Electronic Imaging Systems. For the academic year 2000 to 2001, he was on sabbatical at the Technion—Israel Institute of Technology. His current research and teaching interests are in high-performance synchronous digital and mixed-signal microelectronic design and analysis with application to high-speed portable processors and low-power wireless communications. He is the author of more than 250 papers and book chapters, several patents, and the author or editor of seven books in the fields of high-speed and low-power CMOS design techniques, high-speed interconnect, and the theory and application of synchronous clock distribution networks.

Dr. Friedman is the Chair of the IEEE Transactions on Very Large Scale Integration Systems Steering Committee, Regional Editor of the *Journal of Circuits, Systems and Computers*, a member of the editorial boards of the Proceedings of the IEEE, *Analog Integrated Circuits and Signal Processing*, *Microelectronic Journal*, and *Journal of VLSI Signal Processing*, a member of the Circuits and Systems (CAS) Society Board of Governors, and a member of the technical program committee of a number of conferences. He previously was the Editor-in-Chief of the IEEE Transactions on Very Large Scale Integration (VLSI) Systems, a member of the editorial board of the IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, CAS liaison to the Solid-State Circuits Society, Chair of the VLSI Systems and Applications CAS Technical Committee, Chair of the Electron Devices Chapter of the IEEE Rochester Section, Program or Technical Chair of several IEEE conferences, guest editor of several special issues in a variety of journals, and a recipient of the Howard Hughes Masters and Doctoral Fellowships, an IBM University Research Award, an Outstanding IEEE Chapter Chairman Award, and a University of Rochester College of Engineering Teaching Excellence Award. He is also a Senior Fulbright Fellow.