Scaling Trends of On-Chip Power Distribution Noise

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***Abstract*—The design of power distribution networks in high-performance integrated circuits has become significantly more challenging with recent advances in process technologies. As on-chip currents exceed tens of amperes and circuit clock periods are reduced well below a nanosecond, the signal integrity of on-chip power supply has become a primary concern in the integrated circuit design. The scaling behavior of the inductive and resistance voltage drops across the on-chip power distribution networks is the subject of this paper. The existing work on power distribution noise scaling is reviewed and extended to include the scaling behavior of the inductance of the on-chip global power distribution networks in high-performance flip-chip packaged integrated circuits. As the dimensions of the on-chip devices are scaled by S, where $S > 1$, the resistive voltage drop across the power grids remains constant and the inductive voltage drop increases by S, if the metal thickness is maintained constant. Consequently, the signal-to-noise ratio decreases by S in the case of resistive noise and by S^2 in the case of inductive noise. As compared to the constant metal thickness scenario, ideal interconnect scaling of the global power grid mitigates the unfavorable scaling of the inductive noise but exacerbates the scaling of resistive noise by a factor of S. On-chip inductive noise will, therefore, become of greater significance with technology scaling. Careful tradeoffs between the resistance and inductance of the power distribution networks will be necessary in nanometer technologies to achieve minimum power supply noise.**

***Index Terms*—Power distribution, power supply noise, technology scaling.**

I. Introduction

THE scaling of CMOS technology is expected to continue for at least another ten years [1]. The ongoing miniaturization of integrated circuit (IC) feature sizes has placed significant requirements on the power and ground distribution networks. Circuit integration densities rise with each very deep-submicrometer (VDSM) technology generation due to smaller devices and larger dies; the current density and the total current increase accordingly. At the same time, the higher switching speed of smaller transistors produces faster current transients in the power distribution network. The higher currents cause large ohmic IR voltage drops while the fast current transients cause large inductive $L(dI/dt)$ voltage drops (ΔI noise) in the power distribution networks. Power distribution networks must be designed to minimize these voltage drops, maintaining the local supply voltage within specified design margins. If the power supply voltage sags too low, the performance and functionality of the circuit will be severely compromised. Alternatively, excessive overshoot of the supply voltage can affect circuit reliability. Further exacerbating these problems is the decrease in noise margins with each new generation of VDSM process technology.

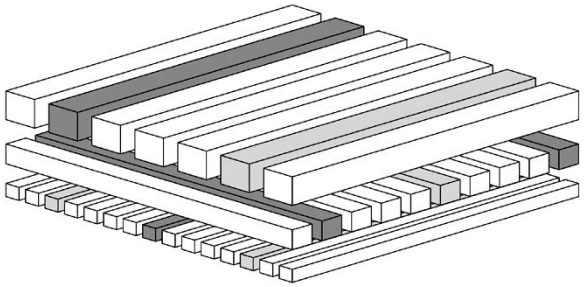

Fig. 1. Multilayer interconnect with the power distribution grid highlighted; the ground lines are light grey, the power lines are dark grey, and the signal lines are white.

Insuring adequate signal integrity of the power supply has become a primary design issue in high-performance, high-complexity digital integrated circuits. A significant fraction of the on-chip resources is dedicated to achieve this objective. Global on-chip power distribution networks are typically designed at the early stages of the design process, when little is known about the power demands at specific locations on an IC. Furthermore, allocating additional wiring resources for the global power distribution network at the later stages of the design process in order to improve the local electrical characteristics of the power network is likely to create routing problems which can be prohibitively expensive to correct. For these reasons, power distribution networks tend to be conservatively designed [2], sometimes using more than a third of the on-chip metal resources [3], [4].

Power distribution networks in high-performance digital ICs are commonly structured as a multilayer grid. In such a grid, straight power/ground (P/G) lines in each metallization layer span the entire die (or a large functional unit) and are orthogonal to the lines in the adjacent layers. The power and ground lines typically alternate in each layer. Vias are used to connect a power (ground) line to another power (ground) line at the overlap sites. The power grid concept is illustrated in Fig. 1, where three layers of interconnect are depicted with the power lines shown in dark grey and the ground lines shown in light grey. The power/ground lines are surrounded by signal lines.

The scaling trend of the voltage drop across the on-chip power distribution grids is, therefore, of practical interest. The results

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TABLE I
IDEAL SCALING OF CMOS CIRCUITS [5]

Parameter	Scaling factor
Device dimensions	$1/S$
Doping concentrations	S
Voltage levels	$1/S$
Current per device	$1/S$
Gate load	$1/S$
Gate delay	$1/S$
Device area	$1/S^2$
Device density	S^2
Power per device	$1/S^2$
Power density	1
Total capacitance	SS_C^2
Total power	S_C^2
Total current	SS_C^2

of this scaling analysis depend upon various assumptions. Existing scaling analyses of power distribution noise are reviewed and compared along with any relevant assumptions. The scaling of the inductance of an on-chip power distribution network as discussed here extends the existing material presented in the literature. Scaling trends of on-chip power supply noise in ICs packaged in high-performance flip-chip packages are the focus of this investigation.

The paper is organized as follows. Related existing work is reviewed in Section II. The interconnect characteristics assumed in the analysis are discussed in Section III. The model of the on-chip power distribution noise used in the analysis is described in Section IV. The scaling of power noise is analyzed in Section V. Implications of the scaling analysis are discussed in Section VI. The conclusions are summarized in Section VII.

II. BACKGROUND

Ideal scaling of CMOS transistors was first described by Dennard *et al.* in 1974 [5]. Assuming a scaling factor S, where $S > 1$, all transistor dimensions uniformly scale as $1/S$, the supply voltage scales as $1/S$, and the doping concentrations scale as S. This "ideal" scaling maintains the electric fields within the device constant and ensures a proportional scaling of the *I-V* characteristics. Under the ideal scaling paradigm, the transistor current scales as $1/S$, the transistor power decreases as $1/S^2$, and the transistor density increases as S^2. The transistor switching time decreases as $1/S$, the power per circuit area remains constant, while the current per circuit area scales as S. The die dimensions increase by a chip dimension scaling factor S_C. The total capacitance of the on-chip devices and the circuit current both increase by SS_C^2 while the circuit power increases by S_C^2. The scaling of interconnect was first described by Saraswat and Mohammadi [6]. These ideal scaling relationships are summarized in Table I.

Several research results have been published on the impact of technology scaling on the integrity of the IC power supply [7]–[10]. The published analyses differ in the assumptions concerning the on-chip and package level interconnect characteristics. The analysis can be classified according to several categories: whether resistive IR or inductive $L(dI/dt)$ noise is considered, whether wire-bond or flip-chip packaging is assumed, and whether packaging or on-chip interconnect parasitic impedances are assumed dominant. Traditionally, the package-level parasitic inductance (the bond wires, lead frames, and pins) has dominated the total inductance of the power distribution system while the on-chip resistance of the power lines has dominated the total resistance of the power distribution system. The resistive noise has therefore been associated with the resistance of the on-chip interconnect and the inductive noise has been associated with the inductance of the off-chip packaging [9], [11], [12].

The scaling behavior of the resistive voltage drop in a wire bonded integrated circuit of constant size has been investigated by Song and Glasser in [7]. Assuming that the interconnect thickness scales as $1/S$, the ratio of the supply voltage to the resistive noise, i.e., the signal-to-noise ratio (SNR) of the power supply voltage, scales as $1/S^3$ under ideal scaling (as compared to $1/S^4$ under constant voltage scaling). Song and Glasser proposed a multilayer interconnect stack to address this problem. Assuming that the top metal layer has a constant thickness, scaling of the power supply signal-to-noise ratio improves by a power of S as compared to standard interconnect scaling.

Bakoglu [8] investigated the scaling of both resistive and inductive noise in wire-bonded ICs considering the increase in die size by S_C with each technology generation. Under the assumption of ideal interconnect scaling (i.e., the number of interconnect layers remains constant and the thickness of each layer is reduced as $1/S$), the SNR of the resistive noise decreases as $1/S^4S_C^2$. The SNR of the inductive noise due to the parasitic impedances of the packaging decreases as $1/S^4S_C^3$. These estimates of the SNR are made under the assumption that the number of interconnect levels increases as S. This assumption scales the on-chip capacitive load, average current, and, consequently, the SNR of both the inductive and resistive noise by a factor of S. Bakoglu also considered an improved scaling situation where the number of chip-to-package power connections increases as SS_C^2, effectively assuming flip-chip packaging. In this case, the resistive SNR_R scales as 1 assuming that the thickness of the upper metal levels is inversely scaled as S. The inductive SNR_L scales as $1/S$ under the assumption that the effective inductance per power connection scales as $1/S^2$.

A detailed overview of modeling and mitigation of package-level inductive noise is presented by Larsson [9]. The SNR of the inductive noise is shown to decrease as $1/S^2S_C$ under the assumption that the number of interconnect levels remains constant and the number of chip-to-package power-ground connections increases as SS_C. The results and key assumptions of the power supply noise scaling analyses are summarized in Table II.

The effect of the flip-chip pad density on the resistive drop in power supply grids has been investigated by Arledge and Lynch in [10]. All other conditions being equal, the maximum resistive drop is proportional to the square of the pad pitch. Based on this trend, a pad density of 4000 pads/cm^2 is the minimum density required to assure an acceptable on-chip IR drop and I/O signal density at the 50-nm technology node [10].

Nassif and Fakhouri describe an analytical expression relating the maximum power distribution noise to the principal

TABLE II
SCALING ANALYSES OF POWER DISTRIBUTION NOISE

Scaling analysis	Noise type	Noise scaling	SNR scaling	Analysis assumptions	
Glasser and Song [7]	On-chip IR noise	S^2	$1/S^3$	Ideal interconnect scaling	Wire-bond package, fixed die size
		S	$1/S^2$	Thickness of the top metal remains constant	
Bakoglu [8]	On-chip IR noise	$S^3S_C^2$	$1/S^4S_C^2$	Ideal interconnect scaling, wire-bond package (the number of power connections is constant)	Current and capacitance scale as $S^2S_C^2$ (due to the scaling of the number of metal levels by S) as compared to SS_C^2
		$1/S$	1	Reverse interconnect scaling ($\propto S$), the number of power connections scale as SS_C^2 (flip-chip)	
	Package $L\frac{dI}{dt}$ noise	$S^3S_C^3$	$1/S^4S_C^3$	The number of power connections remains constant, inductance per connections increases as S_C	
		1	$1/S$	Number of power connections scale as SS_C^2 (flip-chip), inductance per connection scale as $1/S^2$	
Larsson [9]	Package $L\frac{dI}{dt}$ noise	SS_C	$1/S^2S_C$	Wire-bond package, number of package connections increases as SS_C	
Mezhiba and Friedman	On-chip IR noise	1	$1/S$	Metal thickness remains constant	Area array flip-chip package, pad pitch scales as $1/\sqrt{S}$ (*i.e.*, the number of power connections scales as SS_C^2)
		S	$1/S^2$	Ideal interconnect scaling	
	On-chip $L\frac{dI}{dt}$ noise	S	$1/S^2$	Metal thickness remains constant	
		1	$1/S$	Ideal interconnect scaling	

design and technology characteristics [13]. The expression is based on a lumped model similar to the model shown in Fig. 4. The noise is shown to increase rapidly with technology scaling based on the ITRS predictions [14]. Assuming constant inductance, a reduction of the power grid resistance and an increase in the decoupling capacitance are predicted to be the most effective approaches to decreasing the power distribution noise.

III. INTERCONNECT CHARACTERISTICS

The power noise scaling trends depend substantially on the interconnect characteristics assumed in the analysis. The interconnect characteristics are described in this section. The assumptions concerning the scaling of the global interconnect are discussed in Section III-A. The variation of the grid inductance with interconnect scaling is described in Section III-B. Flip-chip packaging characteristics are discussed in Section III-C. The impact of the on-chip capacitance on the results of the analysis is discussed in Section III-D.

A. Global Interconnect Characteristics

The scaling of the cross-sectional dimensions of the on-chip global power lines directly affects the power distribution noise. Two scenarios of global interconnect scaling are considered here.

In the first scenario, the thickness of the top interconnect layers (where the conductors of the global power distribution networks are located) is assumed to remain constant. Through several recent technology generations, the thickness of the global interconnect layers has not been scaled in proportion to the minimum local line pitch due to power distribution noise and interconnect delay considerations. This behavior is in agreement with the 1997 edition of the International Technology Roadmap for Semiconductors (ITRS) [15], [16], where the minimum pitch and thickness of the global interconnect are assumed constant.

In the second scenario, the thickness and minimum pitch of the global interconnect layers are scaled down in proportion to the minimum pitch of the local interconnect. This assumption is in agreement with the more recent editions of the ITRS [1], [14]. Scaling of the global interconnect in future technologies

is therefore expected to evolve in the design envelope delimited by these two scenarios.

The number of metal layers and the fraction of metal resources dedicated to the power distribution network are also assumed constant. The ratio of the diffusion barrier thickness to the copper interconnect core is assumed to remain constant with scaling. The increase in resistivity of the interconnect due to electron scattering at the interconnect surface interface (significant at line widths below 45 nm [1]) is neglected for relatively thick global power lines.

Under the aforementioned assumptions, in the constant metal thickness scenario, the effective sheet resistance of the global power distribution network remains constant with technology scaling. In the scenario of scaled metal thickness, the grid sheet resistance increases with technology scaling by a factor of S.

B. Scaling of the Grid Inductance

The inductive properties of power distribution grids are investigated in [17] and [18]. It is shown that the inductance of the power grids with alternating power and ground lines behaves analogously to the grid resistance. That is, the grid inductance increases linearly with the grid length and decreases inversely linearly with the number of lines in the grid. This linear behavior is due to the periodic structure of the alternating power and ground grid lines. The long range inductive coupling of a specific (signal or power) line to a power line is cancelled out by the coupling to the ground lines adjacent to the power line, which carry current in the opposite direction [17], [19]. Inductive coupling in periodic grid structures, therefore, is effectively a short range interaction. Similar to the grid resistance, the grid inductance can be conveniently expressed as a dimension independent grid sheet inductance $L_{\square}$ [17], [20]. The inductance of a specific grid is obtained by multiplying the sheet inductance by the grid length and dividing by the grid width. The grid sheet inductance can be approximated as [17]

$$L_{\square} = 0.8P\left(\ln\frac{P}{T+W}+\frac{3}{2}\right)\frac{\mu\mathrm{H}}{\square} \tag{1}$$

where W, T, and P are the width, thickness, and pitch of the grid lines, respectively. The sheet inductance is proportional to the line pitch P. The line density is reciprocal to the line pitch. A smaller line pitch means higher line density and more parallel paths for current flow. The sheet inductance, however, is relatively insensitive to the cross-sectional dimensions of the lines, as the inductance of the individual lines is similarly insensitive to these parameters. Note that while the sheet resistance of the power grid is determined by the metal conductivity and the net cross-sectional area of the lines, the sheet inductance of the grid is determined by the line pitch and the ratio of the pitch to the line width and thickness.

In the constant metal thickness scenario, the sheet inductance of the power grid remains constant since the routing characteristics of the global power grid do not change. In the scaled thickness scenario, the line pitch, width, and thickness are reduced by S, increasing the line density and the number of parallel current paths. The sheet inductance therefore decreases by a factor of S, according to (1).

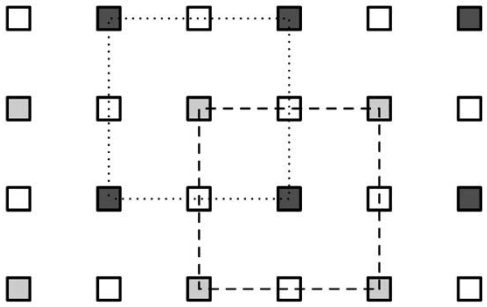

Fig. 2. An area array of on-chip power/ground I/O pads. The power pads are colored dark gray, the ground pads are colored light gray, and the signal pads are white. The current distribution area of the power pad (i.e., the power distribution cell) in the center of the figure is delineated by the dashed line. The current distribution area of the ground pad in the center of the figure is delineated by the dotted line.

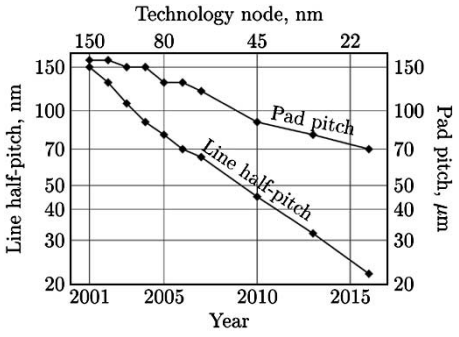

Fig. 3. Decrease in flip-chip pad pitch with technology generations as compared to the local interconnect half pitch.

C. Flip-Chip Packaging Characteristics

In a flip-chip package, the integrated circuit and the package are interconnected via an area array of solder bumps mounted onto the on-chip I/O pads [21]. The power supply current enters the on-chip power distribution network from the power-ground pads. A view of the on-chip area array of power-ground pads is shown in Fig. 2.

One of the main goals of this work is to estimate the significance of the *on-chip* inductive voltage drop in comparison to the on-chip resistive voltage drop. Therefore, all of the power-ground pads of a flip-chip packaged IC are assumed to be equipotential, i.e., the variation in the voltage levels among the pads is considered negligible as compared to the noise within the on-chip power distribution network. For the purpose of this scaling analysis, a uniform power consumption per die area is assumed. Under these assumptions, each power (ground) pad supplies power (ground) current only to those circuits located in the area around the pad, as shown in Fig. 2. This area is referred to as a power distribution cell (or power cell). The edge dimensions of each power distribution cell are proportional to the pitch of the power-ground pads. The size of the power cell area determines the effective distance of the on-chip distribution of the power current. The power distribution scaling analysis becomes independent of die size.

An important element of this analysis is the scaling of the flip-chip technology. The rate of decrease in the pad pitch and the rate of reduction in the local interconnect half-pitch are compared in Fig. 3, based on the ITRS [1]. At the 150 nm line

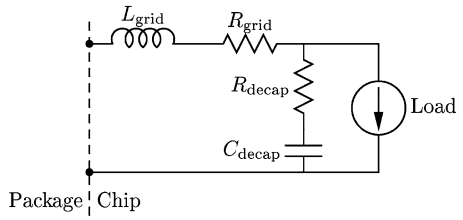

Fig. 4. A simple model of the on-chip power distribution network with a power load and a decoupling capacitance.

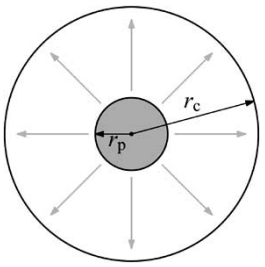

Fig. 5. A model of the power distribution cell. Power supply current spreads out from the power pad in the center of the cell to the cell periphery, as shown by the arrows.

half-pitch technology node, the pad pitch P is 160 μm. At the 32–nm node, the pad pitch is forecasted to be 80 μm. That is, the linear density of the pads doubles for a fourfold reduction in circuit feature size. The pad size and pitch P, therefore, scale as $1/\sqrt{S}$ and the area density ($\propto 1/P^2$) of the pads increases as S with each technology generation. Interestingly, one of the reasons given for this relatively infrequent change in the pad pitch (as compared with the introduction of new CMOS technology generations) is the cost of the test probe head [1]. The maximum density of the flip-chip pads is assumed to be limited by the pad pitch. Although, the number of on-chip pads is forecasted to remain constant, some recent research has predicted that the number of on-chip power-ground pads will increase due to electromigration and resistive noise considerations [10], [22].

D. Impact of On-Chip Capacitance

On-chip capacitors are used to reduce the impedance of the power distribution grid lines as seen from the load terminals. A simple model of an on-chip power distribution grid with a power load and a decoupling capacitor is shown in Fig. 4. The on-chip loads are switched within tens of picoseconds in modern semiconductor technologies. The frequency spectrum of the load current therefore extends well beyond 10 GHz. The on-chip decoupling capacitors shunt the load current at the highest frequencies. The bulk of the power current bypasses the on-chip distribution network at these frequencies. At the lower frequencies, however, the capacitor impedance is relatively high and the bulk of the current flows through the on-chip power distribution network. The decoupling capacitors therefore serve as a low pass filter for the power current.

Describing the same effect in the time domain, the capacitors supply the (high frequency) current to the load during a switching transient. To prevent excessive power noise, the charge on the decoupling capacitor should be replenished by the (lower frequency) current flowing through the power distribution network before the next switching of the load, i.e., typically within a clock period. The effect of the on-chip decoupling capacitors is therefore included in the model by assuming that the current transients within the on-chip power distribution network are characterized by the clock frequency of the circuit, rather than by the switching times of the on-chip load circuits. Estimates of the resistive voltage drop are based on the average power current, which is not affected by the on-chip decoupling capacitors.

IV. Model of Power Supply Noise

The following simple model is utilized in the scaling analysis of the on-chip power distribution noise. A power distribution cell is modeled as a circle of radius r_{c} with a constant current consumption per area I_{a}, as described by Arledge and Lynch [10]. The model is depicted in Fig. 5. The total current of the cell is $I_{\text{cell}} = I_{\text{a}} \cdot \pi r_{\text{c}}^2$. The power network current is distributed from a circular pad of radius r_{p} at the center of the cell. The global power distribution network has an effective sheet resistance $\rho_{\square}$. The incremental voltage drop dV_R across the elemental circular resistance $\rho_{\square}\, dr/2\pi r$ is due to the current $I_{\text{a}}(\pi r_{\text{c}}^2 - \pi r^2)$ flowing through this resistance toward the periphery of the cell. The voltage drop at the periphery of the power distribution cell is

$$\begin{aligned}\Delta V_R &= \int_{r_{\text{p}}}^{r_{\text{c}}} dV_R = \int_{r_{\text{p}}}^{r_{\text{c}}} I(r) \cdot dR(r) \\ &= \int_{r_{\text{p}}}^{r_{\text{c}}} \pi \left(r_{\text{c}}^2 - r^2\right) I_{\text{a}} \cdot \rho_{\square} \frac{dr}{2\pi r} \\ &= I_{\text{a}} \pi r_{\text{c}}^2 \rho_{\square} \cdot \frac{1}{2\pi} \left(\ln \frac{r_{\text{c}}}{r_{\text{p}}} + \frac{r_{\text{p}}^2}{2r_{\text{c}}^2} - \frac{1}{2} \right) \\ &= I_{\text{cell}} \rho_{\square} \cdot C \left(\frac{r_{\text{c}}}{r_{\text{p}}} \right). \end{aligned} \tag{2}$$

The resistive voltage drop is proportional to the product of the total cell current I_{cell} and the effective sheet resistance $\rho_{\square}$ with the coefficient C dependent only on the $r_{\text{c}}/r_{\text{p}}$ ratio. The ratio of the pad pitch to the pad size is assumed to remain constant. The coefficient C, therefore, does not change with technology scaling.

The properties of the grid inductance are analogous to the properties of the grid resistance as discussed in Section III-A. Therefore, analogous to the resistive voltage drop ΔV_R discussed above, the inductive voltage drop ΔV_L is proportional to the product of the sheet inductance $L_{\square}$ of the global power grid and the magnitude of the cell transient current dI_{cell}/dt

$$\Delta V_L = L_{\square} \frac{dI_{\text{cell}}}{dt} \cdot C \left(\frac{r_{\text{c}}}{r_{\text{p}}} \right). \tag{3}$$

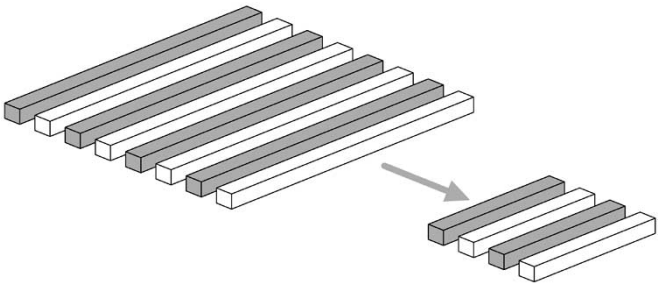

Fig. 6. The scaling of a power distribution grid over four technology generations according to the constant metal thickness scenario. The cross-sectional dimensions of the power lines remain constant. The size of the power distribution cell, represented by the size of the square grid, is halved.

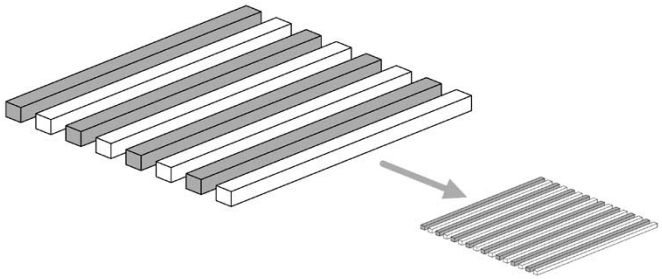

Fig. 7. The scaling of a power distribution grid over four technology generations according to the scaled metal thickness scenario. The cross-sectional dimensions of the power lines are reduced in proportion to the minimum feature size by a factor of four. The size of the power distribution cell, represented by the size of the square grid, is halved.

V. Power Supply Noise Scaling

An analysis of the on-chip power supply noise is presented in this section. The analysis is based on the model described in Sections III and IV. Ideal scaling of the power distribution noise in the constant thickness scenario is discussed in Section V-A. Ideal scaling of the noise in the scaled thickness scenario is analyzed in Section V-B. Scaling of the power distribution noise based on the ITRS projections is discussed in Section V-C.

A. Analysis of Constant Metal Thickness Scenario

The scaling of a power distribution grid over four technology generations according to the constant metal thickness scenario is depicted in Fig. 6. The minimum feature size is reduced by $\sqrt{2}$ with each generation. The minimum feature size over four generations is therefore reduced by four, i.e., $(\sqrt{2})^4 = 4$, while the size of the power distribution cell (represented by the size of the square grid) is halved ($\sqrt{4} = 2$). As the cross-sectional dimensions of the power lines are maintained constant in this scenario, both the sheet resistance $\rho_\square$ and sheet inductance $L_\square$ of the power distribution grid remain constant with scaling under these conditions.

The cell current I_{cell} is the product of the area current density I_{a} and the cell area πr_{c}^2. The current per area I_{a} scales as S; the area of the cell is proportional to P^2 which scales as $1/S$. The cell current I_{cell}, therefore, remains constant (i.e., scales as 1). The resistive drop ΔV_R, therefore, scales as $I_{\text{cell}} \cdot \rho_\square \propto 1 \cdot 1 \propto 1$. The resistive SNR_R^{I} of the power supply voltage, consequently, decreases with scaling as

$$\text{SNR}_R^{\text{I}} = \frac{V_{\text{dd}}}{\Delta V_R} \propto \frac{\frac{1}{S}}{1} \propto \frac{1}{S}. \tag{4}$$

This scaling trend agrees with the trend described by Bakoglu in the improved scaling situation [8]. A faster scaling of the on-chip current as described by Bakoglu is offset by increasing the interconnect thickness by S which reduces the sheet resistance $\rho_\square$ by S. This trend is more favorable as compared to the $1/S^2$ dependence established by Song and Glasser [7]. The improvement is due to the decrease in the power cell area of a flip-chip IC by a factor of S whereas a wire-bonded die of constant area is assumed in [7].

The transient current dI_{cell}/dt scales as $I_{\text{cell}}/\tau \propto 1/(1/S) \propto S$, where $\tau \propto 1/S$ is the transistor switching time. The inductive voltage drop ΔV_L, therefore, scales as $L_\square \cdot dI_{\text{cell}}/dt \propto 1 \cdot S$. The inductive SNR_L^{I} of the power supply voltage decreases with scaling as

$$\text{SNR}_L^{\text{I}} = \frac{V_{\text{dd}}}{\Delta V_L} \propto \frac{\frac{1}{S}}{S} \propto \frac{1}{S^2}. \tag{5}$$

The relative magnitude of the inductive noise therefore increases by a factor of S faster as compared to the resistive noise. Estimates of the inductive and resistive noise described by Bakoglu also differ by a factor of S [8].

B. Analysis of the Scaled Metal Thickness Scenario

The scaling of a power distribution grid over four technology generations according to the scaled metal thickness scenario is depicted in Fig. 7. In this scenario, the cross-sectional dimensions of the power lines are reduced in proportion to the minimum feature size by a factor of four, while the size of the power distribution cell is halved. Under these conditions, the sheet resistance $\rho_\square$ of the power distribution grid increases by S, while the sheet inductance $L_\square$ of the power distribution grid decreases by S with technology scaling.

Analogous to the constant metal thickness scenario, the cell current I_{cell} remains constant. The resistive drop ΔV_R, therefore, scales as $I_{\text{cell}} \cdot \rho_\square \propto 1 \cdot S \propto S$. The resistive SNR_R^{II} of the power supply voltage, consequently, decreases with scaling as

$$\text{SNR}_R^{\text{II}} = \frac{V_{\text{dd}}}{\Delta V_R} \propto \frac{\frac{1}{S}}{S} \propto \frac{1}{S^2}. \tag{6}$$

As discussed in the previous section, the transient current dI_{cell}/dt scales as $I_{\text{cell}}/\tau \propto S$. The inductive voltage drop ΔV_L, therefore, scales as $L_\square \cdot dI_{\text{cell}}/dt \propto 1/S \cdot S \propto 1$. The inductive SNR_L^{II} of the power supply voltage decreases with scaling as

$$\text{SNR}_L^{\text{II}} = \frac{V_{\text{dd}}}{\Delta V_L} \propto \frac{\frac{1}{S}}{1} \propto \frac{1}{S}. \tag{7}$$

The rise of the inductive noise is mitigated if ideal interconnect scaling is assumed and the thickness, width, and pitch of the global power lines are scaled as $1/S$. In this scenario, the density of the global power lines increases as S and the sheet inductance $L_\square$ of the global power distribution grid decreases as $1/S$, mitigating the inductive noise and SNR_L by S. The sheet resistance of the power distribution grid, however, increases as S, exacerbating the resistive noise and SNR_R by a factor of S.

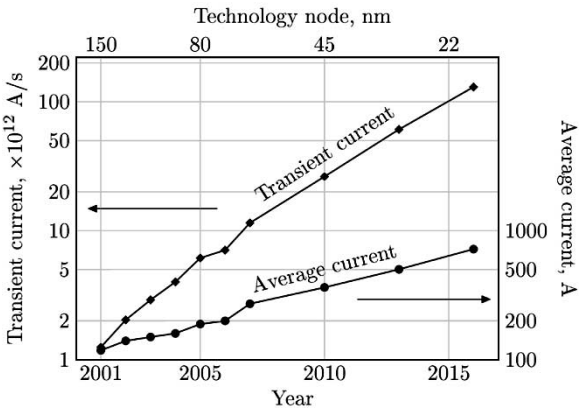

Fig. 8. Increase in power current demands of high-performance microprocessors with technology scaling, according to the ITRS. The average current is the ratio of the circuit power to the supply voltage. The transient current is the product of the average current and the on-chip clock rate, $2\pi f_{\mathrm{clk}}$.

Currently, the resistive parasitic impedance dominates the total impedance of on-chip power distribution networks. Ideal scaling of the upper interconnect levels will therefore increase the overall power distribution noise. However, as CMOS technology approaches the nanometer range and the inductive and resistive voltage drops become comparable, judicious tradeoffs between the resistance and inductance of the power networks will be necessary to achieve the minimum noise level.

C. ITRS Scaling

Although, the ideal scaling analysis allows the comparison of the rates of change of both resistive and inductive voltage drops, it cannot be used to estimate the *ratio* of these quantities for direct assessment of their relative significance. Furthermore, practical scaling does not accurately follow the concept of ideal scaling due to material and technological limitations. An estimate of the ratio of the inductive to resistive voltage drop is therefore conducted in this Section based on the projected 2001 ITRS data [1].

Forecasted demands in the supply current of high-performance microprocessors are shown in Fig. 8. Both the average current and the transient current are rising exponentially with technology scaling. The rate of increase in the transient current is more than double the rate of increase in the average current as indicated by the slope of the trend lines depicted in Fig. 8. This behavior is in agreement with ideal scaling trends. The faster rate of increase in the transient current as compared to the average current is due to rising clock frequencies. The transient current in modern high-performance processors is approximately one tera ampere per second $(10^{12}$ A/s) and is expected to rise, reaching hundreds of tera amperes per second. Such a high magnitude of the transient current is caused by switching hundreds of amperes within a fraction of a nanosecond.

In order to translate the projected current requirements into supply noise voltage trends, a case study interconnect structure is considered. The square grid structure shown in Fig. 9 is used here to serve as a model of the on-chip power distribution grid. The square grid consists of interdigitated power and ground lines with a 1 μm $\times$ 1 μm cross section and a 1 μm line

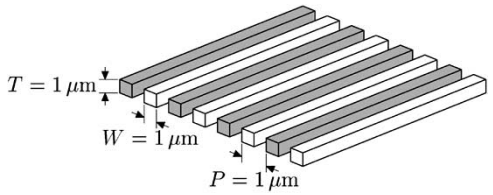

Fig. 9. Power distribution grid used to estimate trends in the power supply noise.

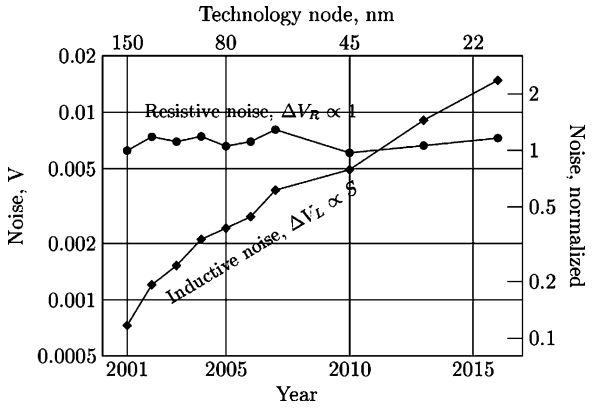

Fig. 10. Scaling trends of resistive and inductive power supply noise under the constant metal thickness scenario.

spacing. The length and width of the grid are equal to the size of a power distribution cell. The grid sheet inductance is 1.8 pH per square, and the grid sheet resistance is 0.16 Ω per square. The size of the power cell is assumed to be twice the pitch of the flip-chip pads, reflecting that only half of the total number of pads are used for the power and ground distribution as forecasted by the ITRS for high-performance ASICs.

The electrical properties of this structure are similar to the properties of the global power distribution grid covering a power distribution cell with the same routing characteristics. Note that the resistance and inductance of the *square* grid are independent of grid dimensions [20] (as long as the dimensions are several-fold greater than the line pitch). The average and transient currents flowing through the grid, however, are scaled from the IC current requirements shown in Fig. 8 in proportion to the area of the grid. The current flowing through the square grid is, therefore, the same as the current distributed through the power grid within the power cell. The power current enters and leaves from the same side of the grid, assuming the power load is connected at the opposite side. The voltage differential across this structure caused by the average and transient currents produces, respectively, on-chip resistive and inductive noise. The square grid has the same inductance to resistance ratio as the global distribution grid with the same line pitch, thickness, and width. Hence, the square grid has the same inductive to resistive noise ratio. The square grid model also produces the same rate of increase in the noise because the current is scaled proportionately to the area of the power cell.

The resulting noise trends under the constant metal thickness scenario are illustrated in Fig. 10. As discussed in Section III, the area of the grid scales as $1/S$. The current area density increases as S. The total average current of the grid, therefore, remains constant. The resistive noise also remains approximately

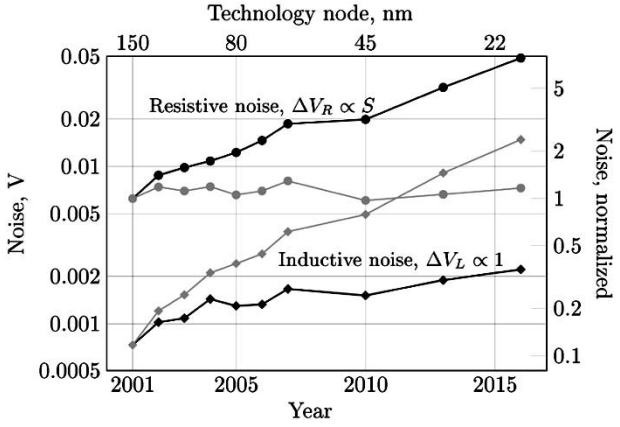

Fig. 11. Scaling trends of resistive and inductive power supply noise under the scaled metal thickness interconnect scaling scenario. The trends of the constant metal thickness scenario are also displayed in light gray for comparison.

constant, as shown in Fig. 10. The inductive noise, alternatively, rises steadily and becomes comparable to the resistive noise at approximately the 45-nm technology node. These trends are in reasonable agreement with the ideal scaling predictions discussed in Section V-A.

The inductive and resistive voltage drops in the scaled metal thickness scenario are shown in Fig. 11. The increase in inductive noise with technology scaling is limited, while the resistive noise increases by an order of magnitude. This behavior is similar to the ideal scaling trends for this scenario, as discussed in Section V-B.

Note that the structure depicted in Fig. 9 has a lower inductance to resistance ratio as compared to typical power distribution grids because the power and ground lines are relatively narrow and placed adjacent to each other, reducing the area of the current loop and increasing the grid resistance [18], [20]. The width of a typical global power line varies from tens to a few hundreds of micrometers, resulting in a significantly higher inductance to resistance ratio. The results shown in Figs. 10 and 11 can be readily extrapolated to different grid configurations, using the expression for the grid sheet inductance, (1).

Several factors offset the underestimation of the relative magnitude of the inductive noise due to the relatively low inductance to resistance ratio of the model shown in Fig. 9. If the global power distribution grid is composed of several layers of interconnect, the lines in the lower interconnect levels have a smaller pitch and thickness, significantly reducing the inductance to resistance ratio at high frequencies [23]. The transient current is conservatively approximated as the product of the average current I_{avg} and the angular clock frequency $2\pi f_{\text{clk}}$. This estimate, while serving as a useful scaling parameter, tends to overestimate the absolute magnitude of the current transients, increasing the ratio of the inductive and resistive voltage drops.

VI. Implications of Noise Scaling

As described in the previous section, the amplitude of both the resistive and inductive noise relative to the power supply voltage increases with technology scaling. A number of techniques have been proposed to mitigate the unfavorable scaling of power distribution noise. These techniques are briefly summarized below.

To maintain a constant supply voltage to resistive noise ratio, the effective sheet resistance of the global power distribution grid should be reduced. There are two ways to allocate additional metal resources to the power distribution grid. One option is to increase the number of metallization layers. This approach adversely affects fabrication time and yield and, therefore, increases the cost of manufacturing. The ITRS forecasts only a moderate increase in the number of interconnect levels, from eight levels at the 130-nm line half-pitch node to eleven levels at the 32-nm node [1]. The second option is to increase the fraction of metal area per metal level allocated to the power grid. This strategy decreases the amount of wiring resources available for global signal routing and therefore can also necessitate an increase in the number of interconnect layers.

The sheet inductance of the power distribution grid, similar to the sheet resistance, can be lowered by increasing the number of interconnect levels. Furthermore, wide metal trunks typically used for power distribution at the top levels can be replaced with narrow interdigitated power/ground lines. Although this configuration substantially lowers the grid inductance, it increases the grid resistance and, consequently, the resistive noise [20].

Alternatively, circuit techniques can be employed to limit the peak transient power current demands of the digital logic. Current steering logic, for example, produces a minimal variation in the current demand between the transient response and the steady state response. In synchronous circuits, the maximum transient currents typically occur during the beginning of a clock period. Immediately after the arrival of a clock signal at the latches, a signal begins to propagate through the blocks of sequential logic. Clock skew scheduling can be exploited to spread in time the periods of peak current demand [24].

The constant metal thickness scaling scenario achieves a lower overall power noise until the technology generation is reached where the inductive and resistive voltage drops become comparable. Beyond this node, a careful tradeoff between the resistance and inductance of the power grid is necessary to minimize the on-chip power supply noise. The increasing significance of the inductance of the power distribution interconnect is similar to that noted in signal interconnect [25], [26]. The trend is, however, delayed by several technology generations as compared to signal interconnect. As discussed in Section III, the high-frequency harmonics are filtered out by the on-chip decoupling capacitance and the power grid current has a comparatively lower frequency content as compared to the signal lines.

VII. Conclusions

An analysis of scaling power distribution noise in flip-chip packaged high-performance IC is presented in this paper. Published scaling analyses of power distribution noise are reviewed and various assumptions of these analyses are discussed. Under the constant metal thickness scenario, where the thickness of the global power lines remains constant, the resistive voltage drop across the power grids remains approximately constant, while the inductive drop increases by S. Consequently, the SNR de-

creases by S in the case of resistive noise and by S^2 in the case of inductive noise. Thus, the on-chip inductive noise increases faster and becomes more significant with technology scaling as compared to resistive noise. Under the scaled metal thickness scenario, the thickness of the global interconnect scales in proportion to the minimum feature size. Ideal interconnect scaling of the upper metal levels improves the inductive noise SNR_L by S and worsens the resistive SNR_R by S. Careful tradeoffs between the resistance and inductance of power distribution networks in nanometer technologies will be necessary to achieve minimum power supply noise levels.

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