Substrate Coupling in Digital Circuits in Mixed-Signal Smart-Power Systems

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***Abstract*—This paper describes theoretical and experimental data characterizing the sensitivity of nMOS and CMOS digital circuits to substrate coupling in mixed-signal, smart-power systems. The work presented here focuses on the noise effects created by high-power analog circuits and affecting sensitive digital circuits on the same integrated circuit. The sources and mechanism of the noise behavior of such digital circuits are identified and analyzed. The results are obtained primarily from a set of dedicated test circuits specifically designed, fabricated, and evaluated for this work. The conclusions drawn from the theoretical and experimental analyses are used to develop physical and circuit design techniques to mitigate the substrate noise problems. These results provide insight into the noise immunity of digital circuits with respect to substrate coupling.**

***Index Terms*—Noise, smart-power, substrate coupling.**

I. Introduction

SUBSTRATE noise can affect the proper operation of both analog and digital integrated circuits. Substrate noise in certain analog applications has received a great deal of attention during the past decade particularly because of the requirements for high-resolution analog and RF signal processing [1]–[6]. A variety of techniques to decrease the effects of noise these sensitive analog circuits—technological, physical, circuit, and others—have been proposed and studied. These techniques include choices for the manufacturing technology, the substrate thickness and doping concentrations, the physical separation between noise aggressors and victims, the placement of substrate contacts, guard rings, and wells, the use of a backplane substrate contacts/biasing, signals transition times, and routing of the power lines [1]–[6]. Additional aspects of the substrate noise mitigation problem are represented by models of the substrate and integrating these models into existing simulation tools and design methodologies [7]–[15].

The substrate noise immunity of digital circuits, however, has received far less attention. One particular reason is that because of the natural noise rejection capabilities—that is, the existence of an inherent noise margin—digital circuits tolerate a relatively higher amount of noise as compared to analog circuits. Furthermore, substrate noise adversely affects digital circuits only in a limited class of applications where sufficiently strong on-chip substrate noise levels are not unusual. *Smart-power* on-chip systems with high-power analog drivers represent one such application.

Regardless of the particular noise source—an analog or a digital circuit—substrate noise problems are typically mitigated by employing technological features providing a high degree of component isolation, or by avoiding the integration of digital and analog components on the same chip substrate (e.g., by using multichip modules). Both of these approaches, however, significantly increase the cost of the final product.

Furthermore, substrate noise problems are expected to deteriorate in future generations of deep submicrometer (DSM) systems requiring on-chip integration of complex digital and analog circuits. From the digital circuits perspective, the lower power supply voltage of these systems exacerbates the problems as the digital noise margins decrease [16]. In systems-on-a-chip (SoC), for example, complex digital processing and control circuitry are integrated on the same integrated circuit (IC) with sensitive analog processing blocks, RF circuits, and high-power circuitry. Since SoCs are typically implemented in a standard digital process—the reasons being enhanced process control and lower cost—reliable solutions are required to achieve minimal noise interaction amongst the various on-chip circuit components. Considering the stringent system performance requirements in ultra-scaled DSM systems [16], the noise immunity of digital circuits to substrate noise becomes increasingly important.

This paper focuses on the noise behavior of digital circuits in mixed-signal systems. The work presented here considers multiple issues related to substrate noise as follows:

1) determining the mechanisms of substrate noise transmission and behavior within digital circuits;
2) comparing the theoretical and experimental noise behavior of digital circuits;
3) providing circuit and physical design techniques to improve the noise reliability of both digital and analog components of a SoC.

The rest of this paper is organized as follows. The noise behavior of digital circuits is discussed in Section II. Test circuits and the experimental results from evaluating these circuits are presented in Section III. Substrate contact placement to minimize the adverse effects of substrate noise on both the analog and digital components of an SoC is discussed in Section IV,

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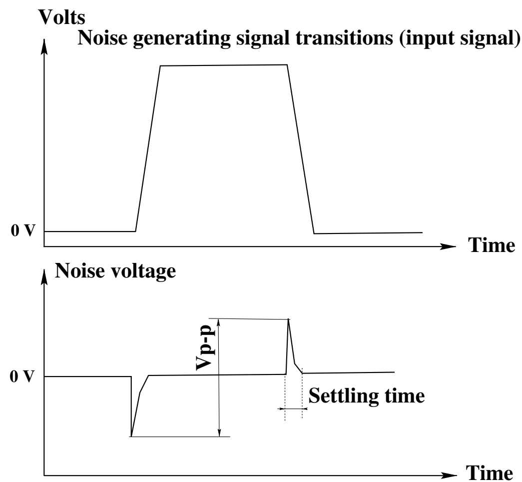

Fig. 1. A typical noise waveform caused by digital switching.

while alternative physical and circuit design solutions are summarized in Section V. Finally, some conclusions are offered in Section VI.

II. Noise Analysis of Digital Circuits

Consider a pair of typical substrate noise waveforms [1]–[5] as illustrated in Fig. 1, showing the noise inducing voltage (top) and a capacitively coupled noise waveform (bottom). Various physical processes must take place for this (or other) substrate noise to reach and affect a digital circuit in a mixed-signal system. A brief analysis of these processes is presented in this section where a digital circuit is considered to be affected by substrate noise if the output state of the digital circuit changes.

The effects of the noise spikes shown in Fig. 1 (bottom) on both an inverter and a simple latch [17] are analyzed in this section (both nMOS and CMOS circuits are analyzed). The analysis is performed by evaluating test circuits and observing the test circuit behavior under simulation using the Cadence–Spectre simulator [18]. The test circuits used in the simulations are shown in Fig. 2—note the nMOS and CMOS inverters in Fig. 2(a) and (c), respectively, the power driver in Fig. 2(b), and the nMOS and CMOS latches in Fig. 2(d) and (e), respectively. To gain insight into the test procedure, observe the typical test setup for the nMOS circuits shown in Fig. 3. In this experimental setup, the pulse voltage sources operating between $+5$ and -5 Volts are connected at nodes A, B, C, and D, respectively, in order to simulate various substrate noise conditions [19]. A similar setup is used for the CMOS circuits neglecting the CMOS parasitic latch-up structure [20].

In the case of the nMOS inverter shown in Fig. 2(a), conditions for inducing a parasitic inverter output transition are created when the inverter's input is *high* and the substrate voltage transient has a positive sign [19]. This parasitic output transition depends upon 1), the duration and magnitude of the noise pulse, 2), the relative transistor size, and 3), the capacitive load C_L of the inverter. For a typical situation with $C_L = 10$ fF and $k_E/k_D = 4$, the minimum substrate noise voltage amplitude required to induce a significant inverter output transition is approximately 1.7 V (note that k_E and k_D are the current gains of the transistor devices QE and QD, respectively).

Next, note that the two inverters shown in Fig. 3 constitute an nMOS static latch and consider an open-loop analysis of this latch under various operating conditions [19]. The primary objective of this analysis is to determine the conditions required for a logic state to be incorrectly transmitted to the output of the bistable element, hence, incorrectly latched under closed loop conditions. There are two important cases to be considered.

In the first case, illustrated in Fig. 4(a), the noise waveforms at inverter1 and inverter2 are *in phase*. In other words, all of the transistors in the inverters are affected by the substrate noise pulse at the same time. This type of noise is often referred to as *uniform* noise. In the second case, depicted in Fig. 4(b), the noise is *not* in phase, that is the transistors in the inverters are affected by the substrate noise pulses at different times.

For CMOS circuits, latch-up and metastability are shown to be the primary mechanisms affecting the integrity of a digital output. When similar to nMOS circuit simulation conditions are applied to the CMOS circuits, a parasitic transition is recorded for both high- and low-logic inputs and for substrate noise amplitudes greater than approximately $+3$ and -3 V, respectively. Note the symmetry of the CMOS behavior with regard to the input data and noise amplitude and phase (for equal transconductance of the *N* and *P* branches of the CMOS logic element), as well as the difference with the nMOS behavior. Note also the larger noise amplitude required for the CMOS circuits. If such large substrate noise levels are present, it is highly likely that latch-up will occur before a parasitic transition is induced.

The principal conclusion of the above analysis is that uniform substrate noise—that is, in phase—must be much larger in amplitude to induce a parasitic transition at the output of a latch as compared to nonuniform noise (not in phase). Other effects are with regard to the noise amplitude, data dependence, and the latch-up and metastability behavior. Among the phenomena and mechanisms responsible for this noise behavior in logic elements are 1) noise transmission through the substrate (amplitude and uniformity); 2) the substrate characteristics (epi versus non-epi, doping profiles, isolated tubs [20]; 3) body effect; 4) the operating point and region of operation of a transistor as well as the geometric dimensions and output load; 5) noise induced forward biasing effects [19]; 6) the logic family, and (7) the voltage transfer characteristics (VTC). Among the major causes responsible for inducing a nonuniform noise within the substrate are [19] 1) the parasitic *RC* elements within the substrate which introduce delays to the substrate noise transmission process; 2) the transmission characteristics of the noise in epi versus non-epi substrates; and (3) the placement of substrate contacts which can influence the noise transmission process by creating lines of nonequal noise. As demonstrated in Fig. 5(a), two transistors, *tx1* and *tx2*, despite being physically close, may belong to lines of different noise magnitude.

III. Experimental Results

A set of test circuits inspired by smart-power applications [17], [21] was developed to experimentally analyze the substrate noise behavior of sensitive digital circuits. In these test circuits, the substrate noise is generated by controlled switching of groups of eight individually selectable power drivers powered at 38 V. A power driver is shown in detail in Fig. 2(b).

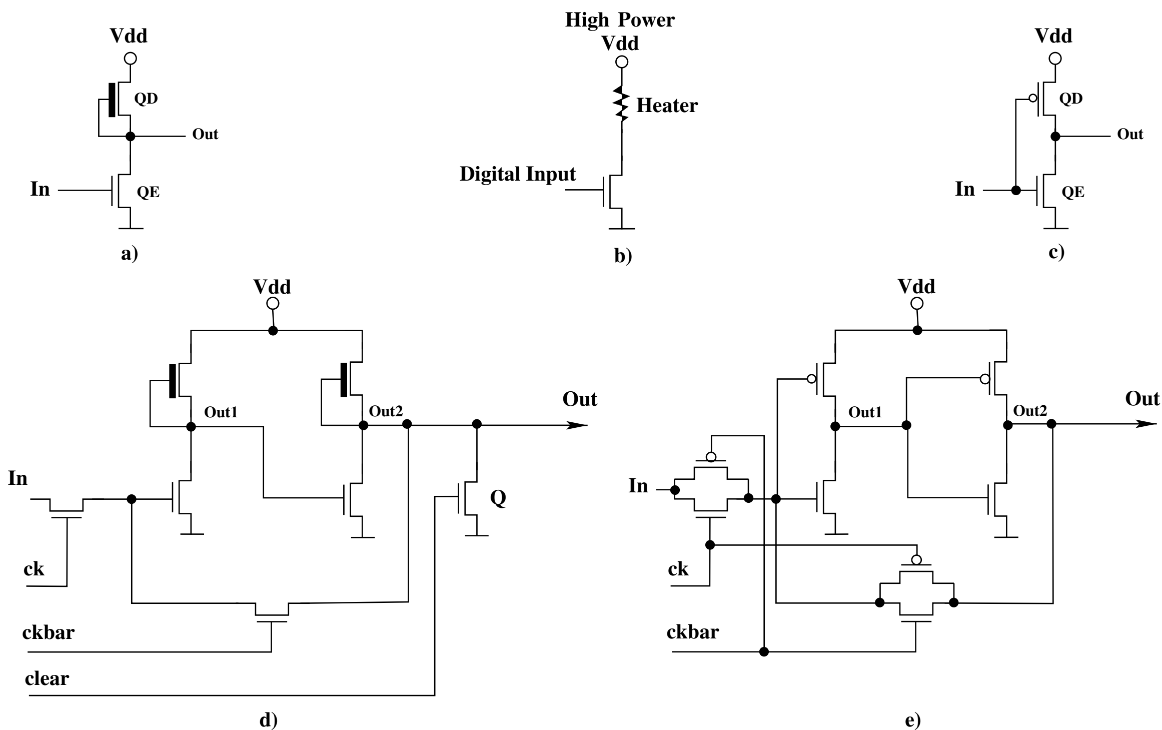

Fig. 2. nMOS and CMOS test circuits. (a) nMOS inverter. (b) nMOS and CMOS power driver. (c) CMOS inverter. (d) nMOS static slave latch. (e) CMOS static latch.

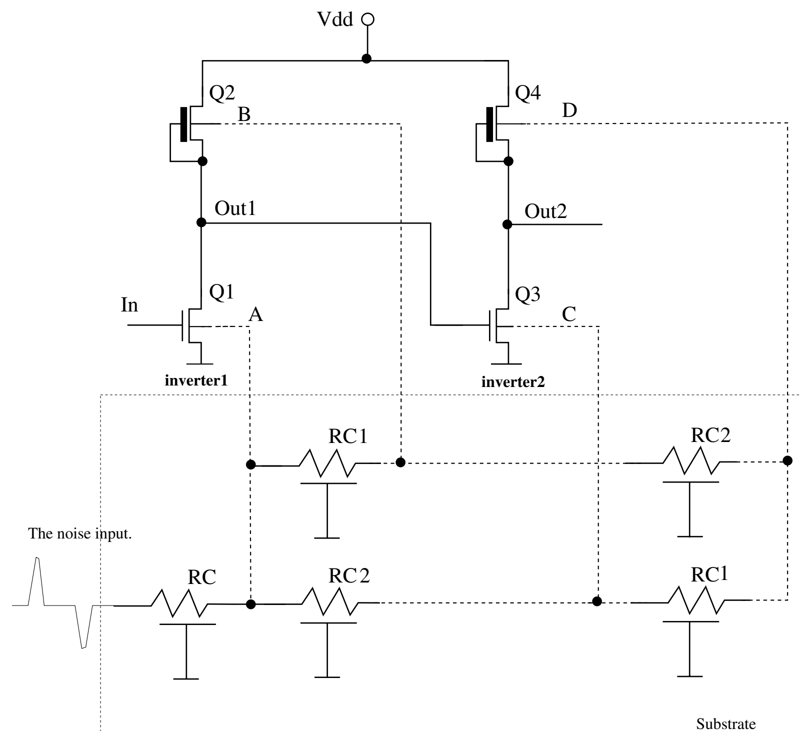

Fig. 3. Two nMOS inverters with substrate noise. The substrate is modeled as a distributed *RC* mesh.

Note that each power driver is driven by 13 V predrivers [17], [22] whereas the predrivers are controlled by standard 5 V logic. Approximately 50 test circuits, in both nMOS and CMOS processes, were designed, fabricated, and tested. These test circuits can be separated into two groups. Test circuits in the first group were used to monitor the effects of substrate noise on static and dynamic digital registers (memory elements). Representative microphotographs of nMOS and CMOS test circuits from this group are shown in Figs. 6 and 7, respectively. Note the substantially large groups of power drivers in both the nMOS and CMOS circuits photographs (Figs. 6 and 7, respectively). The general circuit floorplan (shown in Fig. 8), demonstrates

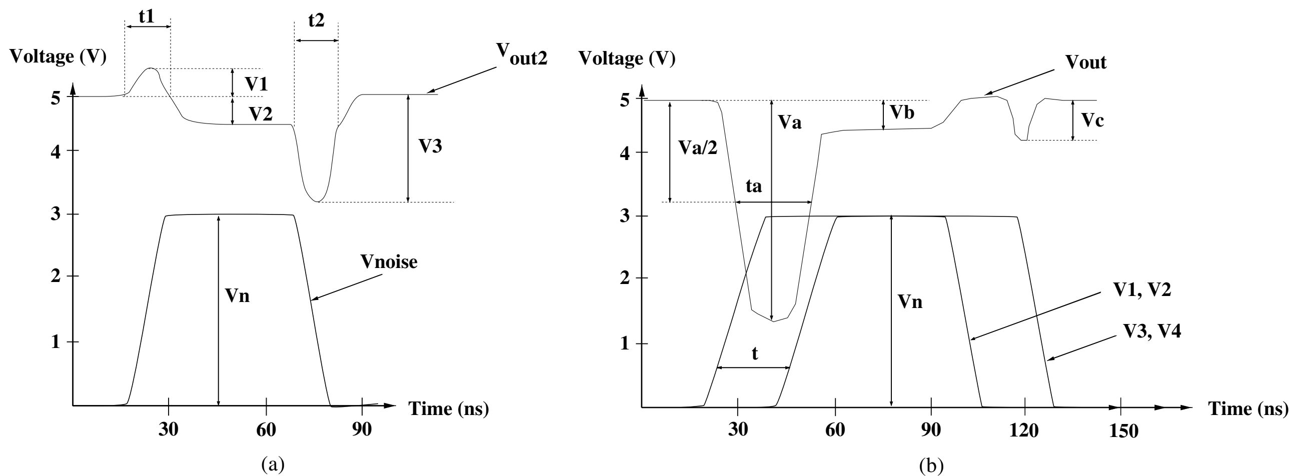

Fig. 4. The output waveforms for an open loop static latch when the substrate noise is (a) uniform and (b) nonuniform. (a) A typical waveform at Out2 when the noise voltages at A, B, C, and D for the circuit shown in Fig. 3 are in phase. (b) Typical waveform at Out2 when the noise voltages at A, B, C, and D for the circuit shown in Fig. 3 are not in phase.

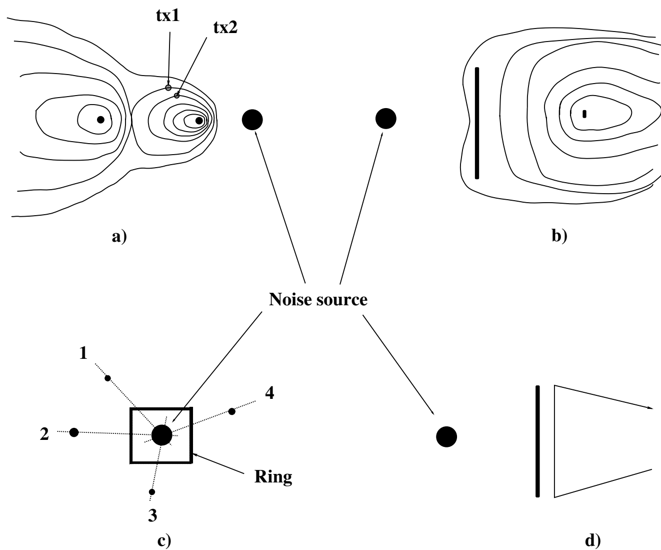

Fig. 5. Spatial noise distributions for small and large substrate contacts and rings. Lines of equal noise are illustrated.

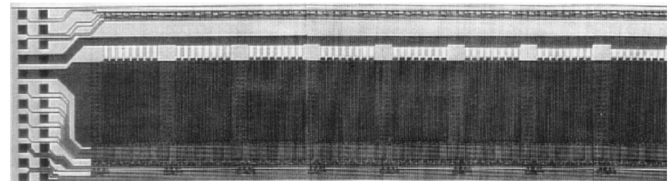

Fig. 6. Microphotograph of nMOS test circuit.

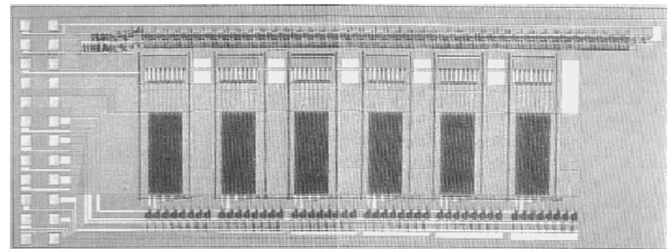

Fig. 7. Microphotograph of CMOS test circuit.

the relative position of the power drivers and the sensitive digital registers nearby (top) in further detail.

The purpose of the second group of test circuits was to provide a means to record the actual substrate noise waveforms generated within the substrate by the power driver [22]—a representative microphotograph of a test circuit from this group is shown in Fig. 9 [20], [23]. During testing, it was observed that the power transistors generate substrate noise not only during the on/off transition process, as described in [1]–[5] and illustrated in Fig. 1, but also while operating in the linear region [17], [22]. An oscillatory substrate noise waveform shown in Fig. 10 was observed during normal operation of the power driver [22]. The shape of this oscillatory waveform may be attributed to a substrate-predriver-driver positive-feedback loop [22]. This feedback loop makes the power driver transition from the linear region to the saturation region and from the saturation region to the linear region, thereby, generating noise fluctuations. The oscillatory substrate noise disturbs the normal operation of the digital circuits since each oscillation may generate further nonuniform noise distributions across the substrate. Note the difference between the experimentally derived oscillatory waveform shown in Fig. 10 and the near ideal noise waveform shown in Fig. 1 where the noise is induced only during signal transitions.

A number of test circuits were designed in order to simultaneously monitor the substrate noise waveforms and the effects of substrate noise on the static and dynamic registers. It was experimentally demonstrated that the number of static and dynamic registers affected by the substrate noise increases with 1) the existence of a nonuniform noise distribution; 2) the greater magnitude and nonuniformity of the noise; and 3) the greater oscillatory behavior of the substrate noise waveform [21], [22] as discussed in Section II.

Note that the noise immunity of both static and dynamic registers was observed to depend strongly on the logic state of the stored data and the register input signal conditioning. In the case of a logic low-input signal and nMOS circuits, for example, the

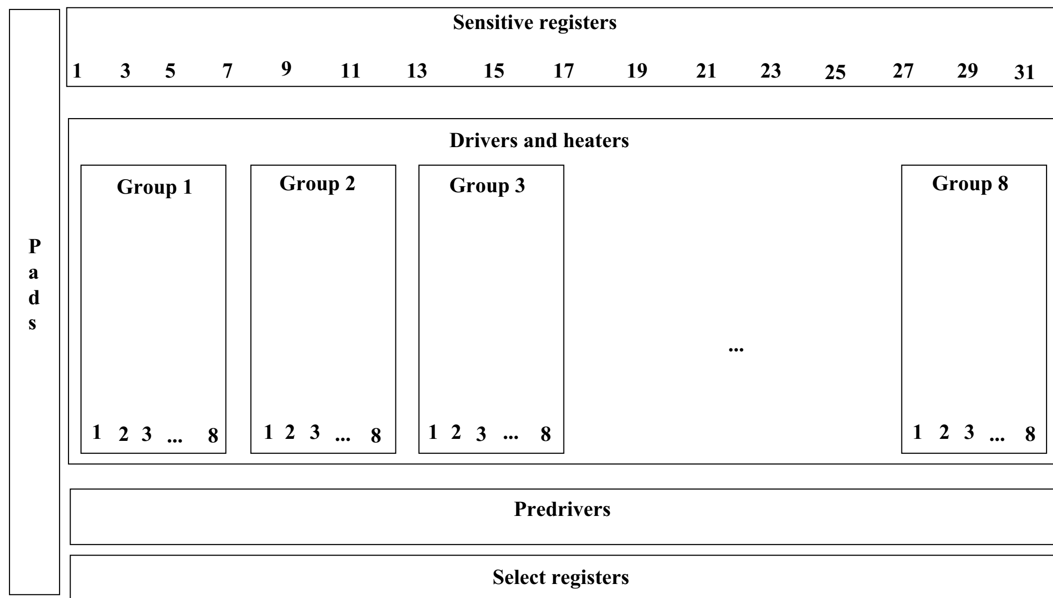

Fig. 8. Floorplan of both of the nMOS and CMOS test circuits.

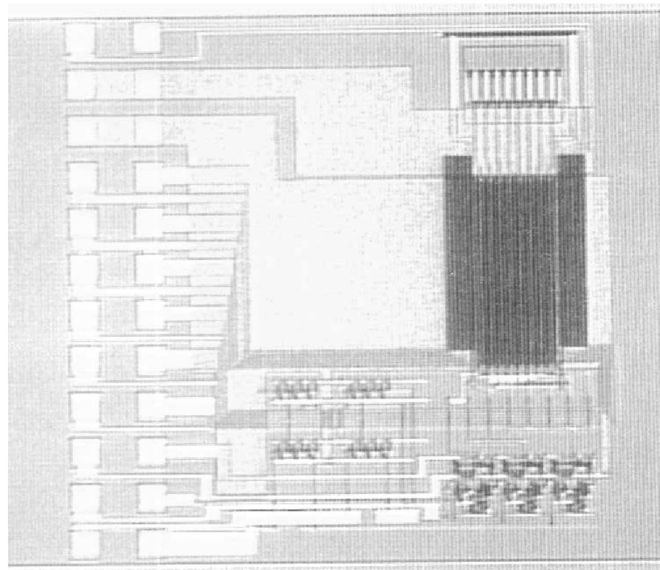

Fig. 9. Microphotograph of a test chip used to probe the substrate noise waveforms.

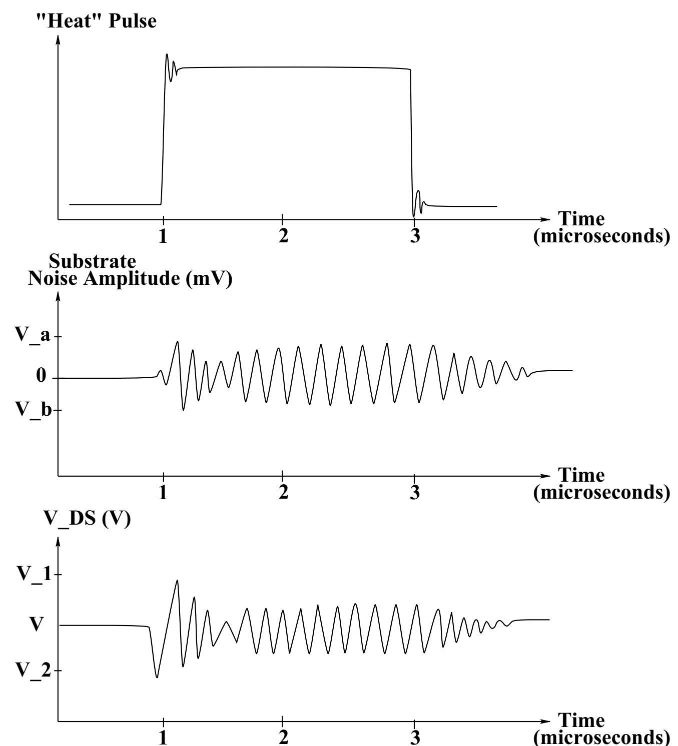

Fig. 10. Experimentally derived substrate bias oscillation in relation to the V_{DS} variations of the power driver transistor.

static registers are effectively immune to noise while the dynamic registers exhibit a higher sensitivity.

Eight clocking regimes were identified based on the state of the clock during the turn-on and turn-off transitions of the power drivers [21]. The behavior of the static and dynamic registers for the clocking regimes one through four, as shown in Fig. 11, is distinct. Clocking regimes five through eight can be reduced to cases one through four. The noise tolerance of the static and dynamic registers as a function of clocking regime, physical separation, driver power supply voltage, number of active drivers, and on-chip location (with respect to the power driver correlated to the clocking regime) are shown in Figs. 12– 16, respectively [21]. These results are discussed in greater detail in [24].

It was also observed that a larger number of registers are affected as the on-time of the power drivers increases [21], particularly when the power and digital grounds are connected off-chip [21]. It was noted that specific registers can be randomly affected from one noise pulse to another noise pulse without altering the test conditions [19]. The routing of the power distribution network is important in managing the noise immunity of the registers because of IR drops and $L(di/dt)$ effects [19], [21], and [22]. Proper substrate contact placement can be used to improve the noise behavior of the digital circuits [19], [21], [22], while improper substrate contact placement can significantly worsen this behavior [25].

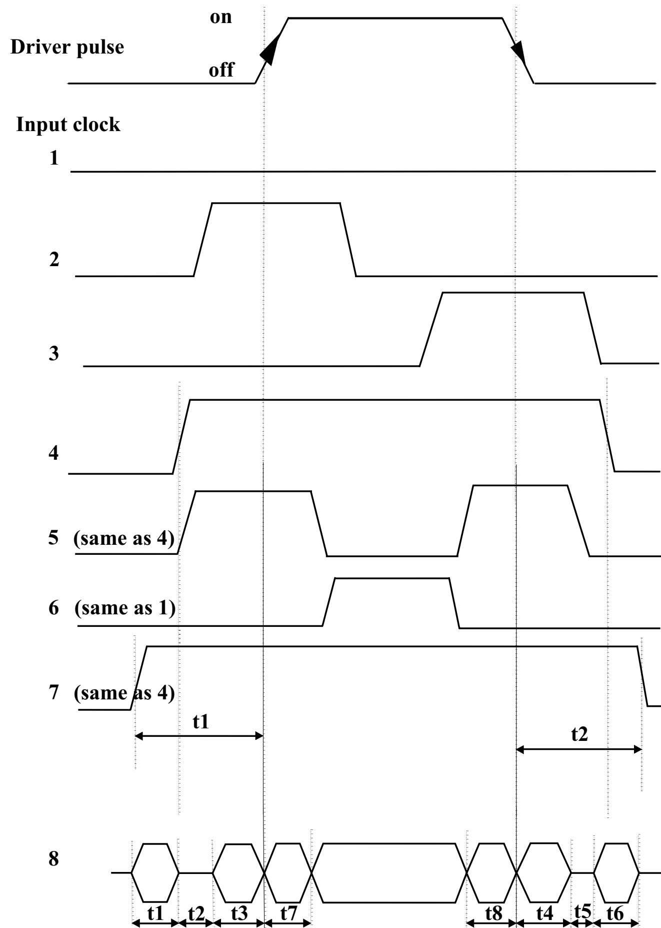

Fig. 11. Relationship between the external input clock signal (clock phases) and the driver on-time, generating different clocking regimes for the test circuits.

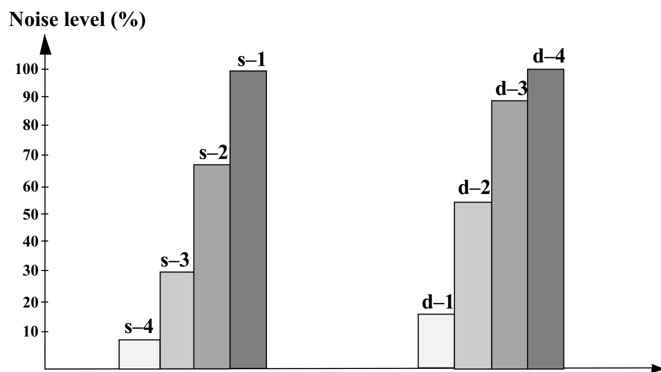

Fig. 12. The noise tolerance as a function of clocking regime for both static and dynamic registers. s = static, d = dynamic, and 1, 2, 3, 4 are according to Fig. 11. The 100% noise level influence is relative for static and dynamic registers. The number of affected dynamic registers is approximately 1.3 times larger than the static registers.

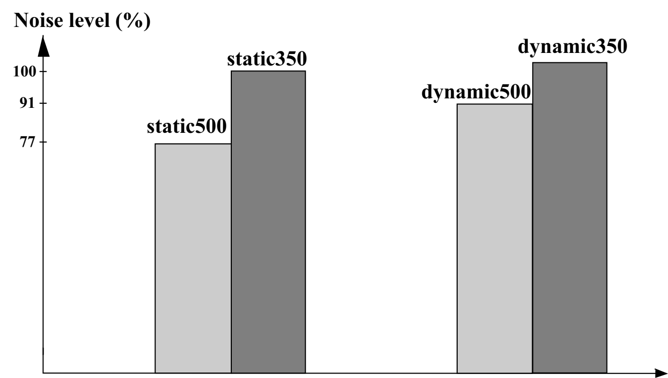

Fig. 13. Dependence of the received noise on the physical separation for both static and dynamic registers. Two distances, 350 μm and 500 μm, are shown. The 100% noise level is relative for static and dynamic registers, and the number of affected dynamic registers is approximately 1.15 times larger than the static registers.

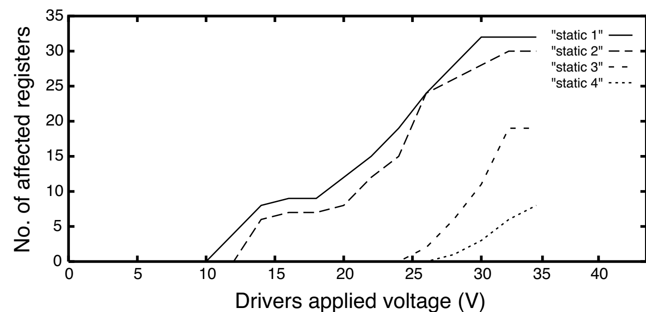

Fig. 14. Number of affected registers as a function of the driver power supply voltage for four clocking regimes (for static registers).

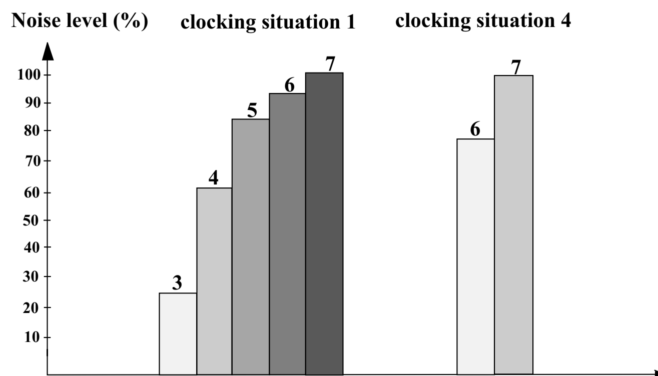

Fig. 15. The relationship between the active drivers (the numbers above each column) and the generated noise for the one and four clocking regimes and for the static registers. The 100% noise level is relative for clocking regimes one and four, and the number of affected registers is approximately 30 times smaller for clocking regime four as compared to clocking regime one.

The experimental data also confirm the theoretical results derived in Section II regarding the behavior of CMOS circuits with respect to substrate noise. Latch-up and metastability are the two primary phenomena by which the registers are affected [20]. An incorrect change of state at the output is marginally observed when the stored data is logic high [20]. This data confirms the behavior that latch-up and metastability occur well before the noise level surpasses the critical noise threshold (see Section II).

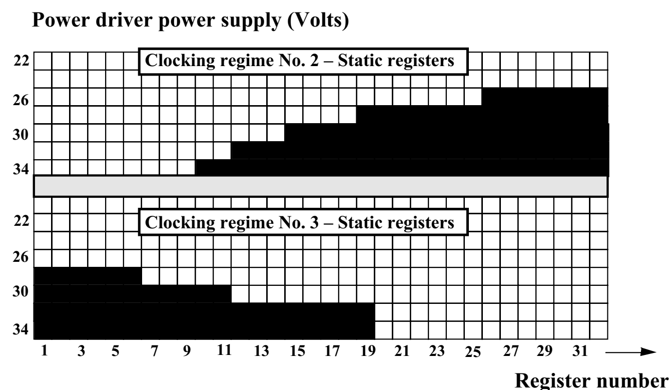

Fig. 16. Noise tolerance affecting register location as a function of the power driver voltage, substrate bias, clocking regime, ground bias, and active power driver group. Group 2 is active, and the black shaded area represents the affected registers.

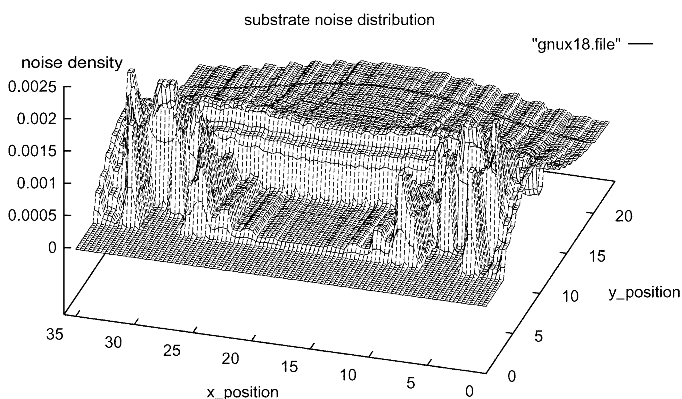

Fig. 17. Substrate noise distribution for an epi technology.

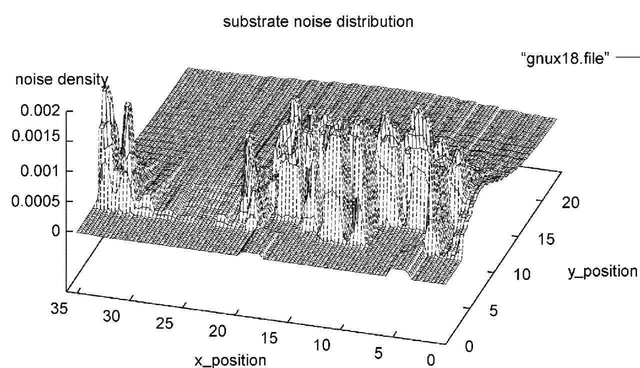

Fig. 18. Substrate noise distribution for a non-epi technology.

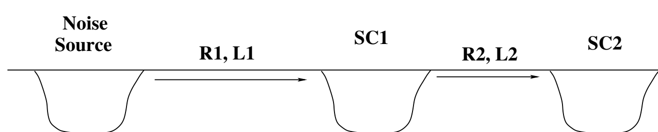

Fig. 19. Efficient placement of multiple substrate contacts in a non-epi technology.

IV. Placement of Substrate Contacts

The magnitude and nonuniformity of the substrate noise within the substrate, circuit and transistor size, data dependencies, the nature of the logic family, power supply voltages, the impedance characteristics of the power distribution network, the substrate parasitic impedances, the relative placement and partitioning of the circuit blocks, and the latch-up and metastability behavior are some of the primary factors discussed in Section III that significantly influence the noise behavior of digital circuits [19]–[23]. Note that all of these issues address improvements in the noise behavior of a mixed-signal system through circuit and physical design without requiring any process technology enhancements.

The goal of this section is to address substrate contact placement and related power distribution network issues in order to minimize the amplitude and decrease the nonuniformity of the substrate noise. The results of this section can be applied to both digital or analog/RF circuits in order to either minimize the generated noise or to reduce the effects of the noise being received.

To achieve these goals, a methodology has been developed to determine the appropriate placement of the substrate contacts [23]. Three-dimensional (3-D) substrate noise distributions are generated for various placements of substrate contacts relative to the noise source and noise receptor [23]. A custom *C* program is used to derive the noise distributions by processing the files generated by the Cadence-Spectre simulator [18]. A 3-D noise distribution of an epi technology is shown in Fig. 17, while a noise distribution of a non-epi technology is shown in Fig. 18. Note that for an epi technology, the noise travels predominantly along the interface between the epi layer and the bulk, while for a non-epi technology, the noise travels predominantly at the substrate surface. This important difference between the two technologies is primarily due to the low-resistivity bulk in an epi technology, and generates significant differences in the noise behavior of the two types of technologies. Major differences in design strategies for the two technologies exist for placing substrate contacts to reduce the noise magnitude and improve the noise uniformity.

As described in [23] and [25], in order to minimize substrate noise in a non-epi technology, two substrate contacts, SC1 and SC2, must satisfy the following rule: the associated resistances, $R1$ and $R2$ (related to the L1 and L2 distances), as shown in Fig. 19, must satisfy

$$\frac{R_1}{R_2} \ll 1. \tag{1}$$

To minimize the resistance $R1$, the contact SC1 must be placed as shown in Fig. 20, that is, as close as possible to the noisy drain. A wide substrate contact is also beneficial [23].

For an epi technology, two methods can be used [23] to reduce the noise level. The first method reduces the noise injected into the bulk by the noise source. Referring to Fig. 21, reducing the noise injected into the bulk is equivalent to placing a substrate contact between the noise source and the noise receptor (the substrate contact, GND) in order to maximize the noise that travels along the surface of the substrate.

A necessary condition to produce this behavior is (see Fig. 21)

$$kL_2 \ll 2kL_1 + L_2, \tag{2}$$

where L_1 is the thickness of the epi layer and $\rho_{epi}/\rho_{\text{bulk}} = k$ (the doping of the epi layer is k times larger than the doping

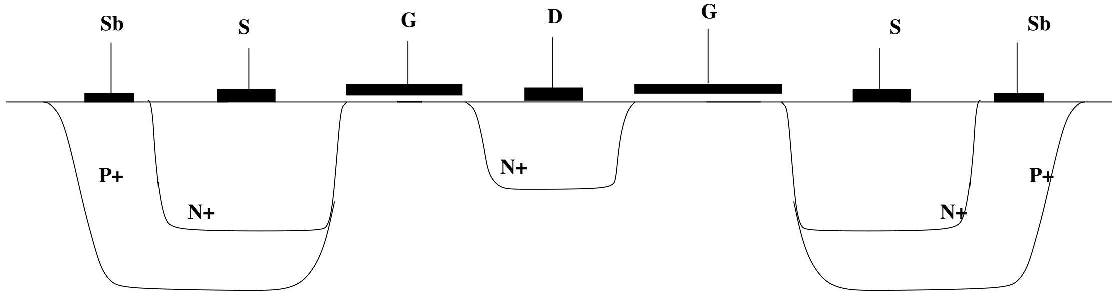

Fig. 20. Placement of a ring surrounding a noisy drain.

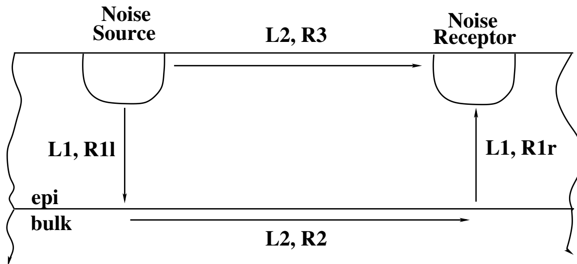

Fig. 21. Resistance distribution between the noise source and a substrate contact for an epi technology.

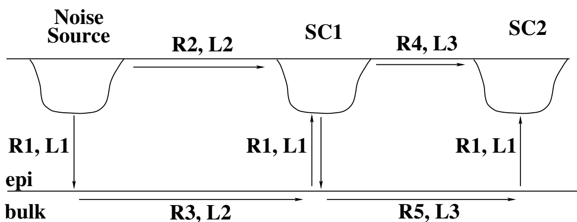

Fig. 22. Efficient multiple substrate contact placement in an epi technology.

of the bulk). Multiple substrate contacts that satisfy the above conditions are beneficial [23].

The noise level in an epi technology is reduced according to the second method by collecting a major portion of the noise from the bulk with two substrate contacts placed as shown in Fig. 22. The strategy is for SC1 to collect significantly more noise than SC2. Note that between the noise source and SC1, the noise may travel either primarily through the epi layer if (2) is satisfied, or mostly through the bulk. Defining R_m as the smallest resistance between the two resistances of the two noise paths, the condition for SC1 to remove a large noise from the bulk is

$$R_m \ll R_5 + R_1. \tag{3}$$

Note that in order to satisfy (3), L_3 must be significantly larger than either L_2, or $L_1 + L_2$. Due to the low resistivity of the bulk, L_3 must be greater than $\rho_{\text{epi}}/\rho_{\text{bulk}}$ times the equivalent distance through the epi layer [23]. A large L_3 translates into an inefficient use of on-chip area. However, this solution is viable for certain applications.

Due to the low-resistivity bulk, the noise uniformity is much greater in an epi technology as compared to a non-epi technology. However, to further improve the noise uniformity in an epi as well as in a non-epi technology, substrate contacts within each logic element (or gate) or small group of transistors is recommended [23]. Particularly for a non-epi technology, the noise uniformity is significantly enhanced if the transistors are placed in a quiet zone close to a large substrate contact on the opposite side of the noise source as shown in Fig. 5(d) [23].

Note the differences between the epi and non-epi technologies. An epi technology is similar to a non-epi technology from the perspective of the substrate noise, for certain doping and epi thickness conditions, as well as for relative device densities with respect to the epi thickness. With these conditions, improved tolerance to substrate noise may be achieved for an epi technology.

Trends for reducing substrate noise as a function of substrate contact placement for epi and non-epi technologies are summarized in Figs. 23 and 24. The noise at SC2 is a function of the ratio of the distance between the thickness of the epi layer L_{epi} and the distance between SC1 and SC2, $D_{\text{SC1}-\text{SC2}}$. Conditions for which curves 1–7, shown in Fig. 24, are based are listed in Table I.

Note that for a non-epi technology, the greatest decrease in noise occurs in region 2. For an epi technology, the most effective conditions for placing substrate contacts in order to reduce the noise is to increase the epi layer thickness, decrease $D_{\text{NS}-\text{SC1}}$, use a wider SC1 ring, and place the second SC2 ring or substrate contact at $L_{\text{epi}}/D_{\text{SC1}-\text{SC2}} \approx 1$. Note, that it is preferred to have $L_{\text{epi}}/D_{\text{SC1}-\text{SC2}} > 1$ rather than $L_{\text{epi}}/D_{\text{SC1}-\text{SC2}} < 1$. Also, note that as compared to a non-epi technology where the use of three rings reduces the noise, the use of multiple rings has no effect on the noise behavior of an epi technology due to the low resistivity bulk.

V. Noise Mitigation Techniques

A summary of the noise mitigation techniques verified through extensive experiments is provided in this section. By applying these techniques, some or all of the following results are achieved: 1) the magnitude and nonuniformity of the noise throughout the substrate are reduced; 2) the digital circuits tolerate higher noise magnitudes and/or nonuniformities; and 3) the noise level that the analog/RF circuits receive is substantially decreased, improving the noise behavior of these circuit blocks. The overall result is a capability for designing an SoC with improved noise immunity implemented in a low-cost technology. While some of the recommended techniques are particularly applicable to a smart–power environment, most of these techniques can be extended to any noisy circuit environment.

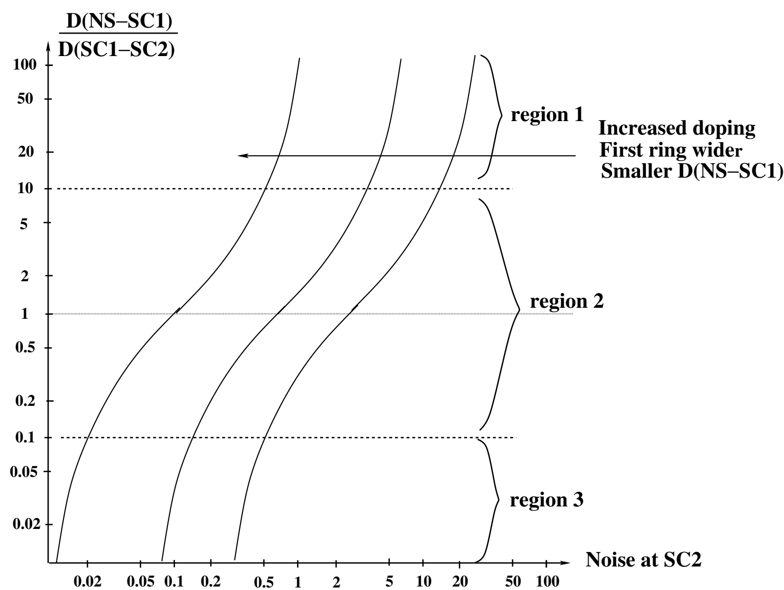

Fig. 23. Noise variation for non-epi technologies depending on the placement of the substrate contacts.

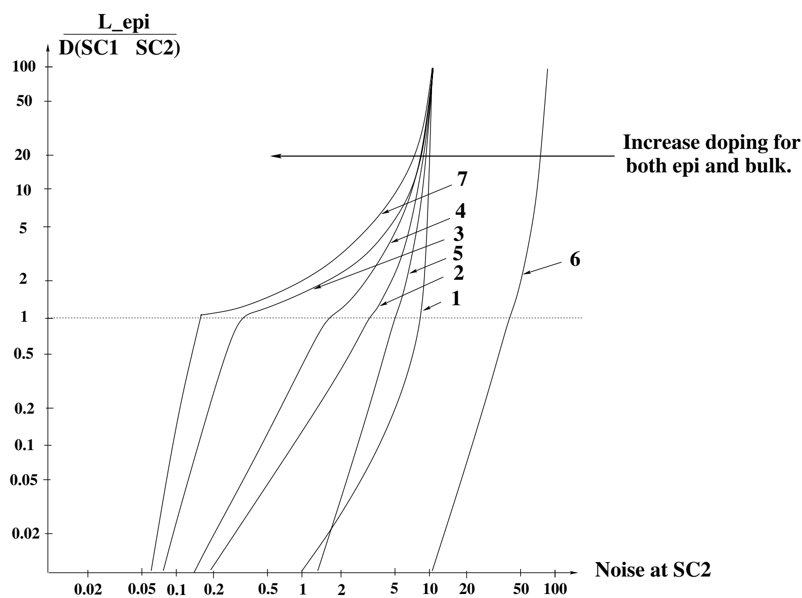

Fig. 24. Noise variation for epi technologies depending on placement of substrate contacts.

TABLE I
CONDITIONS FOR WHICH CURVES 1–7 SHOWN IN FIG. 24 ARE BASED

Curve	Conditions
1	$\rho_{epi}/\rho_{bulk} = 10$ and $D_{NS-SC1} \gg L_{epi}$
2	$\rho_{epi}/\rho_{bulk} = 10$ and $D_{NS-SC1} = L_{epi}$
3	$\rho_{epi}/\rho_{bulk} = 10$ and $D_{NS-SC1} = 0.1L_{epi}$
4	$\rho_{epi}/\rho_{bulk} = 3$ and $D_{NS-SC1} = L_{epi}$ when ρ_{epi} is constant
5	$\rho_{epi}/\rho_{bulk} = 100$ and $D_{NS-SC1} = L_{epi}$ when ρ_{epi} is constant
6	$\rho_{epi}/\rho_{bulk} = 100$ and $D_{NS-SC1} = L_{epi}$ when ρ_{bulk} is constant
7	$\rho_{epi}/\rho_{bulk} = 10$ and $D_{NS-SC1} = 0.1L_{epi}$ when SC1 is double in width as compared to SC1 in curve 3

A. Physical Design Techniques

An effective physical design technique is the use of substrate contacts as discussed in Section IV for epi and non-epi technologies. The theoretical discussion and experimental data permit the formulation of the following additional physical design techniques and observations:

- Special care in designing the power distribution network should be given to minimize IR and Ldi/dt induced voltage variations.
- The ground of the different circuit blocks, such as the drivers, predrivers, and logic blocks, should all be connected on-chip with minimal parasitic resistive paths among the ground lines. A low resistivity metal interconnect, therefore, is recommended, minimizing any parasitic effects which could generate an oscillatory substrate noise waveform.
- A compact layout is beneficial to improve the uniformity of the substrate noise received by the different transistors.

- If possible, it is preferable to place the noise sensitive digital circuitry as far and/or as symmetric as possible with respect to the noise source to improve the overall uniformity of the noise.
- Techniques that minimize the substrate noise induced latch-up and metastability should be a primary objective.

B. *Circuit Design Techniques*

- Static registers are preferable since the noise behavior of static registers is significantly more predictable than dynamic registers.
- The logic design must be optimized to favor those states which are less sensitive to substrate noise (see Section III).
- The choice of logic families is important in reducing the overall sensitivity of digital circuits to substrate noise.
- For the period of time during which the drivers are active (thereby, generating noise), special care must be taken to design the state of the clock used to synchronize the registers. As described previously, the preferred state of the clock is different depending upon whether the registers are static or dynamic. A preferable clock state during the noise generation process significantly reduces the noise sensitivity of the static and dynamic registers assuming the same level of noise within the substrate.
- The logic elements must be sized for symmetric low-to-high and high-to-low operations.
- The logic elements must be similarly loaded, preferably by a large-capacitive load. This technique can only be used in low-speed applications. If low-logic speeds are unacceptable, then the use of similar loads is preferable.
- It is also preferable to operate the power drivers at a lower voltage power supply. If a power resistor is required to dissipate a certain power (as in the present target application [17]), it is preferable to operate the power resistor at larger currents (with larger transistors) rather than at large voltages.
- The on/off process for the power drivers must be skewed in time as much as possible. This strategy decreases the noise amplitude within the substrate.

VI. Conclusions

The research results described in this paper is believed to be the first comprehensive report to experimentally study and verify substrate coupling in digital circuits. Several fundamental questions regarding the noise immunity of digital circuits are answered. The principal mechanisms responsible for reducing the noise immunity of digital circuits are described. A set of test circuits used to experimentally determine the principal characteristics of the noise behavior of digital circuits and to verify the theoretical models are presented. Substrate noise waveforms are also experimentally measured, and the characteristics are correlated to the number of affected registers under a variety of different test conditions.

An analysis of substrate contact placement and other noise mitigation techniques is also presented to achieve improved noise behavior of digital circuits. By applying the results presented in this paper, the magnitude and nonuniformity of the noise throughout the substrate can be reduced, permitting the on-chip digital circuits in a mixed-signal environment to withstand larger noise. This capability is expected to improve the process for integrating an SoC into a low-cost semiconductor technology. These results are also applicable to digital-only circuits since increasing substrate coupling effects is a clear trend in next generation deep submicrometer digital CMOS circuits.

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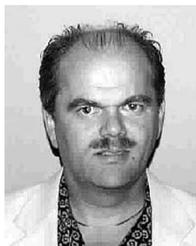

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Scott Warner, photograph and biography not available at the time of publication.

Scott Seabridge, photograph and biography not available at the time of publication.

Cathie Burke, photograph and biography not available at the time of publication.

Juan Becerra, photograph and biography not available at the time of publication.

Thomas E. Watrobski, photograph and biography not available at the time of publication.

Christopher Morton, photograph and biography not available at the time of publication.

William Staub, photograph and biography not available at the time of publication.

Thomas Tellier, photograph and biography not available at the time of publication.

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