Transactions Briefs

Exponentially Tapered H-Tree Clock Distribution Networks

Magdy A. El-Moursy and Eby G. Friedman

***Abstract*—Exponentially tapered interconnect can reduce the dynamic power dissipation of clock distribution networks. A criterion for sizing H-tree clock networks is proposed. The technique reduces the power dissipated for an example clock network by up to 15% while preserving the signal transition times and propagation delays. Furthermore, the inductive behavior of the interconnects is reduced, decreasing the inductive noise. Exponentially tapered interconnects decrease by approximately 35% the difference between the overshoots in the signal at the input of a tree. As compared to a uniform tree with the same area overhead, overshoots in the signal waveform at the source of the tree are reduced by 40%.**

***Index Terms*—Clock distribution network, H-trees, inductive noise, power dissipation, tapered interconnect.**

I. Introduction

With the decrease in feature size of CMOS integrated circuits (ICs), interconnect design has become a primary issue in high speed ICs. Interconnect design is most often used to increase circuit speed [1], however, the interconnect also affects the power dissipated by a circuit [2]. Clock networks can dissipate a large portion of the total power that is dissipated within a synchronous IC, ranging from 25% to as high as 70%. Some work has been published that considers power dissipation in the interconnect design process [3], [4]. Interconnect shaping has been previously introduced as an efficient technique to improve circuit performance [1]. In this paper, interconnect shaping is proposed as a technique to reduce the power dissipated by a clock distribution network as well as the inductive noise.

H-tree clock distribution networks are widely used [5]. The linewidths within a standard H-tree are typically divided by two at the branch points to reduce reflections [6], [7]. The proposed criterion does not maintain a tapering factor of two in sizing the interconnects in H-trees. Rather, exponentially tapered interconnects, as shown in Fig. 1, are proposed.

With increasing signal frequencies and a corresponding decrease in signal transition times, the interconnect impedance can behave inductively [8]. A variety of shielding techniques have been proposed to reduce the inductive behavior of the interconnects within a clock distribution network [9], [10]. Shielding clock lines with adjacent ground lines is a widely used technique [9]. The proposed design methodology not only decreases the transient power dissipation but also reduces the inductive noise of the interconnects. Fewer reflections occur at the branch points, improving the signal integrity.

The paper is organized as follows. In Section II, a criterion for tapering an H-tree network is presented. Different issues that affect the proposed technique are discussed in Section III. In Section IV, simulation results are presented. Some conclusions are provided in Section V.

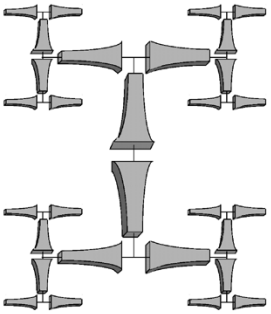

Fig. 1. Exponentially tapered H-tree interconnect structure.

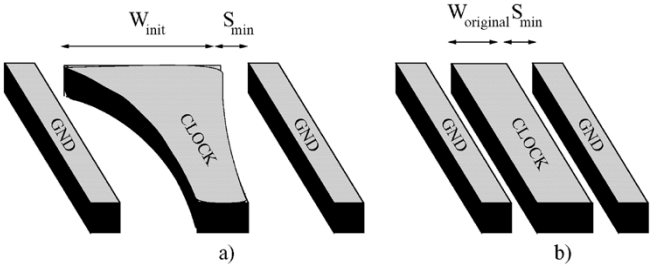

Fig. 2. Coplanar clock line. (a) Exponential tapering. (b) Uniform (no tapering).

II. Tapering an H-Tree for Low Power

Exponential tapering has been shown to be the optimum shape function to produce the minimum signal propagation delay in *RLC* lines [2]. A tapered line, shown in Fig. 2(a), can achieve the same signal characteristics (signal delay and transition time) as the uniform line shown in Fig. 2(b) with a smaller total line capacitance. Tapering a line reduces the coupling capacitance between the signal line and the adjacent ground lines, and, consequently, the total capacitance of the signal line. Although the line capacitance is reduced, the line resistance is greater, thereby maintaining approximately the same signal characteristics. A reduction in the line capacitance decreases the dynamic power while an increase in the line resistance decreases the inductive behavior of the interconnect. In Section II-A, a criterion is presented for tapering the interconnects of an H-tree clock distribution network based on a first-order moment approximation of the transfer function characterizing the clock tree. A second moment approximation is used in Section II-B to taper the interconnects of a clock distribution network while considering the interconnect inductance.

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A. Tapering Using First-Order Moment Approximation

An exponentially tapered *RLC* interconnect line is described in [2]. Due to practical limitations, the line is divided into equal length sections. A first order approximation of the transfer function of each line section is used to characterize the signal. As described in Section III, the line becomes less inductive with tapering, since the line resistance increases. A first-order approximation is adequate to characterize the time constant of each line section at relatively low frequencies. Additional savings in power can be achieved if a higher order approximation is used as described in Section II-B. If the *RC* time constants are maintained the same in both techniques (exponential and uniform), the signal characteristics (propagation delay and transition time) remain the same. The summation of the *RC* time constants of an exponentially tapered line along each branch of an H-tree is maintained equal to or less than the summation of the *RC* time constants of a uniformly sized line. The optimum tapering structure for minimum power satisfies

$$\sum_{i=1}^{N} R_{i-T} C_{i-T} \leq \sum_{i=1}^{N} R_{i-U} C_{i-U} \tag{1}$$

and, consequently, achieves the minimum line capacitance, where R_{i-T} and R_{i-U} are the resistance of each section in a tapered and uniform line, respectively, C_{i-T} and C_{i-U} are the capacitance of each section in a tapered and uniform line, respectively, and N is the number of sections in each branch.

Two design parameters are used to size the interconnect within the tree; the initial width W_{init} and the tapering factor p. A practical implementation for exponential tapering is considered in [11]. For the technology dependent precision of the wire width ΔW, different values of W_{init} and p can satisfy (1). Two practical constraints limit the choice of the initial linewidth W_{init} and the optimum tapering factor p for each branch level. These practical limits can be represented by the following.

1) $W_{\text{init}} \leq W_{\max}$, where $W_{\max}$ is the maximum wire width of a target technology.
2) $p \leq \frac{N}{l(N-1)} ln((W_{\text{init}})/(W_{\min}))$, where $W_{\min}$ is the minimum wire width of a target technology and l is the length of the line segment.

W_{init} cannot be greater than the maximum wire width permitted by the technology. Alternatively, increasing p may result in the width of the far end of a line being smaller than the minimum available wire width. W_{init} and p are chosen to satisfy (1) and any practical constraints while simultaneously minimizing the total line capacitance. A C program is used to determine the optimum tapering structure. In Section II-B, the line inductance is considered in the optimization process.

B. Tapering Using Second-Order Moment Approximation

In Section II-A, a first-order approximation, the *RC* time constant, is used to determine the optimum tapering structure (initial width W_{init} and tapering factor p) for each segment of an H-tree. Interconnect lines within H-tree clock distribution networks are often wide and long, exhibiting considerable line inductance, particularly at high frequencies. The optimum tapering structure can therefore be more accurately determined if line inductance is considered.

An approximation of the second moment of the transfer function of a signal propagating through an *RLC* line is used in [12] to estimate the delay of an *RLC* tree. The approximation of the second moment m_2 of an *RLC* line [12] is equivalent to the approximation of the first moment m_1, the *RC* time constant, of an *RC* line. The approximate second moment of the transfer function is used to maintain the signal characteristics of a tapered line. The line is divided into a number of sections as described in [2]. The second moment of the transfer function at the end of a line section is

$$m_2{}^i = \left(\sum_k C_k R_{ik}\right)^2 - \sum_k C_k L_{ik} \tag{2}$$

where C_k is the capacitance of each line section, R_{ik} is the summation of the resistance of all of the line sections from the begining of the line to the target section, and L_{ik} is the summation of the inductance of all of the line sections from the begining of the line to the target section.

Equivalent to the Elmore delay, the second moment m_{2-U-L_n} is determined at the end of the line segment. For a uniform line segment in branch level L_n, the second moment is

$$m_{2-U-L_n} = \sum_{i=1}^{N_{L_n}} \left[\left(R_{i-U-L_n} \left(\sum_{k=1}^{i} C_{k-U-L_n} + C_{L-L_n} \right) \right)^2 - L_{i-U-L_n} \left(\sum_{k=1}^{i} C_{k-U-L_n} + C_{L-L_n} \right) \right] \tag{3}$$

where N_{L_n} and C_{L-L_n} are the number of sections and the load capacitance of line segment L_n, C_{k-U-L_n} is the capacitance of section k of a uniform line segment, and R_{i-U-L_n} and L_{i-U-L_n} are the resistance and inductance of section i of a uniform line segment, respectively. The second moment approximation of a tapered line is

$$m_{2-T-L_n} = \sum_{i=1}^{N_{L_n}} \left[\left(R_{i-T-L_n} \left(\sum_{k=1}^{i} C_{k-T-L_n} + C_{L-L_n} \right) \right)^2 - L_{i-T-L_n} \left(\sum_{k=1}^{i} C_{k-T-L_n} + C_{L-L_n} \right) \right] \tag{4}$$

where C_{k-T-L_n} is the capacitance of section k of a tapered line segment and R_{i-T-L_n} and L_{i-T-L_n} are the resistance and inductance of section i of a tapered line segment, respectively. The second moment for all possible tapering structures (all possible initial widths W_{init} and tapering factor p as described in [2]) is compared with the moments of a uniform line. The optimum tapering structure is that structure which satisfies (5) and has the minimum total line capacitance,

$$m_{2-T-L_n} \leq m_{2-U-L_n}. \tag{5}$$

In order to simplify the process of determining the optimum tapering structure, a hierarchical technique is applied. The optimum tapering structure of each branch level of a tree is determined separately. Given the load capacitance at the leaf of an H-tree, the optimum tapering structure for the last segment (at the last branch level L_M or the leaf of the tree) is determined, where M is the number of branch levels. The total capacitance for that segment is used to determine the optimum structure for the higher branch level L_{M-1}. This process is repeated until the optimum tapering structure for the first level (the root of the tree) is obtained.

Practical constraints on the maximum and minimum line width, which are presented in Section II-A, are used to determine the optimum structure based on the second moment approximation. Additional considerations in the design of a tapered clock tree are discussed in Section III.

III. Design Issues in Exponentially Tapered H-Trees

Different issues that affect the design of an H-tree structured clock network are discussed in this section. In Section III-A, the effects of tapering on the signal characteristics of an H-tree are described. The overhead area of the interconnect network of an exponentially tapered

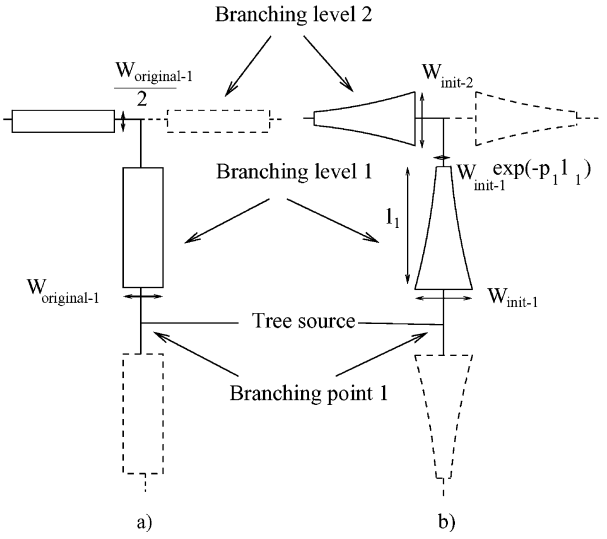

Fig. 3. Interconnect in an H-tree. (a) Uniform tapering. (b) Exponential tapering.

tree is discussed in Section III-B. The proposed structure is also compared in this section with a uniform structure with the same area overhead. In [11], skew reduction in an exponentially tapered H-tree network is discussed.

A. Signal Integrity

The linewidth of an interconnect within an H-tree is typically divided by two in a uniformly tapered tree to match the line impedance at the branch points, as shown in Fig. 3(a). In a uniformly tapered tree, the interconnect inductance often cannot be ignored, particularly at the source of the tree where the line is widest. Matching the impedance reduces reflections and improves signal integrity decreasing the inductive noise. This characteristic is not maintained in exponential tapering.

The branches of a tree are numbered according to the number of branch points (see Fig. 3). As shown in Fig. 3(b), the initial width of the interconnect at each branch level $W_{\text{init}-L_n}$ is chosen based on the constraints described in Section II. The tapering factor of each branch level p_{L_n} is determined by satisfying (1) for the first-order approximation and (5) for the second-order approximation. All of the interconnects in the tree belonging to the same branch level have the same p_{L_n} and $W_{\text{init}-L_n}$.

With the criterion proposed in this paper, the impedance mismatch does not affect the signal integrity of the lines since the interconnect resistance is greater. If a simple *RC* line model is considered, in order to reduce the line capacitance (to reduce the dynamic power) while the *RC* time constant is maintained the same, the line resistance is increased, reducing the effect of the inductance of the interconnect on the signal waveform. Furthermore, this technique reduces the reflections at the branch point, decreasing the inductive noise. Moreover, exponential tapering decreases the inductive noise, since the impedance mismatch is distributed along the line and not concentrated at the branch points. A reduction in resistance at the source of the line compensates the signal degradation that occurs due to the increase in the line resistance at the far end of the line.

The inductive behavior of the line can be characterized by the line damping factor $\zeta = (R_{\text{line}})/(2)\sqrt{(C_{\text{line}})/(L_{\text{line}})}$ [8], where $R_{\text{line}}, C_{\text{line}}$, and L_{line} are, respectively, the line resistance, capacitance, and inductance. The inductive behavior decreases as the damping factor increases, reducing the importance of matching the line impedance at the branch points. The difference between the first overshoot and undershoot $\Delta V_{\text{over}-\text{under}}$ at the driving point of the tree is treated as a metric characterizing the reflections in the tree. The area overhead of the proposed technique is discussed in Section III-B.

B. Routing Area

In the proposed H-tree structure, the interconnects comprising the clock network are assumed to be shielded by two ground lines. Coplanar shielded structures are commonly used in industry, particularly in clock networks, to reduce the interconnect coupling to adjacent lines and to minimize the delay uncertainty of the clock signal [6], [9], [10]. In the proposed structure, the interconnect width at the near end is larger, reducing the space between the signal (or clock) line and the ground shield. The space is assumed to be minimum in the uniform structure shown in Fig. 2(b). In order to maintain the distance between the signal and ground shield, the distance between the ground lines $S_{\text{large}} = (W_{\text{init}} - W_{\text{original}})/(2) + S_{\min}$ is increased by the same amount as the increase in the initial width W_{init}. For wider spacing between the signal and ground shield, the interconnect area is greater.

For the same area overhead, the line capacitance is reduced by increasing the space between the shield lines without changing the signal (or clock) line width. The capacitance (and, therefore, the dynamic power dissipation) of a line structure with wider spacing and uniform interconnect width is greater than the capacitance of an exponentially tapered structure.

Increasing the distance between the ground shield and the signal lines, produces a smaller reduction in the line capacitance (and dynamic power) as compared to exponentially tapering the lines. Furthermore, a wider space between the ground lines increases the inductance of the line since the area of the current return path is larger. Furthermore, an increase in the space without a change in the interconnect width maintains the same resistance as a uniform structure. An increase in the line inductance (without an increase in the resistance) increases the inductive behavior of the line. In Section IV, a comparison is presented between the proposed tapered structure and two alternative nontapered structures.

IV. Simulation Results

Different industrial H-tree structured clock distribution networks have been investigated to evaluate the proposed design technique. The optimum width $W_{\text{init}-L_n}$ and tapering factor p_{L_n} for each branch level L_n within each tree are determined. There are six branch levels $(M = 6)$ in this clock tree example. Closed-form expressions for the line impedance parameters (resistance, capacitance, and inductance) are used to model the tree interconnect [2]. Each interconnect branch is divided into a number of sections with length $l_1 = 125$ μm. l_1 is chosen to be greater than $l_{\min}$, the shortest line in the tree. Two ground lines, with a 1-μm width, shield the tree interconnects. The minimum distance between the clock line and the ground shield $S_{\min}$ is 1 μm. Copper interconnect and low-κ dielectric materials are assumed in order to evaluate the inductive properties of the lines.

A 64-sink clock tree covering a die area of 4.25×4.25 mm^2 is modeled as a distributed *RLC* network to observe the signal characteristics. A symmetric capacitive load is assumed at all of the sinks (no clock skew among the sinks).

Different techniques are used to size the interconnect within the tree as listed in Table II. The interconnect branch level is listed in the first column. The width of the uniform wires that achieves the minimum signal transition time at the loads of the tree is listed in the second column. In the third and fourth columns, the optimum initial width and tapering factor, respectively, of each branch level are listed for an exponentially tapered interconnect based on a first-order approximation.

TABLE I
SIGNAL CHARACTERISTICS AND POWER DISSIPATION OF DIFFERENT H-TREE CLOCK DISTRIBUTION STRUCTURES

Technique	t_r (psec)	t_{pd} (psec)	P_{total} (mW)	Reduction	$\Delta V_{over-under}$ (mV)	Reduction
Uniform tapering	149	227	5.18	—	683	—
Exponential using first order approximation	141	215	4.56	12%	675	1%
Uniform (larger spacing)	143	208	5.00	3.5%	836	-23%

TABLE II
H-TREE DESIGN TECHNIQUES USING FIRST AND SECOND MOMENT APPROXIMATION

Interconnect	Uniform tapering	Exponential tapering using first order			Uniform with larger spacing		Exponential tapering using second order			Uniform with larger spacing	
Branch Level	$W_{original}$ (μm)	W_{init} (μm)	p (mm^{-1})	$\zeta/\zeta_{original}$	S_{large} (μm)	$\zeta/\zeta_{original}$	W_{init} (μm)	p (mm^{-1})	$\zeta/\zeta_{original}$	S_{large} (μm)	$\zeta/\zeta_{original}$
1	10.0	14.7	1.8	1.30	3.4	0.83	11.6	2.2	1.85	1.80	0.91
2	5.0	8.3	1.8	1.18	2.6	0.80	8.0	2.3	1.07	2.50	0.82
3	2.5	4.3	3.7	1.14	2.0	0.83	3.8	4.6	1.56	1.65	0.87
4	1.3	2.6	4.0	1.11	1.7	0.84	2.1	3.5	1.20	1.40	0.89
5	0.6	0.7	2.5	1.01	1.0	0.98	0.73	2.7	1.02	1.05	0.98
6	0.5	0.5	0.0	1.00	1.0	1.00	0.5	0.0	1.00	1.0	1.00

TABLE III
SIGNAL CHARACTERISTICS AND POWER DISSIPATION OF DIFFERENT H-TREE CLOCK DISTRIBUTION STRUCTURES

Technique	t_r (psec)	t_{pd} (psec)	P_{total} (mW)	Reduction	$\Delta V_{over-under}$ (mV)	Reduction
Uniform tapering	142	236	6.09	—	784	—
Exponential using first order approximation	142	232	5.38	12%	765	2%
Exponential using second order approximation	147	235	5.18	15%	511	35%
Uniform (larger spacing)	139	228	5.60	8%	854	-10%

The ratio between the damping factor of each line segment for a tapered line and a uniform line is listed in the fifth column. The damping factor increases as compared to a uniform line, reducing the inductive effects in the signal waveform. A uniform line width (listed in the second column) with a larger spacing (listed in the sixth column) is also listed in the table as a design choice. Unlike a tapered line, the damping factor decreases if a larger spacing is used, increasing the inductive behavior (which produces ringing effects) in the signal waveform.

A 0.24-μm CMOS inverter is used to drive the tree in the example circuit characterized by Table II. An input ramp signal with a 50-ps transition time is applied at the input of the driver of the tree. The lines at the source of the tree are wide (highly inductive), making these lines the most inductive among all of the interconnect within the tree. The greatest amount of reflections occurs at the source of the tree. The attenuation of the signal along the interconnect tree degrades the overshoots at the load end. The difference between the first overshoot and undershoot is therefore observed at the source of the tree. The difference between the first overshoot and undershoot $\Delta V_{\mathrm{over-under}}$ decreases from 683 to 675 mV at the first branching point of a tapered structure. Alternatively, the difference increases to 836 mV when a larger spacing is assumed without shaping the lines. Tapering the interconnects achieves a reduction in $\Delta V_{\mathrm{over-under}}$ of approximately 20% as compared to a uniform design with the same area overhead.

In Table I, the signal characteristics (the propagation delay and transition time) and the transient power dissipated by a tree are listed for three interconnect structures. Exponential tapering and uniform tapering with a larger spacing maintain the same signal characteristics while dissipating less power. Exponential tapering, however, further reduces the power. A reduction in power dissipation of about 12% is achieved as compared to about 3.5% with no tapering.

The signal transition time at the input of the H-tree is reduced to 10 ps. For such a fast transition time, a second-order approximation is more effective as a criterion for tapering the lines within the tree. The interconnect width for an exponentially tapered line based on a second moment approximation is listed in Table II. A greater reduction in the damping factor is achieved using a second moment approximation, reducing reflections in the tree.

The signal characteristics are listed in Table III. The second moment approximation achieves a greater power reduction of 15% as compared to the first-order approximation.

The signal waveform at three points; the input of the driver, the first branching point, and the sinks (or loads) is shown in Fig. 4. $\Delta V_{\mathrm{over-under}}$ decreases from 784 to 511 mV at the first branching point of a tapered structure. The difference increases to 854 mV when a larger spacing is assumed without shaping the lines. Tapering the interconnects achieves a reduction in $\Delta V_{\mathrm{over-under}}$ of approximately 35%, thereby improving the signal integrity. Alternatively, increasing the spacing increases $\Delta V_{\mathrm{over-under}}$ by 10%, degrading the signal integrity. As compared to a uniform tree with the same area overhead, the difference between the overshoots is reduced by 40% in a tapered line.

The aspect ratio (the ratio between the line thickness to the line width) increases as technology advances, reducing the propagation

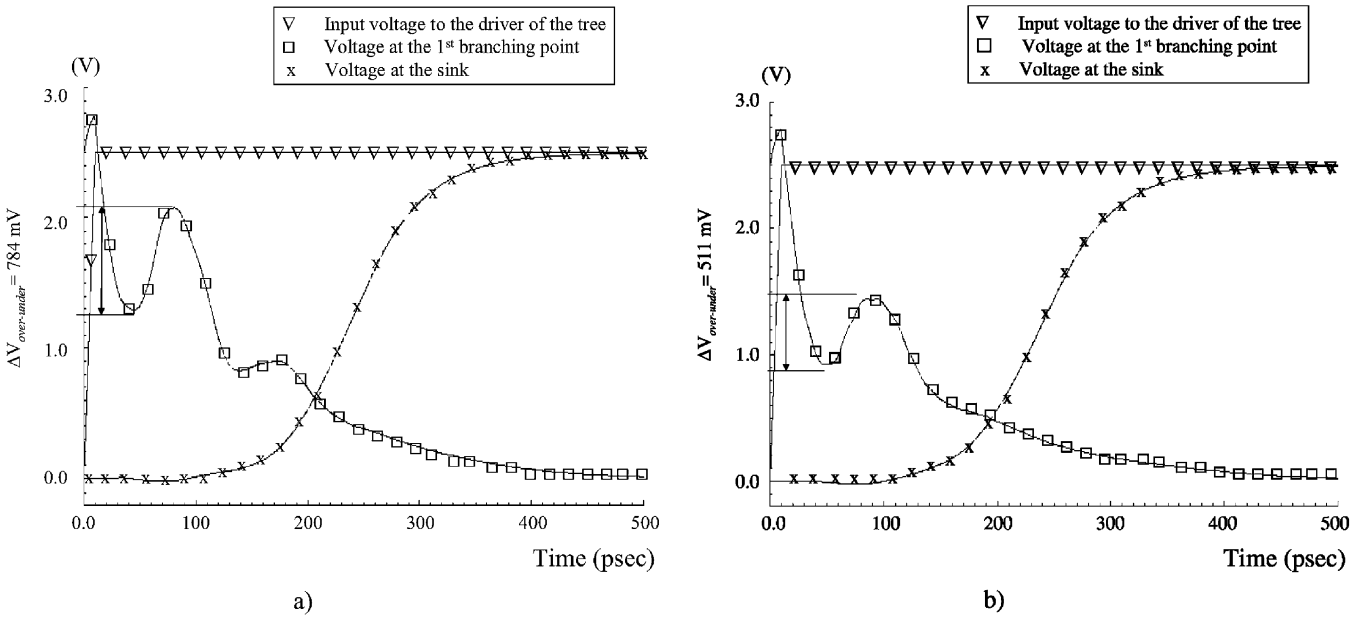

Fig. 4. Waveforms at different nodes within the tree. (a) Uniform tapering and (b) exponential tapering using second-order approximation.

delay. Exponential tapering, based on a second-order approximation, is compared with uniform tapering for an interconnect thickness of 0.1 μm. A smaller reduction in power dissipation (only 3%) is achieved (as compared to Tables I and III) since the line thickness is larger. For a higher aspect ratio, the coupling capacitance is greater, increasing the per cent reduction in power dissipation in tapered lines. As technologies advance, a higher aspect ratio and interconnect thickness becomes typical. The proposed tapering technique will therefore achieve a greater reduction in power with technology scaling.

V. Conclusions

A structure for sizing the interconnects within an H-tree network is proposed. The structure does not maintain a tapering factor of two in the line width at the branch points along the H-tree. The proposed technique reduces power dissipation while improving the signal characteristics.

First- and second-order approximations of the transfer function can be used to size tapered lines of a clock distribution network. The first-order approximation reduces the power dissipation and inductive noise of an H-tree structured clock distribution network. Alternatively, a second-order approximation can be used to achieve a greater reduction in both power dissipation and inductive noise.

Exponentially tapered interconnects based on a first-order approximation are shown to reduce the power dissipated by an industrial clock distribution network by up to 12% while maintaining the same signal transition times and propagation delay at the load. A higher reduction in power dissipation of 15% is achieved when the second moment is used in the optimization process. This exponential tapering technique is expected to be more efficient with advancements in technology.

Furthermore, the inductive behavior of the interconnects is reduced, decreasing the inductive noise. Smaller reflections occur in an exponentially tapered tree. A reduction of 35% in the difference between the signal overshoots at the input of a tree is achieved, increasing the efficiency of using exponential tapering in propagating signals at high frequencies. As compared to a uniform tree with the same area overhead, the difference between the overshoots is reduced by 40%.

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