Transactions Briefs

Shielding Effect of On-Chip Interconnect Inductance

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***Abstract*—Interconnect inductance introduces a shielding effect which decreases the effective capacitance seen by the driver of a circuit, reducing the gate delay. A model of the effective capacitance of an RLC load driven by a CMOS inverter is presented. The interconnect inductance decreases the gate delay and increases the time required for the signal to propagate across an interconnect, reducing the overall delay to drive an RLC load. Ignoring the line inductance overestimates the circuit delay, inefficiently oversizing the circuit driver. Considering line inductance in the design process saves gate area, reducing dynamic power dissipation. Average reductions in power of 17% and area of 29% are achieved for example circuits. An accurate model for a CMOS inverter and an RLC load is used to characterize the propagation delay. The accuracy of the delay model is within an average error of less than 9% as compared to SPICE.**

***Index Terms*—CMOS, gate delay, interconnect modeling, on-chip inductance, propagation delay, RLC interconnects, shielding effect.**

I. Introduction

With the decrease in feature size of CMOS circuits, on-chip interconnect dominates both circuit delay and power dissipation. Interconnect resistance increases the importance of modeling the interconnect as a distributed load. Based on different RC models, the signal propagation delay through a resistive load has been characterized [1], [2]. These models consider the delay of the passive load, ignoring the delay of the gate which drives the load. Furthermore, the effect of the load resistance on the gate delay is not considered. The driver gate should also be included in the delay model for enhanced delay estimation [3], [4]. Based on a reduced-order model of the driving point impedance [5] the concept of an effective capacitance has been introduced in [6] to better determine the gate delay. An iterative approach is proposed to determine the delay of a gate driving an RC tree. It has been shown that the effective capacitance of a distributed load is less than the total load capacitance, effectively reducing the gate delay. An enhanced method has been developed to replace the iterative approach [7]. As shown in [8], an effective capacitance improves the accuracy of the delay model.

To determine the effective capacitance seen by a driver, a reduced-order model for the driving-point admittance is required. An efficient model for the driving-point characteristics of resistive interconnects is presented in [5] and [9]. An accurate approximation is provided to estimate the delay of a gate driving an RC load [6]. The inductive behavior of interconnect, however, can no longer be neglected, particularly in long, low resistance interconnect lines [10], [11]. The inductive interconnect increases the on-chip noise as well as the computational complexity of the design process. Furthermore, the on-chip inductance affects certain design techniques such as repeater insertion [12]. It is shown in this brief that the on-chip inductance can also decrease the signal propagation delay. The concept of an effective capacitance based on a high-order model for the driving point admittance can be used to determine the gate delay of an RLC load.

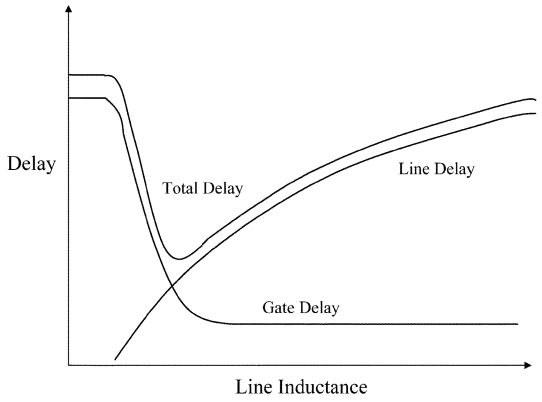

Fig. 1. Propagation delay as a function of the line inductance.

The propagation delay of an inductive load has been previously analyzed in the literature. Most of these investigations replace the driver with a linear resistance [12]–[14]. The accuracy of these models depends upon the ratio between the driver impedance and the load impedance and the accuracy of the model used to represent the equivalent impedance of the driver. The work described in [15] uses a more accurate driver model, with a lumped model for the load. A more accurate model for both the driver and the load is used in this brief to demonstrate a new concept, the shielding effect of the load inductance. The shielding effect of the load inductance is used to characterize the effective capacitance of an RLC load. To determine the effective capacitance of an RLC load, a realizable reduced-order model is used to characterize the load [16]–[18].

As shown in this brief, the line inductance decreases the delay of the gate driving the load, increasing the interconnect delay. The total circuit delay may decrease with higher inductance, as shown in Fig. 1. This result is the first to show (to the authors' knowledge) that interconnect inductance can decrease the delay of a circuit. The minimum delay occurs when the load is matched with the driver. From a noise perspective, the line inductance should be suppressed. As described in this brief, however, the line inductance can save power and area. Furthermore, if the line is matched with the driver, any ringing effects are eliminated in the signal waveform.

This brief is organized as follows. In Section II, the effective capacitance of an RLC load as compared to an RC load is presented. The effect of inductive shielding on the total propagation delay is discussed in Section III. In Section IV, a comparison between inductive shielding and resistive shielding is described. An analytic solution for the signal propagation delay of an inverter driving an inductive load is provided in Section V. In Section VI, a comparison between the analytic model and simulation is presented. Some conclusions are offered in Section VII.

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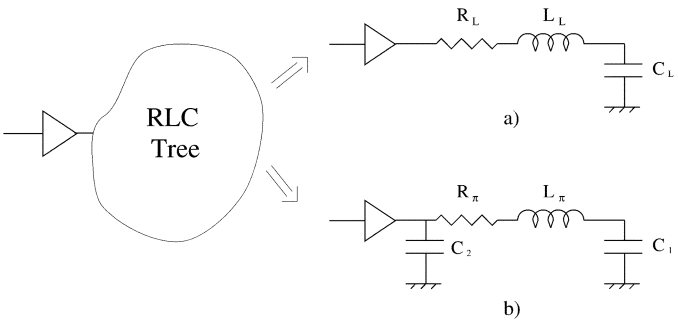

Fig. 2. Reduced-order model for a general RLC tree. (a) Lumped model. (b) π_{21} model.

II. Effective Capacitance of RLC Interconnect

Reduced-order models are used to increase the computation efficiency of the timing analysis process. A lumped model of an RLC load which uses the first two moments of the transfer function is shown in Fig. 2(a). The lumped model suffers from significant inaccuracy. Furthermore, the shielding effect of the load inductance is not considered. A circuit representation of a three moment reduced-order model (π_{21} model) is shown in Fig. 2(b) [5].

An efficient technique is presented in [16] to determine the values of R_π, L_π, C_1, and C_2 for a general RLC load. If the interconnect inductance is not considered, the π_{21} RLC model reduces to an π_{21} RC model with the same values of R_π, C_1, and C_2 [17] and [18].

Intuitively, the effective capacitance is the equivalent capacitance which replaces the reduced-order π_{21} model while producing the same delay at the load. The effective capacitance of an RLC load is

$$C_{\text{eff}-\text{RLC}} = C_2 + C_{x-RLC} \tag{1}$$

where C_{x-RLC} is characterized in Appendix A. C_{x-RLC} is less than C_1, reducing the total capacitance seen by the driver for the π_{21} model as compared to a lumped model. C_{x-RC} is determined for an RC load in [6]. C_{x-RLC} is less than C_{x-RC} for an inductive load. C_{x-RLC} decreases with increasing load inductance since the inductive shielding effect increases. The gate delay is proportional to the effective capacitance seen at the driving point. Since the effective capacitance decreases for larger inductances, the gate delay decreases. The interconnect inductance shields part of the load capacitance, reducing the gate delay.

For a total load capacitance and resistance of 400 fF and 100 Ω, respectively, the impedance parameters of the π_{21} model are $R_\pi = 48\,\Omega$, $C_2 = 67$ fF, and $C_1 = 333$ fF [17]. As shown in [17] and [18], L_π is linearly dependent on the load inductance. In order to characterize the effective capacitance for different load inductances, the ratio between the effective capacitance of an RLC model and an RC model is determined. The ratio between the effective capacitance of the π_{21} RLC and RC models for different load inductances is shown in Fig. 3. The effective capacitance decreases as the load inductance increases.

The shielding effect of the interconnect inductance increases the importance of including the line inductance in the delay analysis [19]. Ignoring the inductance overestimates the circuit delay, requiring a larger buffer to drive the load. The effect of the interconnect inductance on the total signal propagation delay is discussed in Section III.

III. Effect of Line Inductance on the Delay Model

The effective capacitance can be used to characterize the gate delay. The signal propagation delay depends upon the active gate and passive interconnect components of the signal path. The gate delay is the time required to charge the capacitance seen through the equivalent resistance of the driver. The interconnect delay is the time required for the signal to propagate along the line. These two components cannot be separated as the driver and load represent a single system. The interconnect inductance reduces both the capacitance seen by the driver (as described in Section II) and the equivalent output resistance of the driver by increasing the period during which the driving transistors operate in saturation, reducing the overall gate delay.

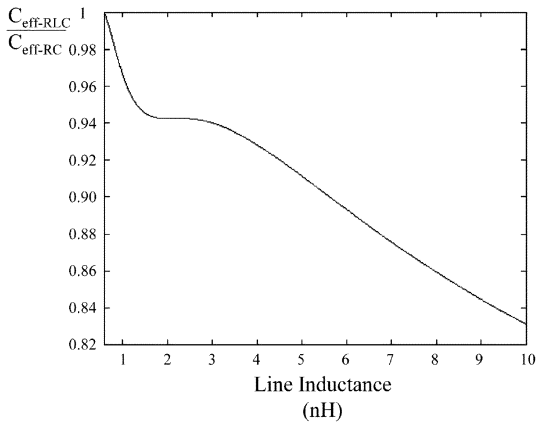

Fig. 3. Ratio between the effective capacitance of an RLC and RC load.

For an ideal source driving a distributed RLC line, however, the signal delay is primarily due to the line delay. The line inductance increases the signal propagation delay. For an ideal source driving an RLC line, the line delay can be modeled as [12]

$$t_{pd-RLC} = e^{-2.9\left(R_{\text{line}}(0.5C_{\text{line}}+C_L)/2\sqrt{L_{\text{line}}(C_{\text{line}}+C_L)}\right)^{1.35}} \times \sqrt{L_{\text{line}}(C_{\text{line}}+C_L)} + 0.74R_{\text{line}}(C_L+0.5C_{\text{line}}) \tag{2}$$

C_L is the load capacitance driven by the line and R_{int}, C_{int}, and L_{int} are the total line resistance, capacitance, and inductance, respectively.

The line delay increases with the line inductance as described in [19]. As the line inductance increases, two competing effects change the total delay of the signal, as shown in Fig. 1. The delay due to the active transistor decreases while the delay due to the passive interconnect increases.

To exemplify the effect of the line inductance on the propagation delay, a CMOS inverter driving a long inductive interconnect with $R_{\text{line}} = 50\ \Omega$ and $C_{\text{line}} = 400$ fF is considered. The total delay for different driver sizes based on a 0.24 μm CMOS technology is shown in Fig. 4. Different values of the line inductance with $C_L = 50$ fF are considered. Note the general similarity to Fig. 1.

The propagation delay decreases with increasing line inductance until a minimum delay is reached. The total delay decreases with higher line inductance over a wide range of driver size (the NMOS transistor size W_n ranges from 10 to 50 μm). For small drivers (i.e., $W_n < 5$ μm), the line inductance has no effect on the propagation delay since the delay is dominated by the driver output resistance. For large drivers (i.e., $W_n > 50$ μm), the line inductance increases the delay. The output resistance of these drivers is small and the interconnect delay dominates the total delay. Large drivers are not preferred as the decrease in signal delay is not significant, while the required area and dissipated power are large. Furthermore, the input gate capacitance is greater with larger drivers, increasing the load and therefore the delay of the previous logic stage. Cascaded buffer tapering can be used for large drivers, but the power dissipation increases due to the additional inverters (cascaded tapered inverters [20]) employed to reduce the delay.

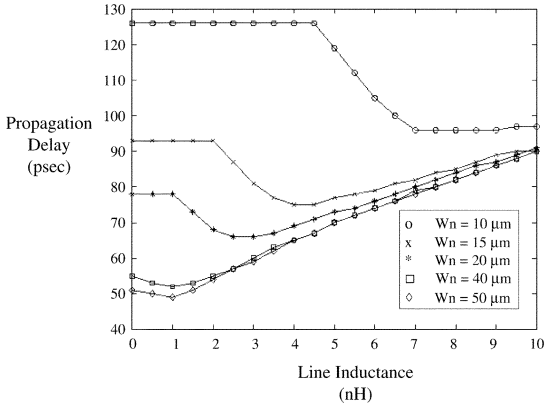

Fig. 4. Total delay for different values of line inductance and driver size of a distributed RLC interconnect as determined by the Cadence circuit simulator.

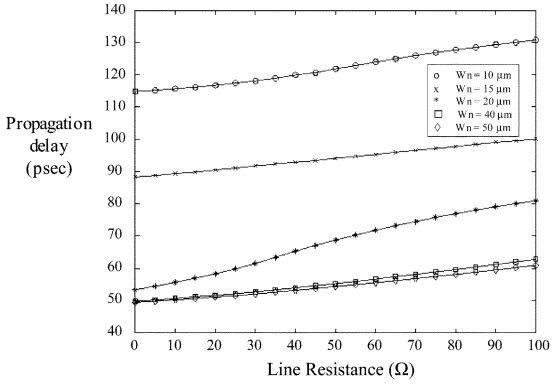

Fig. 5. Total delay for different values of line resistance and driver size for a distributed RLC interconnect (Cadence circuit simulator).

Curve fitting is used to determine the optimum value of the line inductance to achieve the minimum propagation delay. The minimum delay is determined over a wide range of line inductance (from 0.1 to 10 nH), load capacitance (from 10 to 250 fF), inverter size (from 5 to 50 μm), line capacitance (from 100 fF to 1 pF), and line resistance (from 25 Ω to 100 Ω). The minimum delay occurs when the ratio between the equivalent output resistance of the driver R_{tr} equals the magnitude of the lossy characteristic impedance of the line $|Z_{\rm line}|$ or $Z_T = 1$

$$Z_T = \frac{R_{tr}}{|Z_{\rm line}|} \tag{3}$$

$$R_{tr} = \frac{V_{dd}}{k_n (V_{dd} - V_{tn})^{\alpha}} + \frac{V_{dd}}{k_n \left[2(V_{dd} - V_{tn})V_{dd} - \frac{{V_{dd}}^2}{2}\right]} \tag{4}$$

$$|Z_{\rm line}| = \sqrt{\frac{\sqrt{{R_{\rm line}}^2 + (\omega L_{\rm line})^2}}{\omega C_{\rm line}}} \tag{5}$$

where $\omega = 2\pi/t_r$, V_{dd} is the supply voltage, k_n is the transconductance of the NMOS transistor of the driving inverter, V_{tn} is the threshold voltage of an NMOS transistor, $\alpha = 1.3$ and models the velocity saturation in a short-channel transistor, and t_r is the signal transition time at the output of the driving inverter. t_r is iteratively determined based on the concept of an effective capacitance.

The total propagation delay increases if the line inductance is less than the matched condition. Ignoring the line inductance overestimates the delay and the size of the driver. The line inductance is considered in Section VI in the design of an inverter driving a section of RLC interconnect. The savings in both power and area if line inductance is considered is noted.

Interconnect resistance also has a shielding effect on the gate delay. However, resistive shielding has a different effect on the total propagation delay. A comparison between the shielding effect of the interconnect resistance and inductance is described in Section IV.

IV. Inductive Shielding Versus Resistive Shielding

The shielding effect, which reduces the effective capacitance seen by a driver, exists in both RC and RLC loads. The interconnect resistance and/or inductance impedes the propagation of the signal along the line, shielding part of the total line capacitance. The effective capacitance for both RC and RLC lines is less than the total line capacitance, reducing the gate delay. For RC interconnects, the line delay is linearly proportional to the line resistance. The increase in the line delay is greater than the reduction in the gate delay. The total signal propagation delay increases with interconnect resistance, as shown in Fig. 5. The propagation delay of a CMOS inverter driving a distributed RLC line with $L_{\rm line} = 2$ nH is determined for the line parameters mentioned in Section III. Unlike the line inductance, the propagation delay increases with line resistance for different driver sizes.

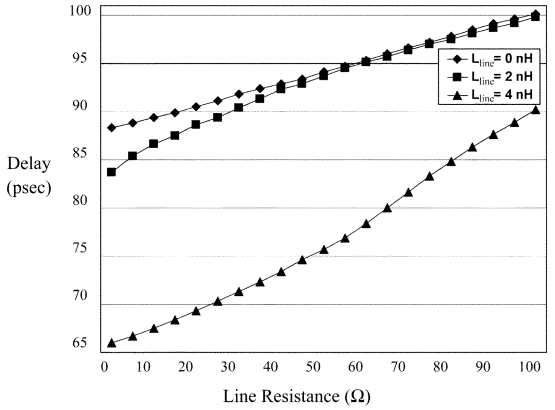

Fig. 6. Total delay for different values of line resistance and inductance of a distributed RLC interconnect (Cadence circuit simulator).

For highly inductive lines, the line resistance does not significantly affect the signal propagation delay. The propagation delay is $\propto \sqrt{L_{\rm line} C_{\rm line}}$ in lossless lines. This limiting case provides intuition describing the sublinear dependence between the line delay and the line inductance. The line delay is sublinearly proportional to the line inductance in RLC lines. The reduction in gate delay, with an increase in line inductance, decreases the total propagation delay of the signal as described in Section III.

As technology advances, new materials are used to reduce the line resistance and therefore the signal delay. These lower resistive materials increase the importance of considering the line inductance. As interconnect resistance decreases, the interconnect inductance has a greater effect on the signal characteristics. As shown in Fig. 6, the propagation delay decreases as the line resistance decreases. The reduction in the propagation delay is shown for different values of line inductance. The propagation delay decreases more rapidly for those lines with a larger inductance. A greater reduction in propagation delay can be achieved if low resistive materials are used in highly inductive lines.

For an inductive load, more sophisticated models are required to capture the effects of the interconnect inductance on the signal characteristics. An analytic solution characterizing the signal propagation delay of an inverter driving a reduced-order π_{21} model of a distributed RLC line is presented in Section V.

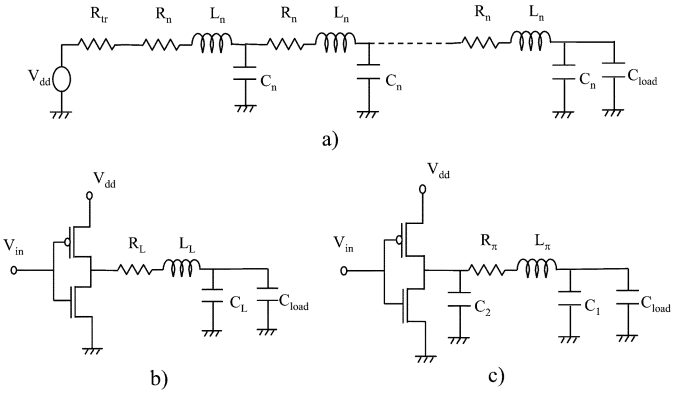

Fig. 7. Interconnect and driver models. (a) Distributed with constant source resistance [12]. (b) Lumped with nonlinear transistor model. [15] (c) π_{21} with nonlinear transistor model.

V. Propagation Delay of CMOS Inverter Driving an Inductive Load

Different models have been developed to determine the propagation delay of a CMOS gate (inverter) driving an RLC load. The propagation delay is used to refer to the total delay from the input of the gate to the load. Simple models are used in [12], [15] to simplify the circuit analysis process. A linear model of the driver transistor is not sufficiently accurate to characterize the propagation delay. The distributed model described in [12] is shown in Fig. 7(a). This model replaces the driver of an RLC interconnect with an equivalent resistance. The accuracy of the model depends upon the accuracy of modeling the nonlinear element (inverter) with a constant resistance. The lumped model used to determine the delay expression in [15] is shown in Fig. 7(b). This model suffers from inaccuracy since the shielding effect of the load inductance is not considered.

More accurate expressions to calculate the propagation delay of a CMOS inverter driving an RLC load based on the π_{21} model, which is shown in Fig. 7(c), are provided in Appendix B. As described in Section II, the interconnect inductance reduces the effective capacitance seen by the driver, reducing the gate delay. Furthermore, the inductance decreases the effective resistance of the driving gate, further reducing the gate delay. The load inductance impedes the flow of the current to the interconnect load, delaying when the driving transistor enters the saturation region. The reduction in the gate delay contributes to a reduction in the total propagation delay. A comparison between the three models for different load parameters is presented in Section VI.

VI. Simulation Results

Three different models are used to illustrate the importance of an accurate model to represent both the driver and the interconnect. In Table I, a comparison between the model described in [12], a lumped RLC model [15], and the π_{21} model (described in Appendix B) is listed. The π_{21} model achieves high accuracy, determining the delay with an average error of less than 9% for different line parameters.

The line inductance reduces the total signal propagation delay as discussed in previous sections of this brief. Including the inductance in the interconnect model is important in the design of a line driver. Excluding the inductance overestimates the delay of the circuit and underestimates the current sourced by the driver. Including the line inductance can reduce the driver size, saving both area and power.

A 0.24 μm CMOS technology is used to demonstrate the effect of including the line inductance in the design of a line driver. An interconnect line with $R_{\rm line} = 10\ \Omega/{\rm mm}$, $C_{\rm line} = 105\ {\rm fF/mm}$, and $L_{\rm line} = 650\ {\rm pH/mm}$ is assumed to determine the reduction in the size of the line driver if inductance is considered. A symmetric CMOS inverter is used to drive a line loaded by a capacitive load of 50 fF to achieve a target delay. The target delay and the driver size that achieves this delay are listed in Table II. A reduction in power dissipation of 5% and in gate area of 13% is achieved if line inductance is considered. As technology advances, different dielectric and line materials will be used to reduce the interconnect delay. Low-κ dielectric materials and copper interconnect will reduce both the line capacitance and resistance, increasing the effect of inductance on the signal behavior. A 17% reduction in power dissipation and 29% reduction in gate area is demonstrated for a low-κ copper interconnect example circuit.

TABLE I
Propagation Delay With Different Models for Different Line Inductances

$W_n = 20\ \mu$m, $R_{line} = 50\ \Omega$							
L_{line} nH	$C_{line} = 400$ fF						
	Cadence	Ismail/Friedman [12]		Tang/Friedman [15]		π_{21}	
	(psec)	psec	Error	psec	Error	psec	Error
0.0	77	35.2	-54.2%	59.5	-22.7%	68.2	-11.3%
1.0	74	35.7	-51.7%	62.2	-15.8%	70.0	-5.4%
2.0	67	38.1	-43.0%	66.6	-0.5%	64.7	-3.4%
3.0	68	41.4	-39.0%	97.8	43.8%	63.3	-6.8%
4.0	70	45.0	-35.6%	101.8	45.5%	72.6	3.8%
5.0	73	48.6	-33.4%	105.2	44.1%	80.3	10.0%
Maximum		-54.27%		-45.95%		-11.35%	
Average		41.51%		30.75%		6.11%	
L_{line} nH	$C_{line} = 1$ pF						
	Cadence	Ismail/Friedman [12]		Tang/Friedman [15]		π_{21}	
	(psec)	psec	Error	psec	Error	psec	Error
0.0	148	86.3	-41.6%	97.8	-33.8%	130.1	-12.0%
1.0	147	86.4	-41.2%	93.3	-36.5%	129.6	-11.7%
2.0	153	87.0	-43.0%	86.5	-43.4%	131.5	-14.0%
3.0	145	88.7	-38.7%	81.1	-44.0%	134.2	-7.3%
4.0	132	91.1	-30.9%	76.6	-41.9%	122.5	-7.1%
5.0	118	94.0	-20.2%	96.8	-17.8%	117.1	-0.7%
Maximum		-43.00%		-45.64%		-14.00%	
Average		36.23%		38.69%		8.91%	

VII. Conclusions

The shielding effect of interconnect inductance is introduced. The effective capacitance of an RLC load decreases with increasing line inductance, reducing the gate delay of a driver. Furthermore, the line inductance reduces the equivalent output resistance of a driver, reducing the total propagation delay. Resistive shielding, however, does not reduce the propagation delay since the increase in the line delay is typically greater than any reduction in the gate delay.

A parameter Z_T, the ratio between the output driver resistance and the magnitude of the lossy characteristic impedance of the line, is introduced to characterize the signal propagation delay of a CMOS inverter driving an RLC interconnect. The minimum propagation delay is achieved when $Z_T = 1$, where the driver is matched with the lossy characteristic impedance of the line.

The line inductance can significantly affect the resulting circuit performance. A smaller line driver can be used to drive an interconnect line if the line inductance is considered, more accurately achieving the target delay than if the line inductance is ignored. Furthermore, the per cent savings in both area and power dissipation is expected to increase as technology advances. A reduction of 17% in power dissipation and 29% in gate area is achieved for an example circuit.

An accurate model of the propagation delay of a CMOS inverter driving an RLC load is provided. An error of less than 9% as compared to dynamic circuit simulation is exhibited.

TABLE II
REDUCTION IN AREA AND POWER DISSIPATION WHEN CONSIDERING LINE INDUCTANCE FOR DIFFERENT DIELECTRIC AND LINE MATERIALS

Dielectric material	Resistivity	Target delay (psec)	W_n (μm)		Per cent reduction in power dissipation	Per cent reduction in area
			RC	RLC		
SiO_2	Aluminum	100	19	16.5	5%	13%
	Copper	100	17.8	15.2	6%	15%
Low-κ	Aluminum	60	23	19	9%	17%
	Copper	60	21	15	17%	29%

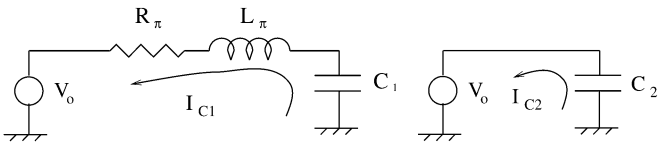

Fig. 8. Discharge currents for the π_{21} RLC model.

APPENDIX A
EFFECTIVE CAPACITANCE OF AN RLC LOAD

In order to compare the effective capacitance of RC and RLC delay models, the signal transition time at the output of a driving inverter V_o is assumed equal for both models. The waveform used in [6] is assumed to compare the effective capacitance of an RLC model with the model described in [6].

$$V_o(t) = \begin{cases} V_{dd} - ct^2, & \text{for } 0 \le t \le t_x \\ a + b(t - t_x), & \text{for } t_x \le t \le t_D \end{cases} \tag{A.1}$$

where $b = -0.8(V_{dd}/t_r)$ and t_x, t_D, a, and c are constants that characterize the waveform of V_o. t_r is the transition time of V_o which is obtained iteratively after determining the effective capacitance. The waveform of a signal propagating along an RLC line may be distorted by the inductance. However, the effect of this distortion on the effective capacitance is not significant. The effective capacitance of the π_{21} model is the capacitance which draws a current equal to the average current drawn from both C_1 and C_2 in the π_{21} model [6]. The average currents, I_{c1-av} and I_{c2-av}, discharge (for an output high-to-low transition) the capacitances C_1 and C_2, respectively, as shown in Fig. 8. Laplace transforms are used to obtain an expression for I_{c1-av} [19].

Equalizing the average current required to drive an effective capacitance $I_{\mathrm{Ceff-av}}$ with the summation of I_{C1-av} and I_{C2-av}, the effective capacitance $C_{\mathrm{eff-RLC}}$ can be expressed as

$$C_{\mathrm{eff-RLC}} = C_2 + \frac{t_D}{2ct_x(t_D - \frac{t_x}{2})} I_{c1-av}. \tag{A.2}$$

APPENDIX B
PROPAGATION DELAY BASED ON π_{21} REDUCED-ORDER MODEL

As shown in [2], the signal waveform shape is important for accurately estimating the delay. A ramp input signal is assumed to determine the propagation delay of a CMOS inverter driving a π_{21} model for an RLC load. To determine an analytic solution for the propagation delay assuming the π_{21} model shown in Fig. 7(c), an expression for the signal waveform across C during a high-to-low transition $V_c(t)$ is determined [19].

The propagation delay can be determined by numerically solving the nonlinear equation (B.1) to determine $t_{50\%}$

$$V_c(t_{50\%}) - \frac{V_{dd}}{2} = 0. \tag{B.1}$$

The propagation delay is

$$t_{pd} = t_{50\%} - \frac{t_{rIn}}{2} \tag{B.2}$$

where t_{rIn} is the transition time of the input signal of the driving gate.

REFERENCES

[1] W. C. Elmore, "The transient response of damped linear networks," *J. Appl. Phys.*, vol. 19, pp. 55–63, Jan. 1948.
[2] A. B. Kahng and S. Muddu, "Analysis of RC interconnections under ramp input," in *Proc. ACM/IEEE Design Autom. Conf.*, Jun. 1996, pp. 533–538.
[3] L. Chen, S. K. Gupta, and M. A. Breuer, "A new gate delay model for simultaneous switching and its applications," in *Proc. ACM/IEEE Design Autom. Conf.*, Jun. 2001, pp. 289–294.
[4] V. Adler and E. G. Friedman, "Repeater design to reduce delay and power in resistive interconnect," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 45, pp. 607–616, May 1998.
[5] P. R. O'Brien and T. L. Savarino, "Modeling the driving-point characteristic of resistive interconnect for accurate delay estimation," in *Proc. IEEE/ACM Int. Conf. Computer-Aided Design*, Nov. 1989, pp. 512–515.
[6] J. Qian, S. Pullela, and L. Pillage, "Modeling the effective capacitance for the RC interconnect of CMOS gates," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 13, pp. 1526–1535, Dec. 1994.
[7] A. B. Kahng and S. Muddu, "New efficient algorithms for computing effective capacitance," in *Proc. ACM Int. Symp. Physical Design*, Apr. 1998, pp. 147–151.
[8] C. V. Kashyap, C. J. Alpert, and A. Devgan, "An effective capacitance based delay metric for RC interconnect," in *Proc. IEEE/ACM Int. Conf. Computer-Aided Design*, Nov. 2000, pp. 229–234.
[9] A. Devgan and P. R. O'Brien, "Realizable reduction for RC interconnect circuits," in *Proc. IEEE/ACM Int. Conf. Computer-Aided Design*, Nov. 1999, pp. 204–207.
[10] Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Figures of merit to characterize the importance of on-chip inductance," *IEEE Trans. Very Large Scale (VLSI) Syst.*, vol. 7, pp. 442–449, Dec. 1999.
[11] B. Krautr, S. Mehrotra, and V. Chandramoouli, "Including inductive effects in interconnect timing analysis," in *Proc. IEEE Custom Integr. Circuits Conf.*, May 1999, pp. 445–452.
[12] Y. I. Ismail and E. G. Friedman, "Effects of inductance on the propagation delay and repeater insertion in VLSI circuits," *IEEE Trans. Very Large Scale (VLSI) Syst.*, vol. 8, pp. 195–206, Apr. 2000.
[13] R. Venkatesan, J. A. Davis, and J. D. Meindl, "Compact distributed RLC interconnect models—Part IV: Unified models for time delay, crosstalk, and repeater insertion," *IEEE Trans. Electron Devices*, vol. 50, pp. 1094–1101, Apr. 2003.
[14] K. Banerjee and A. Mehrotra, "Analysis of on-chip inductance effects for distributed RLC interconnects," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 21, pp. 904–915, Aug. 2002.
[15] K. T. Tang and E. G. Friedman, "Delay and power expressions characterizing a CMOS inverter driving an RLC load," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 3, May 2000, pp. 283–286.
[16] X. Yang, C.-K. Chang, W. H. Ku, and R. J. Carragher, "Hurwitz stable reduced order modeling for RLC interconnect trees," in *Proc. IEEE/ACM Int. Conf. Computer-Aided Design*, Nov. 2000, pp. 222–228.
[17] A. B. Kahng and S. Muddu, "Efficient gate delay modeling for large interconnect loads," in *Proc. IEEE Multi-Chip Module Conf.*, Feb. 1996, pp. 202–207.
[18] L. Yin and L. He, "An efficient analytical model of coupled on-chip RLC interconnects," in *Proc. ACM/IEEE Design Autom. Conf.*, Jan. 2001, pp. 385–390.
[19] M. A. El-Moursy and E. G. Friedman, "Shielding effect of on-chip interconnect inductance," in *Proc. IEEE Great Lakes Symp. VLSI*, Apr. 2003, pp. 165–170.
[20] B. S. Cherkauer and E. G. Friedman, "A unified design methodology for CMOS tapered buffers," *IEEE Trans. Very Large Scale (VLSI) Syst.*, vol. 3, pp. 99–111, Mar. 1995.