Low-Power Repeaters Driving *RC* and *RLC* Interconnects With Delay and Bandwidth Constraints

Guoqing Chen and Eby G. Friedman, *Fellow, IEEE*

***Abstract*—Interconnect plays an increasingly important role in deep-submicrometer very large scale integrated technologies. Multiple design criteria are considered in interconnect design, such as delay, power, and bandwidth. In this paper, a repeater insertion methodology is presented for achieving the minimum power in an *RC* interconnect while satisfying delay and bandwidth constraints. These constraints determine a design space for the number and size of the repeaters. The minimum power is shown to occur at the edge of the design space. With delay constraints, closed form solutions for the minimum power are developed, where the average error is 7% as compared with SPICE. With bandwidth constraints, the minimum power can be achieved with minimum-sized repeaters. The effects of inductance on the delay, bandwidth, and power of an *RLC* interconnect with repeaters are also analyzed. By including inductance, the minimum interconnect power under a delay or bandwidth constraint decreases as compared with an *RC* interconnect.**

***Index Terms*—Bandwidth, delay, interconnect, low power, RC, repeater, RLC.**

I. Introduction

REPEATER insertion is an efficient method for reducing interconnect delay and signal transition times in integrated circuits. The optimal number and size of the repeaters to achieve the minimum delay have been described in [1] for an *RC* interconnect, and in [2] for an *RLC* interconnect. The size of an optimal repeater is typically much larger than a minimum-sized repeater. Since millions of repeaters will be inserted to drive global interconnects in future high-complexity circuits [3], significant power will be consumed by these repeaters, particularly if delay-optimal repeaters are used. A power-delay tradeoff is, therefore, necessary to support efficient repeater insertion design methodologies [4].

The number and size of the repeaters to minimize the dynamic power and area of an interconnect while satisfying a target delay constraint have been described by Nalamalpu and Burleson in [5]. Burleson *et al.* further compared repeaters with boosters in [6]. The input transition time of a repeater is generally greater than the output transition time. In this case, the short-circuit power can be comparable or even greater than the dynamic power [7]. With CMOS technology scaling, leakage power is increasing rapidly, and is expected in future technologies to reach the same magnitude as the dynamic power [8]. By including both short-circuit and leakage power, a low-power repeater design methodology is presented in [9]. The power is minimized with a 5% delay penalty. Closed-form solutions, however, are not provided. In these papers, inductance effects are also not included. In upper metal layers, wide interconnects are frequently used, which have low resistance, making inductance effects nonnegligible in high-speed circuits.

With on-chip signal frequencies continuously increasing, bandwidth has become another important criterion in interconnect design. In this paper, a new repeater insertion methodology is proposed for achieving the minimum power while satisfying delay and bandwidth constraints. This paper is an extended version of [10] and [11]. Different power components of the interconnect are compared and multiple constraints are considered. The paper is organized as follows. In Section II, the timing and power models of *RC* interconnects are reviewed. Based on these models, analytic methods are presented for achieving the minimum power while satisfying delay and bandwidth constraints. In Section III, the effects of inductance on this repeater design methodology are analyzed. Finally, some conclusions are offered in Section IV.

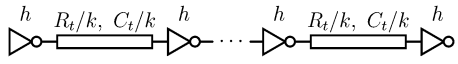


Fig. 1. Repeater insertion in a long *RC* interconnect line.

II. Power Dissipation in an *RC* Interconnect With Delay and Bandwidth Constraints

By including the effects of the input transition time, a timing model of an *RC* interconnect with repeaters is presented in Section II-A. The three primary power dissipation sources in interconnects are reviewed in Section II-B. Given a delay or a bandwidth constraint, a design space for a repeater system can be determined. The minimum achievable power in this design space is described in Sections II-C and D for delay and bandwidth constraints, respectively. Multiple constraints are analyzed in Section II-E.

A. Delay and Transition Time Model of RC Interconnects

As shown in Fig. 1, a distributed *RC* interconnect is evenly divided into k segments by repeaters. R_t and C_t are the total resistance and capacitance, respectively, of the interconnect. The repeaters are h times as large as a minimum-sized repeater,

Manuscript received February 1, 2005; revised August 29, 2005. This work was supported in part by the Semiconductor Research Corporation under Contract 2003-TJ-1068 and 2004-TJ-1207, the National Science Foundation under Contracts CCR-0304574, the Fulbright Program under Grant 87481764, a grant from the New York State Office of Science, Technology and Academic Research to the Center for Advanced Technology in Electronic Imaging Systems, and by grants from Intel Corporation, Eastman Kodak Company, and Manhattan Routing.

The authors are with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY 14627-0231 USA (e-mail: guchen@ece.rochester.edu; friedman@ece.rochester.edu).

Digital Object Identifier 10.1109/TVLSI.2005.863750

TABLE I
DEVICE PARAMETERS OF BPTM 45-nm MODEL. $V_{\rm dd} = 1.1$ V

Device	Temp. (°C)	I_{dsat}/W (μA/μm)	I_{sub}/W (nA/μm)	$\lvert V_t\rvert$ (volts)	$\lvert V_{dsat}\rvert$ (volts)	α
NMOS	25	1064	42.7	0.330	0.468	0.91
NMOS	100	1035	712.0	0.257	0.516	0.88
PMOS	25	534	25.3	0.325	0.600	1.05
PMOS	100	514	374.1	0.243	0.672	0.97

with the output resistance $R_{\rm tr0}/h$, output capacitance hC_{d0}, and input capacitance hC_{g0}, where $R_{\rm tr0}$, C_{d0}, and C_{g0} are the output resistance, output capacitance, and input capacitance, respectively, of a minimum-sized repeater.

The repeater is assumed in this paper to be implemented as a CMOS inverter. The inverter is also assumed to be symmetric such that the effective output resistance is the same for both rising and falling signal transitions. The Berkeley predictive technology model (BPTM) [12], [13] for a 45-nm printed channel length is used, corresponding to the 80-nm technology node described in the International Technology Roadmap for Semiconductors (ITRS) [8]. Some model parameters are modified to capture the trends of the saturated drain current and subthreshold current predicted by the ITRS. The device parameters used in this paper are listed in Table I, where α is the velocity saturation index and is determined with the method described in [14]. The PMOS transistor is 2.2 times as large as the NMOS transistor in the inverter, and the minimum gate width is assumed to be 45 nm.

C_{g0} and C_{d0} can be obtained with SPICE by measuring the charge stored on the input and output of the minimum-sized repeater during signal transitions. In this paper, $C_{g0} = 0.455$ fF and $C_{d0} = 0.413$ fF. $R_{\rm tr0}$ can be approximated as

$$R_{\rm tr0} = K\frac{V_{\rm dd}}{I_{\rm dn0}} \tag{1}$$

where K is a fitting parameter, and $I_{\rm dn0}$ is the saturated drain current of a minimum-sized NMOS transistor with both $V_{\rm gs}$ and $V_{\rm ds}$ equal to $V_{\rm dd}$. K can be determined by matching the 50% delay or transition time of the step response of an *RC* equivalent circuit to SPICE simulations. Note that the K obtained by matching the 50% delay and the K obtained by matching the transition time are different and are denoted as K_d and K_r, respectively. In this paper, K_d is 0.78 and K_r is 0.55. The corresponding output resistances are R_{d0} and R_{r0}.

The delay $t_{\rm ds}$ and transition time $t_{\rm rs}$ of a single interconnect stage for a step input can be obtained from [15]

$$t_{\rm ds} = 0.377\frac{R_tC_t}{k^2} + 0.693\left(R_{d0}C_0 + \frac{R_{d0}C_t}{hk} + \frac{R_tC_{g0}h}{k}\right) \tag{2}$$

$$\begin{aligned} t_{\rm rs} &= \frac{t_{90\%} - t_{10\%}}{0.8} \\ &= 1.1\frac{R_tC_t}{k^2} + 2.75\left(R_{r0}C_0 + \frac{R_{r0}C_t}{hk} + \frac{R_tC_{g0}h}{k}\right) \end{aligned} \tag{3}$$

where $C_0 = C_{d0} + C_{g0}$. With a finite input slew rate, both the repeater delay [14] and repeater output transition time [16] depend linearly on the input transition time t_{r_in}. The contribution of t_{r_in} to the repeater delay can be represented by γt_{r_in}. For a rising input, γ is determined as [14]

$$\gamma_r = \frac{1}{2} - \frac{1 - v_{\rm tn}}{1 + \alpha_n} \tag{4}$$

where $v_{\rm tn} = V_{\rm tn}/V_{\rm dd}$. By changing the suffix n to p in (4), the coefficient γ_f for a falling input can be obtained. An average of γ_r and γ_f is used as γ in the rest of this paper to determined the interconnect delay.

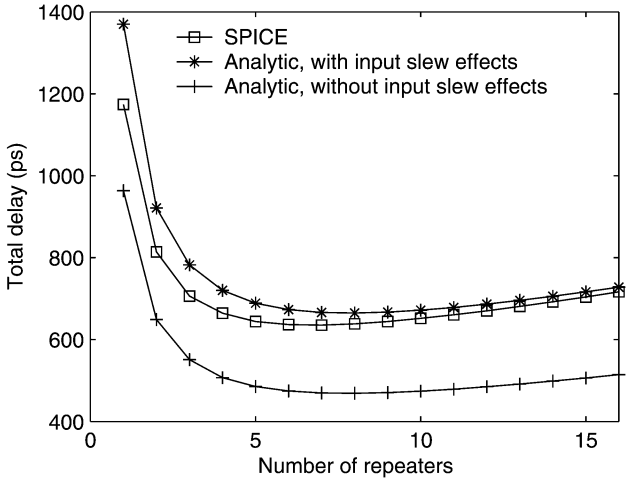


Fig. 2. Total delay for an *RC* interconnect driven by repeaters. $R = 0.31\ \Omega/\mu$m, $C = 0.223$ fF$/\mu$m, $l = 5$ mm, $h = 50$, and $T = 25\ ^\circ$C.

The linear dependence of the repeater output transition time on t_{r_in} is only valid for slow input signals with small load capacitances [16]. Furthermore, the signal is degraded by the interconnect impedance before reaching the far end, decreasing the sensitivity of the far end transition time to the input slew rate. The effect of the input slew rate on the far end transition time is, therefore, ignored in this paper. The signal transition times determine the highest switching speed an on-chip signal can achieve, i.e., the bandwidth of the circuit. The total delay of the interconnect is

$$\begin{aligned} T_{\rm total} &= k(t_{\rm ds} + \gamma t_{\rm rs}) \\ &= a_1\frac{R_tC_t}{k} + a_2\left(R_0C_0k + \frac{R_0C_t}{h} + R_tC_{g0}h\right) \end{aligned} \tag{5}$$

where

$$a_1 = 0.377 + 1.1\gamma \tag{6}$$

$$a_2 = 0.693 + 2.75\gamma \tag{7}$$

$$R_0 = \frac{0.693R_{d0} + 2.75\gamma R_{r0}}{a_2}. \tag{8}$$

The total delay obtained from (5) as well as the model neglecting input transition time effects are compared with SPICE in Fig. 2 for different numbers of repeaters. In the SPICE simulation, the first driver and the far end load are assumed to be implemented by the same sized repeater. The input signal slew of the first driver is assumed to be the same as the signal slew at the end of the interconnect. The interconnect parameters are extracted for a minimum-sized global interconnect at the 80-nm technology node [8]. As shown in Fig. 2, neglecting the effects of the

input transition time significantly underestimates the total delay. When the number of repeaters is small, each repeater drives a long interconnect. The signal transition time at the input of each repeater (the output of the previous stage) is sufficiently large; therefore, the assumption made in [14] ($t_{r\_in} < 3t_{r\_out}$) is no longer valid. The gate delay does not increase linearly with the input transition time and (5) becomes less accurate. This situation will normally not occur in practical circuits due to the slow transition time. In this example, when more than four repeaters are inserted, the error of (5) is within 7% of SPICE.

By setting $\partial T_{\text{total}}/\partial k$ and $\partial T_{\text{total}}/\partial h$ to zero, the optimal k and h to minimize T_{total} can be obtained

$$k_{\text{opt}} = \sqrt{\frac{a_1 R_t C_t}{a_2 R_0 C_0}} \tag{9}$$

$$h_{\text{opt}} = \sqrt{\frac{R_0 C_t}{R_t C_{g0}}}. \tag{10}$$

The corresponding minimum delay is

$$T_{\min} = 2\sqrt{a_1 a_2 R_t C_t R_0 C_0}\left(1 + \sqrt{\frac{a_2 C_{g0}}{a_1 C_0}}\right). \tag{11}$$

This delay-minimal repeater design methodology is not necessarily an appropriate strategy in practical circuits. First, the delay is not sensitive to the size of the repeaters near the optimal point, therefore, significant power and area are wasted to achieve only a small improvement in speed when approaching the optimal point (for minimum delay). Second, with increasing on-chip signal frequencies, it is possible that a delay-minimal design methodology will not satisfy the specific bandwidth requirement.

B. Power Dissipation Components in Interconnects With Repeaters

Power dissipation is a primary criterion in VLSI circuits due to high integration densities and high speeds. There are three significant power dissipation mechanisms in digital CMOS circuits: dynamic power, short-circuit power, and leakage power.

1) Dynamic Power: Dynamic power is the power consumption due to charging and discharging the load capacitance. Dynamic power has been well studied and is characterized by the following well-known expression:

$$P_d = \alpha_s f C_L V_{\text{dd}}^2 \tag{12}$$

where f is the clock frequency and α_s is the switching factor (assumed here as 0.15 [9]). For an *RC* interconnect with repeaters, the load capacitance C_L includes both the interconnect capacitance and the parasitic capacitance of the repeaters. The total dynamic power in a *RC* line with repeaters is

$$P_d = \alpha_s f C_L V_{\text{dd}}^2 = \alpha_s f (C_t + khC_0) V_{\text{dd}}^2. \tag{13}$$

2) Short-Circuit Power: If the signal applied at the input of a CMOS inverter has a finite slew rate, a direct current path exists between V_{dd} and ground when the input signal switches between V_{tn} and $V_{\text{dd}} + V_{\text{tp}}$. The power consumed in this way

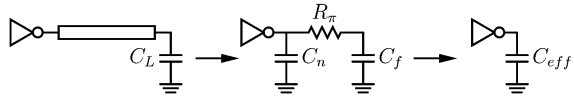


Fig. 3. π model representation of a distributed *RC* interconnect and the effective capacitance.

is called short-circuit power [17]. The short-circuit power is a function of the input transition time, output load capacitance, and the size of the transistor. A closed-form model of the short-circuit power [18] is adopted here because the model provides a clear relationship between the short-circuit power and related circuit parameters. From this model, the short-circuit energy dissipated in a CMOS inverter during a full signal switch ($0 \to 1 \to 0$) can be approximated as

$$E_s = \frac{4 I_{\text{dsat}}^2 t_r^2 V_{\text{dd}}}{V_{\text{dsat}} G C_{\text{out}} + 2H I_{\text{dsat}} t_r}. \tag{14}$$

In this expression, C_{out} is the output load capacitance. $V_{\text{dsat}} = (V_{\text{dsatn}} + V_{\text{dsatp}})/2$ and $I_{\text{dsat}} = (I_{\text{dsatn}} + I_{\text{dsatp}})/2$. $G = (G_r + G_f)/2$ and $H = (H_r + H_f)/2$. G_r and H_r are the coefficients associated with rising inputs, and can be determined as [18]

$$G_r = \frac{(\alpha_n + 1)(1 - v_{\text{tn}})^{\alpha_n}(1 - v_{\text{tp}})^{\alpha_p/2}}{F_r(1 - v_{\text{tn}} - v_{\text{tp}})^{\alpha_p/2 + \alpha_n + 2}} \tag{15}$$

$$H_r = \frac{2^{\alpha_p}(\alpha_p + 1)(1 - v_{\text{tp}})^{\alpha_p}}{(1 - v_{\text{tn}} - v_{\text{tp}})^{\alpha_p + 1}} \tag{16}$$

where

$$F_r = \frac{1}{\alpha_n + 2} - \frac{\alpha_p}{2(\alpha_n + 3)} + \frac{\alpha_p\left(\frac{\alpha_p}{2} - 1\right)}{\alpha_n + 4}. \tag{17}$$

G_f and H_f can be obtained by exchanging the n and p suffixes in (15)–(17). The total capacitance in a single interconnect stage includes the output parasitic capacitance of the repeater, the interconnect capacitance, and the input capacitance of the following repeater:

$$C_{\text{stage}} = C_0 h + \frac{C_t}{k}. \tag{18}$$

Due to the shielding effect of the interconnect resistance, the load capacitance seen by the repeater is less than C_{stage} during an input signal transition. An effective capacitance C_{eff}, therefore, needs to be determined to estimate the short-circuit power. In order to obtain C_{eff}, the interconnect is first approximated by a π model which matches the first three moments of the admittance at the repeater output, as shown in Fig. 3. The π model parameters can be obtained from the method presented in [19]. The effective capacitance of this π structure can be obtained in a similar way as in [20]. In [20], the driver output waveform is approximated by a quadratic function followed by a linear function. The output waveform of the repeaters generally follows a quadratic function during the input transition time. With this assumption, the effective capacitance of the π model can be determined as

$$C_{\text{eff}} = C_n + C_f\left[1 - 2\sigma + 2\sigma^2(1 - e^{-(1/\sigma)})\right] \tag{19}$$

where $\sigma = R_\pi C_f / t_{\rm ev}$, and $t_{\rm ev}$ is the time when the effective capacitance is evaluated. As expected, $C_{\rm eff}$ is between C_n and $C_n + C_f$. σ can be viewed as a metric charactering the shielding effect of the resistance. With increasing σ, $C_{\rm eff}$ decreases from $C_n + C_f$ to C_n. The effective capacitance should be evaluated to determine the short-circuit current, which flows during a non-step input signal transition. By fitting SPICE simulations, the evaluation time is determined as $t_{\rm ev} = 0.46(1 - v_{\rm tn} - |v_{\rm tp}|)t_r$. The total short-circuit power of the inserted repeaters, therefore, is

$$P_s = \frac{4\alpha_s f I_{d0}^2 t_r^2 V_{\rm dd} k h^2}{V_{\rm dsat} G C_{\rm eff} + 2 H I_{d0} t_r h} \tag{20}$$

where I_{d0} is the average saturated drain current of the NMOS and PMOS transistors in a minimum-sized repeater, and $C_{\rm eff}$ is the effective capacitance of each interconnect stage.

3) Leakage Power: In deep-submicrometer CMOS technologies, the dominant leakage current source is composed of subthreshold current and gate leakage current [21]. The total leakage power dissipated in the repeaters is

$$P_l = hkV_{\rm dd}(I_{sub0} + I_{g0}) \tag{21}$$

where $I_{\rm sub0}$ is the average subthreshold current of the NMOS and PMOS transistors in a minimum-sized repeater. I_{g0} is the average gate leakage current of a minimum-sized repeater with low and high inputs. The leakage power is expected to dominate dynamic power and short-circuit power in future advanced technologies and high complexity systems, especially for those interconnects with low switching activities. Since the subthreshold current increases rapidly with increasing temperature, a worst case temperature of 100 °C is assumed in this paper to emphasize the leakage power. In this case, $I_{\rm sub0} = 34.5$ nA and $I_{g0} = 1.4$ nA.

C. Power Dissipation With Delay Constraints

For a delay constraint $T_{\rm req}$ greater than $T_{\rm min}$, the design space of the repeaters can be characterized as $T_{\rm total} \le T_{\rm req}$, which is the area inside the closed curves shown in Fig. 4. From (5), the edge of the design space satisfies

$$a_1 \frac{R_t C_t}{k} + a_2 \left(R_0 C_0 k + \frac{R_0 C_t}{h} + R_t C_{g0} h \right) = T_{\rm req}. \tag{22}$$

With $T_{\rm req}$ approaching $T_{\rm min}$, the design space converges to the minimum delay point $(h_{\rm opt}, k_{\rm opt})$. Note in Fig. 4 that the minimum h that can satisfy the delay requirement occurs when $k = k_{\rm opt}$. Alternatively, the minimum k that can satisfy the delay requirement occurs when $h = h_{\rm opt}$.

The total power dissipated by an *RC* interconnect with repeaters is the summation of the three primary power dissipation components

$$P_{\rm total} = P_d + P_s + P_l. \tag{23}$$

In Fig. 5, $P_{\rm total}$ is plotted as a function of k and h. For each h, an optimal k exists to achieve the minimum power. If k is too small, the signal transition time will be large, and the total power is dominated by the short-circuit power. If k is too large, the total power is dominated by the dynamic power and leakage power. P_d and P_l increase linearly with increasing h for a fixed k. P_s, however, is more complicated. In order to obtain an analytic solution, some approximations are made to $C_{\rm eff}$. The effective capacitance $C_{\rm eff}$ in one stage is a function of h and k. The ratio between $C_{\rm eff}$ and $C_{\rm stage}$ is plotted in Fig. 6. In most cases, this ratio is varied in the range from 0.5 to 1. An average ratio of 0.75 is used in (20) to evaluate the short-circuit power. With this approximation, $\partial P_s / \partial h$ is always positive, which means that P_s increases monotonically with increasing h for a fixed k. The total power $P_{\rm total}$, therefore, also increases monotonically with increasing h for a fixed k. This behavior is illustrated in Fig. 5. For the design space shown in Fig. 4, the minimum power can only be reached on the left edge of the design space.

The power dissipation at the edge of the design space is plotted as a function of h in Fig. 7. The dynamic and leakage power is plotted together since both of these power components depend linearly on kh. For each repeater size h, there may exist two values of k, causing the same delay $T_{\rm req}$, as shown in Fig. 4. These two values of k correspond to two power values,

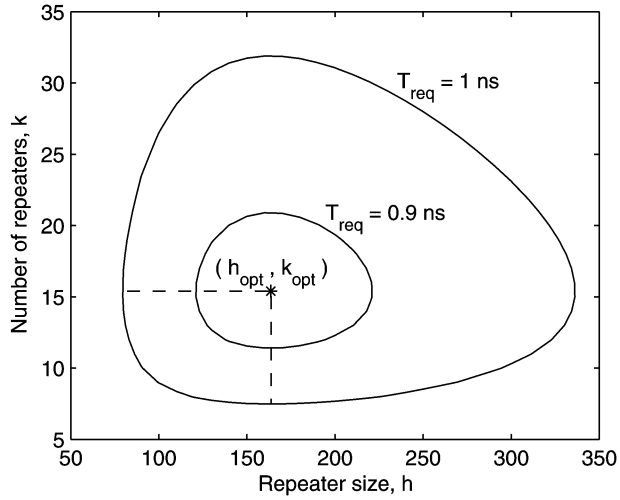


Fig. 4. Repeater design space with delay constraint. $R = 0.31\ \Omega/\mu$m, $C = 0.223$ fF$/\mu$m, and $l = 10$ mm.

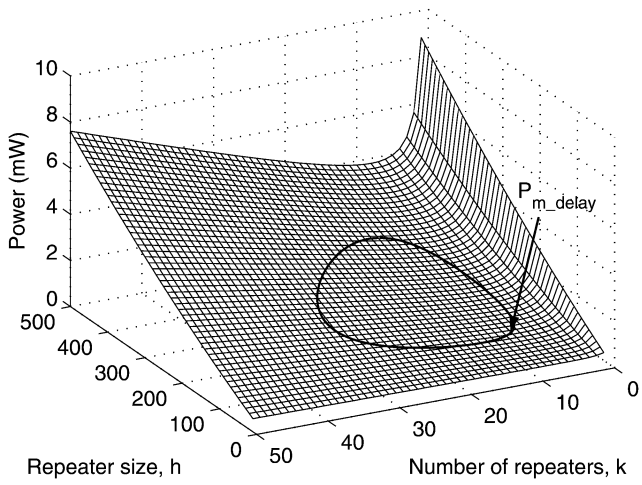


Fig. 5. Total power dissipation in an interconnect with repeaters as a function of h and k. $f = 1$ GHz, $R = 0.31\ \Omega/\mu$m, $C = 0.223$ fF$/\mu$m, and $l = 10$ mm.

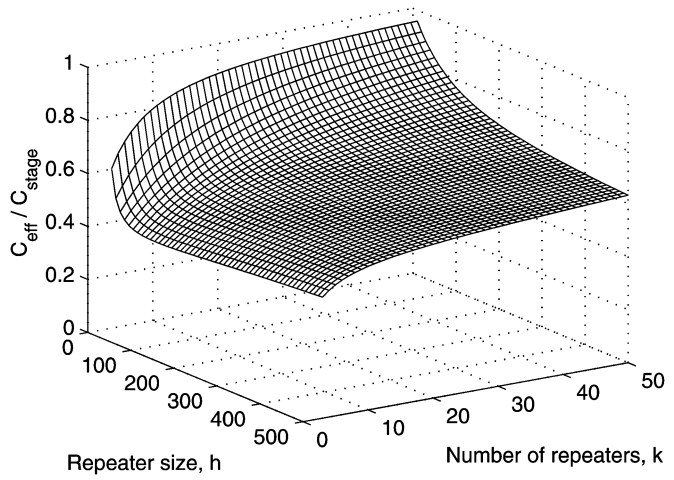


Fig. 6. Ratio of C_{eff} to C_{stage}. $R = 0.31\ \Omega/\mu$m, $C = 0.223$ fF$/\mu$m, and $l = 10$ mm.

as shown in Fig. 7. The minimum total power with delay constraints P_{m_delay} can be obtained by solving $dP_{\text{total}}/dh = 0$. Note that at the edge of the design space, k is a function of h. In order to provide a closed form solution for P_{m_delay}, the curve of $P_d + P_l$ around the power-optimal point is approximated by a part of an ellipse, as shown in Fig. 7(b). The optimal design parameters (h_0, k_0) for minimizing $P_d + P_l$ with a delay constraint T_{req} can be solved by the Lagrange method [5]

$$k_0 = \frac{-b - \sqrt{b^2 - T_{\text{req}}^2 a_1 a_2 R_0 C_0 R_t C_t}}{T_{\text{req}} a_2 R_0 C_0} \tag{24}$$

$$h_0 = \frac{T_{\text{req}} k_0 - 2a_1 R_t C_t}{2a_2 R_t C_{g0} k_0} \tag{25}$$

$$b = a_2 R_0 R_t C_t (a_2 C_{g0} - a_1 C_0) - \frac{T_{\text{req}}^2}{4}. \tag{26}$$

In Fig. 7(b), h_1 is the minimum repeater size that can satisfy a target delay constraint, which can be obtained by inserting $k_1 = k_{\text{opt}}$ into (22). P_0 and P_1 are the corresponding values of $P_d + P_l$ at (h_0, k_0) and (h_1, k_1), respectively. The curve of P_s is approximated by a linear function. With these approximations, the power-optimal repeater size h_p with a delay constraint is

$$h_p = h_0 - \frac{x_0 (h_0 - h_1)^2}{\sqrt{x_0^2 (h_0 - h_1)^2 + (P_1 - P_0)^2}} \tag{27}$$

where

$$x_0 = 4\alpha_s f I_{d0}^2 V_{\text{dd}} k_0^2 t_{r0}^2 \cdot \frac{1.5 V_{\text{dsat}} G (C_0 h_0 k_0 + C_t) h_0 + 2 H I_{d0} k_0 t_{r0} h_0^2}{\left[0.75 V_{\text{dsat}} G (C_0 h_0 k_0 + C_t) + 2 H I_{d0} k_0 t_{r0} h_0\right]^2} \tag{28}$$

$$t_{r0} = t_r(h_0, k_0). \tag{29}$$

A detailed derivation is provided in the Appendix. The corresponding k_p can be solved by inserting h_p into (22). Upon obtaining h_p and k_p, P_{m_delay} can be obtained directly from (23). If k_p is not an integer, the nearest two integers are used to determine the minimum power (h_p will need to be recalculated).

For different interconnect loads and delay constraints, results from the proposed method are compared with SPICE simulations as listed in Table II. The average error of the analytically obtained minimum power is 7%. In these experiments, the total power does not include the power consumed by the load buffer. In Table III, different power components from the analytic model are listed separately for delay-optimal circuits and power-optimal circuits with delay constraints. The dynamic power listed in the table is only due to the parasitic capacitance of the repeaters, since the dynamic power due to the interconnect capacitance is a constant for a specific interconnect. As compared with the power dissipation in a delay-optimal circuit, significant power savings is achieved by adopting a power-optimal circuit with delay constraints. For a power-optimal circuit, all of the three power components decrease with increasing delay targets. Note that for a delay-optimal circuit, the short-circuit power is slightly less than the dynamic power of the repeaters. For a power-optimal circuit with delay constraints, the short-circuit power can be greater than the dynamic power of the repeaters. The short-circuit power grows in significance with increasing delay targets. The leakage power is less than a quarter of the dynamic power of the repeaters for the examples listed in Table III.

The effect of switching factor α_s on the solution of the power-optimal design is illustrated in Fig. 8. The curve is step like since the corresponding k_p is an integer. As shown in Fig. 8, under a delay constraint, h_p decreases with increasing α_s. At the limiting case, $\alpha_s = 0$, only leakage power exists, and the optimal repeater size is $h_p = h_0$.

As shown in Fig. 7, the short-circuit power at the edge of the design space increases with increasing repeater size, while dynamic power and leakage power decrease with increasing repeater size around the power optimal solution. A larger repeater size with fewer number of repeaters is, therefore, preferable for dynamic and leakage power dominant cases, and a smaller repeater size with a greater number of repeaters is preferable for short-circuit power dominant cases. For circuits with low power supplies, the threshold voltage is normally reduced to maintain performance. The leakage power, therefore, is a more dominant component of the total power consumption. In this case, the optimal repeater size h_p is closer to h_0.

D. Power Dissipation With Bandwidth Constraints

The bandwidth of an interconnect is assumed in this paper to be limited solely by the output signal transition time. Faster signal transition times support a shorter signal bit period, therefore, a higher bandwidth. For a bandwidth constraint B_{req}, the signal transition time is assumed to be less than or equal to half the bit period, i.e., $t_r \leq 1/2(B_{\text{req}})$. The design space for different bandwidth constraints is shown in Fig. 9. The design space is the area in the upper right side of the curve. From (3), the expression characterizing the design space edge can be determined as

$$1.1\frac{R_t C_t}{k^2} + 2.75\left(R_{r0} C_0 + \frac{R_{r0} C_t}{hk} + \frac{R_t C_{g0} h}{k}\right) = \frac{1}{2B_{\text{req}}}. \tag{30}$$

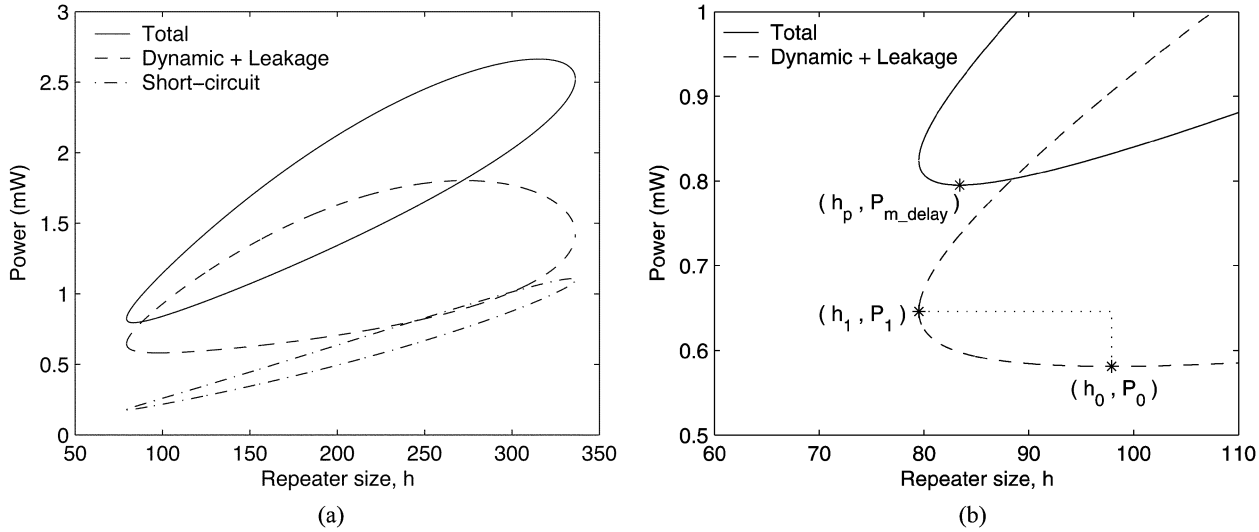


Fig. 7. Power dissipation with constant delay. $f = 1$ GHz, $T_{\rm req} = 1$ ns, $R = 0.31\ \Omega/\mu$m, $C = 0.223$ fF$/\mu$m, and $l = 10$ mm.

TABLE II
MINIMUM POWER WITH DELAY CONSTRAINTS OBTAINED ANALYTICALLY AS COMPARED WITH SPICE SIMULATIONS. $f = 1$ GHz

R_t (kΩ)	C_t (pF)	T_{req} (ps)	SPICE			Analytic			
			k_p	h_p	P_{m_delay} (μW)	k_p	h_p	P_{m_delay} (μW)	% Error
1	1	400	4	90	315.3	4	88.9	335.2	6.3
1	1	500	3	59	267.8	4	54.6	283.0	5.7
2	2	800	8	90	624.5	9	85.1	669.7	7.2
2	2	900	7	69	558.5	8	67.1	602.8	7.9
2	2	1000	7	56.5	528.3	7	56.7	565.8	7.1
3	1	700	7	47.5	300.6	7	49.7	331.1	10.1
3	1	800	7	36	274.9	7	36.6	296.2	7.7
3	1	900	6	30.5	260.7	6	30.6	277.5	6.4
2	3	1000	9	112	935.2	10	102.2	982.3	5.0
2	3	1200	9	71.5	801.6	9	71.1	857.4	7.0
2	3	1400	9	55	753.7	8	55.9	799.2	6.0

TABLE III
DIFFERENT POWER COMPONENTS DISSIPATED IN THE REPEATERS. $f = 1$ GHz

R_t (kΩ)	C_t (pF)	T_{req} (ps)	Delay-optimal			Power-optimal		
			P_{d_rep} (μW)	P_s (μW)	P_l (μW)	P_{d_rep} (μW)	P_s (μW)	P_l (μW)
1	1	400	182.2	171.7	45.7	56.0	73.8	13.6
1	1	500	182.2	171.7	45.7	34.4	50.8	8.4
2	2	800	364.3	343.3	91.3	111.9	147.5	27.2
2	2	900	364.3	343.3	91.3	84.5	117.2	20.6
2	2	1000	364.3	343.3	91.3	62.5	108.8	15.2
3	1	700	175.3	172.9	43.9	54.7	71.4	13.2
3	1	800	175.3	172.9	43.9	40.3	56.1	9.8
3	1	900	175.3	172.9	43.9	28.9	52.2	7.0
2	3	1000	520.6	519.6	130.5	160.9	208.0	39.1
2	3	1200	520.6	519.6	130.5	100.8	163.1	24.5
2	3	1400	520.6	519.6	130.5	70.4	145.5	17.1

From (30), k is solved as a function of h

$$k(h) = \frac{\sqrt{\tau_2^2 - 4.4\tau_1 R_t C_t} + \tau_2}{-2\tau_1} \tag{31}$$

where

$$\tau_1 = 2.75 R_{r0} C_0 - \frac{1}{2B_{\rm req}} \tag{32}$$

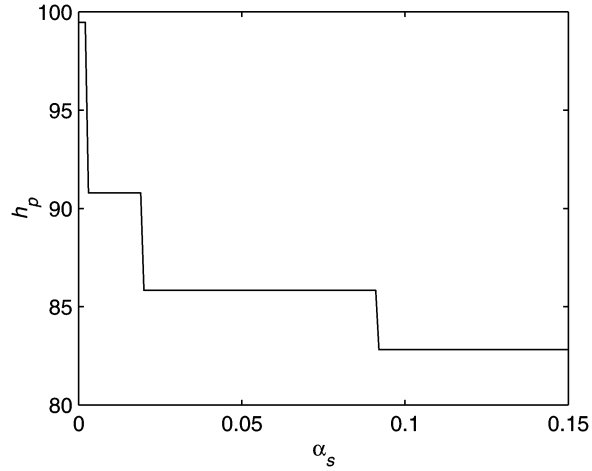


Fig. 8. Effect of α_s on the optimal repeater size h_p. $R = 0.31\ \Omega/\mu$m, $C = 0.223$ fF$/\mu$m, $l = 10$ mm, $f = 1$ GHz, and $T_{\rm req} = 1$ ns.

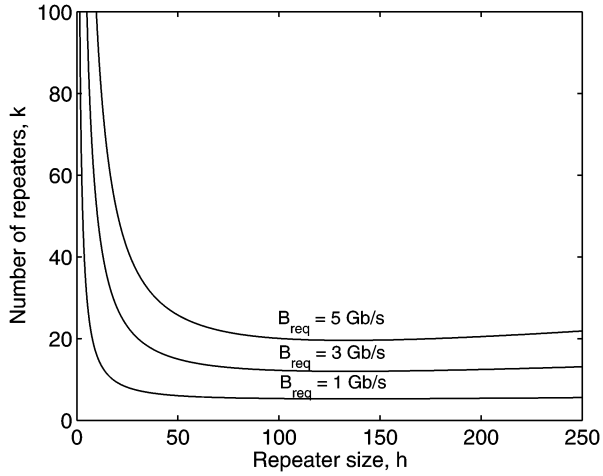


Fig. 9. Repeater design space with bandwidth constraints. $R = 0.31\ \Omega/\mu$m, $C = 0.223$ fF$/\mu$m, and $l = 10$ mm.

$$\tau_2 = 2.75\left(\frac{R_{r0}C_t}{h} + R_t C_{g0} h\right). \tag{33}$$

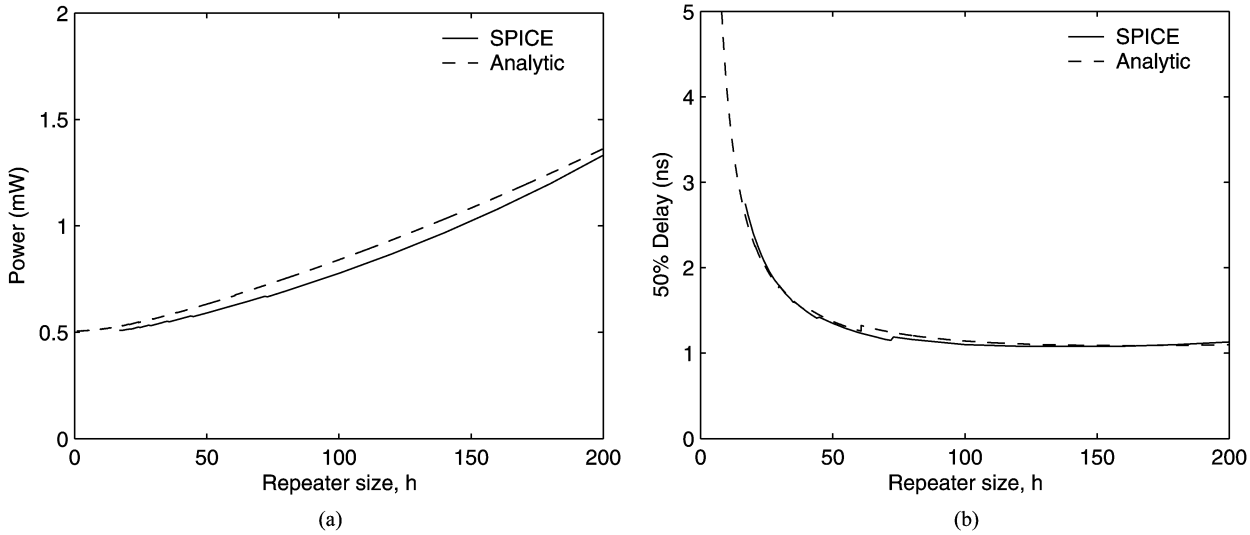


Fig. 10. Power dissipation and 50% delay at the edge of the design space with bandwidth constraint. $B_{\rm req} = 1\ {\rm Gb/s}$, $R = 0.31\ \Omega/\mu{\rm m}$, $C = 0.223\ {\rm fF}/\mu{\rm m}$, and $l = 10$ mm. (a) Power dissipation. (b) 50% delay.

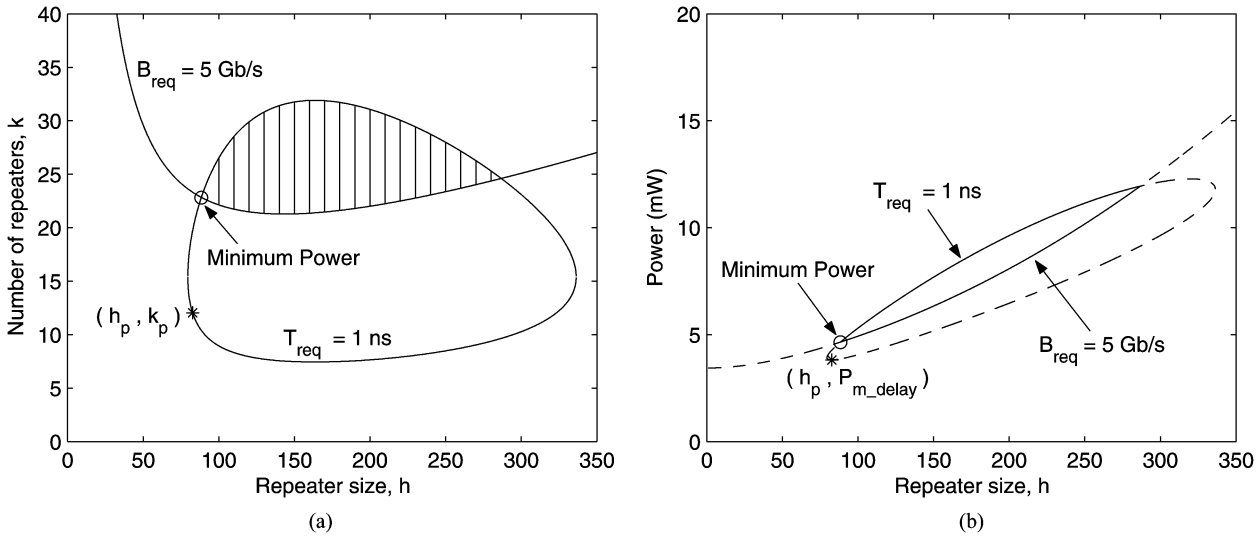


Fig. 11. Design space and power dissipation at the edge of the design space with both delay and bandwidth constraints. (a) Design space. (b) Power dissipation.

In order for k to be a positive real number, τ_1 should be negative. An upper limit, therefore, is placed on the bandwidth by the process technology

$$B_{\rm req} \le \frac{1}{5.5 R_{r0} C_0}. \tag{34}$$

Similar to the delay-constraint case, the minimum power with a bandwidth constraint can only be reached at the edge of the design space. P_s in (20) can be rewritten as

$$P_s = \frac{4\alpha_s f I_{d0}^2 t_r^2 V_{\rm dd} kh}{0.75 V_{\rm dsat} G\left(C_0 + \frac{C_t}{kh}\right) + 2 H I_{d0} t_r}. \tag{35}$$

For a fixed t_r, P_s increases monotonically with increasing kh. This relationship is also valid for P_d and P_l. At the edge of the design space, $t_r = 1/2B_{\rm req}$; therefore, kh can be obtained from (31)

$$kh = \frac{\sqrt{(\tau_2 h)^2 - 4.4\tau_1 R_t C_t h^2} + \tau_2 h}{-2\tau_1}. \tag{36}$$

From (36), kh increases monotonically with h (note that τ_1 is negative). The total power at the edge of the design space, therefore, increases monotonically with increasing h, as shown in Fig. 10(a). The minimum power satisfying the bandwidth constraint can be achieved with minimum-sized repeaters. For minimum-sized repeaters, the corresponding k and total delay, however, are unpractically large as shown in Figs. 9 and 10. In order to produce an effective repeater system, the delay and area constraints should also be considered.

E. Power Dissipation With Both Delay and Bandwidth Constraints

The design space under both delay and bandwidth constraints is the intersection of the design spaces described in Sections II-C and II-D, as shown in Fig. 11(a). The minimum power is also achieved at the edge of the design space. As described in Section II-C, the minimum power satisfying the delay constraint occurs at (h_p, k_p). If these design parameters satisfy the bandwidth requirement, (h_p, k_p) is the optimal design point for minimizing power while satisfying both the delay and bandwidth

constraints. If (h_p, k_p) cannot satisfy the bandwidth requirement, the minimum power occurs at the left intersection of the two design space edges, as shown in Fig. 11(a) and (b). The coordinates of the intersection are obtained by solving (22) and (30). If no intersection exists between the two design spaces, the two constraints cannot be simultaneously satisfied, and one or both of the constraints have to be released. Other constraints, such as the number and size of the repeaters, can be similarly handled.

III. Effects of Inductance on the Repeater Insertion Methodology

For wide global interconnects, the inductance is not negligible and has to be considered in repeater design methodologies. In Section III-A, a timing model of an *RLC* interconnect is reviewed. In Section III-B, the effects of inductance on the repeater design space are analyzed. The minimum power consumption while satisfying delay and bandwidth constraints is described in Section III-C.

A. Timing Model of RLC Interconnect

In [2], a variable ζ is introduced to characterize the effects of inductance. By including the repeater output capacitance, ζ becomes

$$\zeta = \frac{Rl}{2k}\sqrt{\frac{C}{L}} \cdot \frac{R_T C_T \left(1 + \frac{C_{d0}}{C_{g0}}\right) + C_T + R_T + 0.5}{\sqrt{1 + C_T}} \quad (37)$$

where $R_T = kR_{\mathrm{tr}0}/(hRl)$ and $C_T = hkC_{g0}/(Cl)$. The corresponding ζ with R_{d0} and R_{r0} is denoted as ζ_d and ζ_r, respectively. The delay model of an *RLC* interconnect is an extension of the result from [2] where the repeater output capacitance and input slew effects are included. The delay of a single stage interconnect for a step input can be obtained by curve fitting

$$t_{\mathrm{ds}} = \frac{e^{-2.3\zeta_d^{1.5}} + 1.48\zeta_d}{w_n} \quad (38)$$

where $w_n = k/\sqrt{Ll(Cl + C_{g0}hk)}$. The coefficients in (38) are slightly different from those in [2] due to the effects of the repeater output capacitance. In [22], an accurate estimate of the rise time in an *RLC* interconnect is also obtained by curve fitting. The expressions, however, are analytically complicated. In this paper, a simplified piecewise approximation of the rise time is used

$$t_r = \frac{t_{90\%} - t_{10\%}}{0.8} = \begin{cases} \dfrac{4.4\zeta_r - 1.8}{0.8 w_n}, & \zeta_r > 0.41 \\ 0, & \text{otherwise.} \end{cases} \quad (39)$$

When $\zeta_r < 0.5$, the interconnect is highly inductance dominant, and (39) can introduce a large error. In Fig. 12, ζ_r is plotted for different repeater sizes and interconnect lengths. The driver size is normalized to the size of a minimum inverter. The size of the load gate is the same as the driver. $W_{\min} = 0.18\ \mu$m is the minimum global wire width specified in the ITRS [8]. The

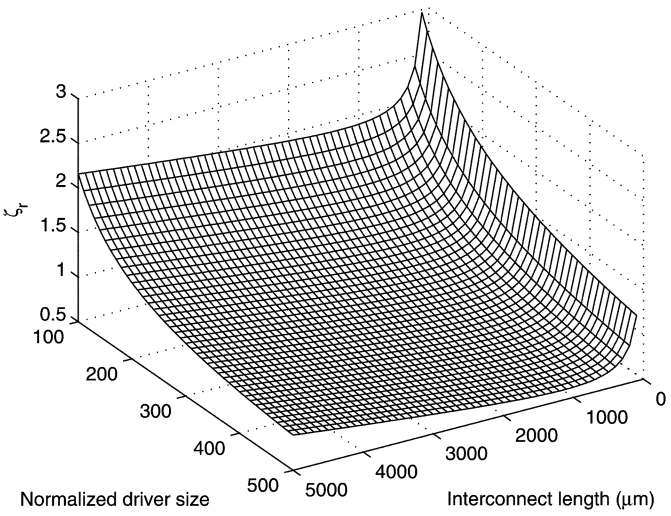


Fig. 12. Inductance effect for different driver sizes and interconnect lengths. $W = 20W_{\min}$ and $L = 1\ \mathrm{pH}/\mu\mathrm{m}$.

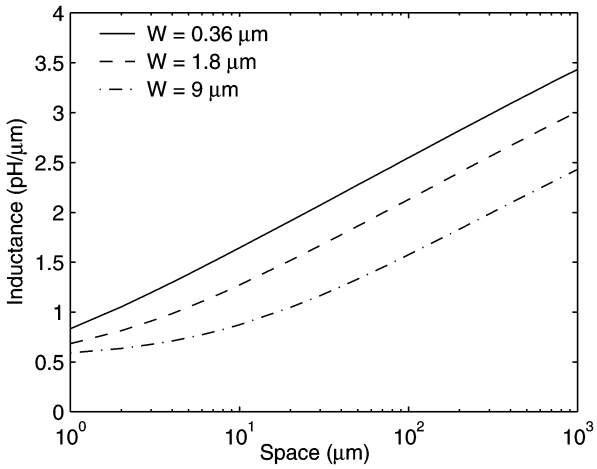


Fig. 13. Inductance values with difference current return paths.

space between adjacent interconnects is assumed equal to the interconnect width. As shown in Fig. 12, inductance effects become more significant with larger drivers. Note that for a fixed driver size, a minimum ζ_r can be achieved in this example when the interconnect length is approximately 1 mm. When the wire length is too short or too long, the interconnect is dominated either by the repeater resistance or the wire resistance, respectively. In Fig. 13, the inductance per unit length is plotted as a function of the space between the signal line and the current return path. The wire thickness is 0.4 μm. Three wire widths are examined, 0.36, 1.8, and 9 μm. The width of the reference line for the current return path is assumed to be the same as the signal line width. The inductance values are obtained with FastHenry [23] for a wire length of 10 mm. As shown in Fig. 13, the interconnect inductance increases slowly with increasing space between the signal line and the current return path. With the same line space, wider wires exhibit smaller inductance. When the return paths are within 10 μm, the inductance ranges from 0.5 to 1.5 pH/μm.

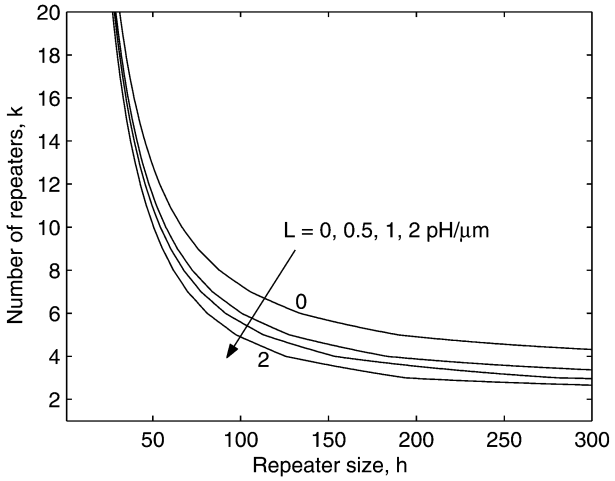


Fig. 14. Effects of inductance on the repeater design space satisfying bandwidth constraints. $B_{\rm req} = 2$ Gb/s, $l = 10$ mm, and $W = 10W_{\rm min}$.

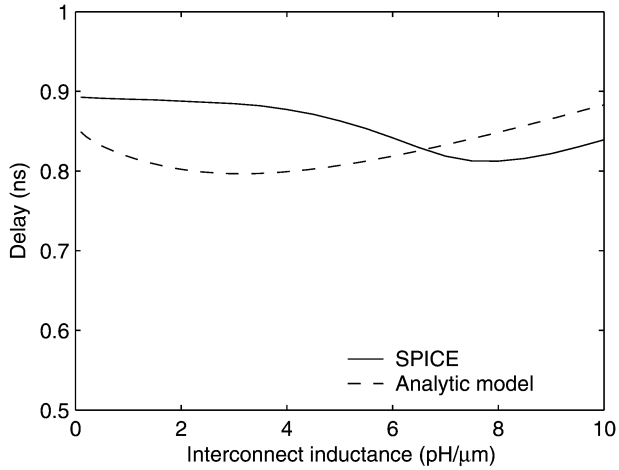


Fig. 15. Effects of inductance on the interconnect delay with repeaters. $l = 10$ mm, $k = 10$, $h = 100$, and $W = 10W_{\rm min}$.

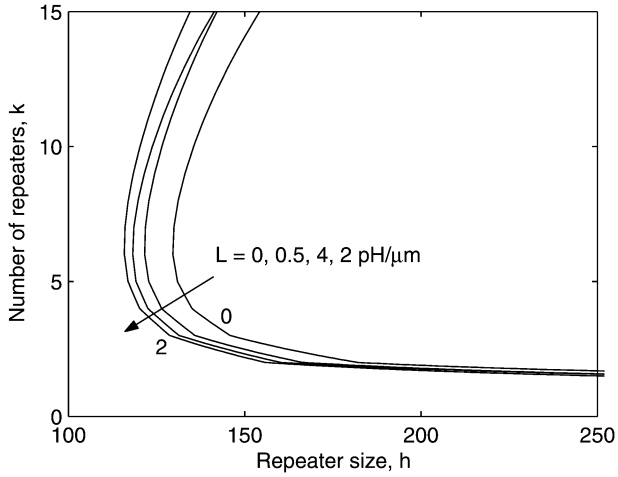


Fig. 16. Effects of inductance on the repeater design space satisfying delay constraints. $T_{\rm req} = 700$ ps, $l = 10$ mm, and $W = 10W_{\rm min}$.

B. Effects of Inductance on the Repeater Design Space

By including interconnect inductance, both the delay and signal transition time of an interconnect are affected. The repeater design space satisfying delay or bandwidth constraints is also changed, which is described in Sections III-B1 and III-B2, respectively.

1) Bandwidth Constraints: The signal transition time at the far end of an *RLC* interconnect decreases with increasing inductance effects [7]. The inductance, therefore, increases the bandwidth of an interconnect. The repeater design space satisfying a bandwidth constraint is plotted in Fig. 14 for different values of inductance. With increasing inductance, the number and size of the repeaters can be reduced while maintaining the same signal transition time.

2) Delay Constraints: The delay of an interconnect with repeaters can be affected by inductance in three ways. First, the propagation delay along the interconnect can increase with increasing inductance [24]. Second, the inductance reduces the signal transition time, decreasing the gate delay due to the input slew effect. Third, due to the inductive shielding effect (described by El-Moursy and Friedman in [24]), both the effective capacitance seen by the driver and the equivalent output resistance of the driver are reduced. The gate delay is, therefore, further reduced. (Since the delay model used in this paper is based on curve fitting, and a constant driver resistance is assumed, the third inductance effect is not considered in this model).

As presented above, the interconnect inductance has competing effects on the total delay. The total delay of an interconnect with repeaters is plotted in Fig. 15. As shown in Fig. 15, with increasing line inductance, the total delay decreases until a minimum delay is achieved. The analytic model overestimates the inductance effects when the inductance is low; however, the trend of the inductance effect is captured. In Fig. 16, the repeater design space satisfying a delay constraint is plotted for different values of inductance. Only the portion of the design space with fewer and smaller repeaters is of interest. As shown in Fig. 16, the design space first expands and then shrinks with increasing inductance. Larger inductance does not necessarily result in fewer and smaller repeaters. When the inductance changes from 2 pH/μm (the left curve in Fig. 16) to 4 pH/μm (the curve second to the left in Fig. 16), the number and/or size of the repeaters should be increased to satisfy the same delay constraint.

C. Power Dissipation With Delay and Bandwidth Constraints

The inductance affects the minimum power with delay and bandwidth constraints in two ways. First, the design space is changed as discussed in Section III-B. Second, the short-circuit power consumed by the repeaters may also be affected by the inductance for a fixed interconnect configuration. As presented in Section III-B, the inductance can produce faster signal transition times, reducing the time during which the short-circuit current can flow [7]. The inductance also shields part of the far end capacitance [24], resulting in a smaller effective load capacitance and increasing the peak short-circuit current.

Similar to an *RC* line, a distributed *RLC* interconnect with a capacitive load can be represented by a π model [25]. The effective capacitance of the π model is

$$C_{\rm eff} = C_n + C_f\left[1 - \frac{4R_\pi C_f}{t_r} + \frac{8k_3}{t_r^2 s_1}(e^{(s_1 t_r/2)} - 1) + \frac{8k_4}{t_r^2 s_2}(e^{(s_2 t_r/2)} - 1)\right] \quad (40)$$

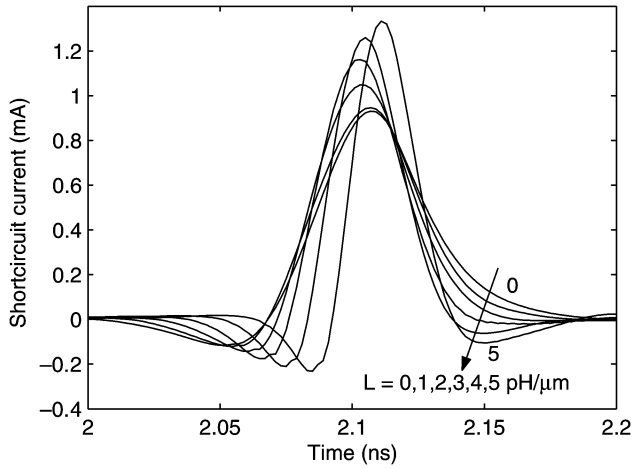


Fig. 17. Effects of inductance on short-circuit current in repeaters. $l = 10$ mm, $k = 10$, $h = 150$, and $W = 10W_{\min}$.

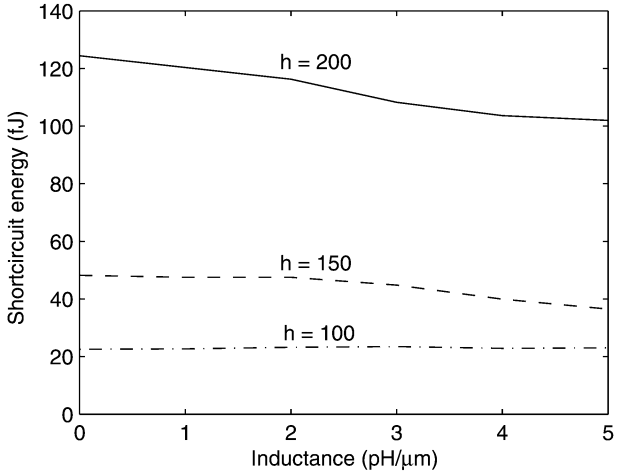


Fig. 18. Effects of inductance on the short-circuit power in repeaters. $l = 10$ mm, $k = 10$, and $W = 10W_{\min}$.

where

$$s_{1,2} = \frac{-R_\pi \pm \sqrt{R_\pi^2 - \frac{4L_\pi}{C_f}}}{2L_\pi} \tag{41}$$

$$k_3 = \frac{1}{s_1^2(s_1 - s_2)L_\pi C_f} \tag{42}$$

$$k_4 = \frac{1}{s_2^2(s_2 - s_1)L_\pi C_f}. \tag{43}$$

In Fig. 17, the short-circuit current of a repeater in an interconnect system is illustrated for different inductance values. The short-circuit energy consumed in one signal transition is depicted in Fig. 18. When $h = 100$, the effect of the inductance on the transition time cancels the inductive shielding effect on the load, making the short-circuit power less sensitive to inductance. This result shows that the common assumption that inductance can reduce short-circuit power is not always true. Actually, the short-circuit energy increases slightly with increasing inductance until a maximum energy is achieved. With a larger repeater size, the effect of inductance on the transition time increases and starts to dominate the inductive shielding effect on the load for large inductances, decreasing the short-circuit power. For $h = 150$, the short-circuit energy is almost constant when $L < 2\ \mathrm{pH}/\mu\mathrm{m}$, however, both the period and peak value

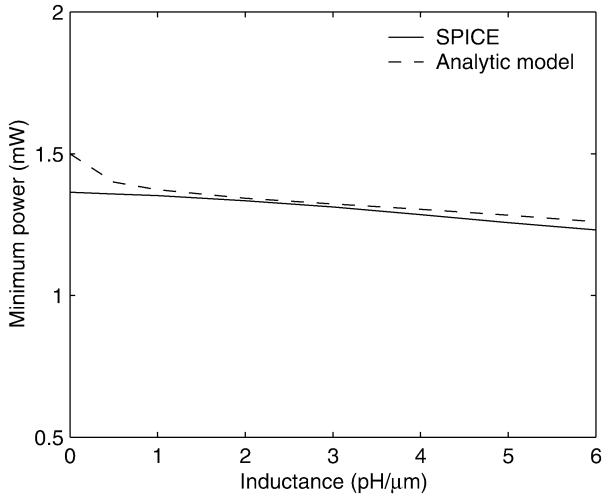


Fig. 19. Effects of inductance on the minimum interconnect power while satisfying a delay constraint. $l = 15$ mm, $W = 10W_{\min}$, and $T_{\mathrm{req}} = 1$ ns.

of the short-circuit current vary over this range of inductance, as shown in Fig. 17. When $h = 200$, the effect of inductance on the transition time dominates the shielding effect for any value of inductance. For very large repeaters, the short-circuit power always decreases with increasing inductance.

As described in Section II, the minimum power of an *RC* interconnect with repeaters can be achieved at the edge of the design space. For practical *RLC* interconnect structures, this behavior is also valid. Given a design space, the minimum power can be solved numerically by applying the Lagrange method. In Fig. 19, the minimum achievable power of an interconnect with inserted repeaters while satisfying a delay constraint is plotted for different values of inductance. The clock frequency is 1 GHz. As shown in Fig. 19, by including inductance, the minimum interconnect power under a delay constraint is slightly reduced. This reduction is partially due to the extension of the design space (for low values of inductance) and partially due to the reduction in short-circuit power (for large values of inductance).

As described in Section II, the minimum power of an *RC* interconnect with bandwidth constraints can be achieved by using the minimum-sized repeater in the design space. This statement, however, is not correct for *RLC* interconnect. The optimal k for an *RLC* line to achieve the minimum power is normally unpractically large. In Fig. 20, the minimum achievable power of an *RLC* interconnect satisfying a bandwidth constraint is plotted for different values of inductance. In this example, k is limited to 10. As shown in Fig. 20, the inductance reduces the minimum power under a bandwidth constraint. Note in Figs. 19 and 20 that the analytic model overestimates the inductance effect for small values of inductance. The error of the analytic method is less than 10% in Fig. 19 and less than 6% in Fig. 20.

IV. Conclusion

In this paper, a repeater insertion design methodology is presented to achieve the minimum power with delay and bandwidth constraints. Input slew effects are considered in the delay model. The minimum power is achieved at the edge of the design space. Closed-form solutions for the minimum power in an *RC* interconnect are developed with delay constraints, where

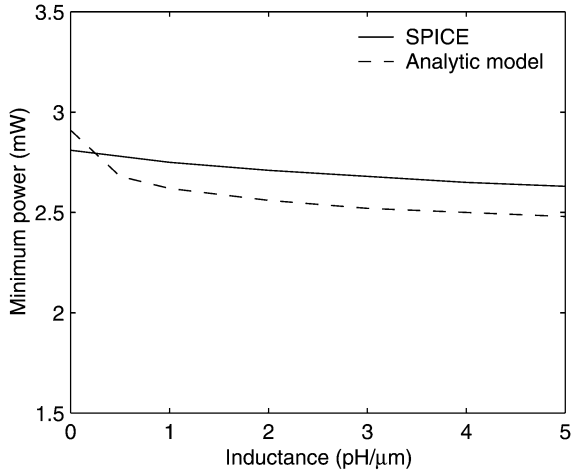


Fig. 20. Effects of inductance on the minimum interconnect power while satisfying a bandwidth constraint. $l = 15$ mm, $W = 10W_{\min}$, and $B_{\rm req} = 2$ Gb/s.

the average error of the model is 7% as compared with SPICE simulations. Satisfying a bandwidth constraint, the minimum power dissipated in an *RC* interconnect can be achieved with minimum-sized repeaters. The effects of inductance on the repeater insertion methodology are also analyzed. It is shown that the effect of inductance on the interconnect delay (including the delay of the repeaters) and on the short-circuit power is nonmonotonic. The overall effects of inductance reduce the minimum achievable power under a delay or bandwidth constraint.

Appendix
Minimizing $P_{\rm total}$ With a Delay Constraint for *RC* Interconnect

Since both P_d and P_l linearly depend on kh, the problem of minimizing $P_d + P_l$ can be formulated as: minimizing function $X(h,k) = kh$ subject to the constraint $T_{\rm total}(h,k) \le T_{\rm req}$. As described in Section II, the minimum $P_d + P_l$ can only be achieved at the edge of the design space. The constraint $T_{\rm total} \le T_{\rm req}$, therefore, can be further simplified as $T_{\rm total}(h,k) - T_{\rm req} = 0$. From the Lagrange method [26], the solution should satisfy the following two equations:

$$\frac{\partial[X + \lambda(T_{\rm total} - T_{\rm req})]}{\partial h} = 0 \tag{44}$$

$$\frac{\partial[X + \lambda(T_{\rm total} - T_{\rm req})]}{\partial k} = 0 \tag{45}$$

where λ is called the Lagrange multiplier. From (5), (44) and (45) are rewritten as

$$k + \lambda\left(a_2 R_t C_{g0} - \frac{a_2 R_0 C_t}{h^2}\right) = 0 \tag{46}$$

$$h + \lambda\left(a_2 R_0 C_0 - \frac{a_1 R_t C_t}{k^2}\right) = 0. \tag{47}$$

Similar to the approach in [5], eliminating λ from (46) and (47) results in

$$a_2 R_0 C_0 k + \frac{a_2 R_0 C_t}{h} = a_2 R_t C_{g0} h + \frac{a_1 R_t C_t}{k}. \tag{48}$$

From the constraint expression (22), it can be observed that both sides of (48) are equal to $T_{\rm req}/2$

$$a_2 R_0 C_0 k + \frac{a_2 R_0 C_t}{h} = \frac{T_{\rm req}}{2} \tag{49}$$

$$a_2 R_t C_{g0} h + \frac{a_1 R_t C_t}{k} = \frac{T_{\rm req}}{2}. \tag{50}$$

Solving the above two expressions, (24)–(26) can be obtained.

The curve of $P_d + P_l$ around the power-optimal point is approximated as a part of an ellipse

$$\frac{(h - h_0)^2}{(h_1 - h_0)^2} + \frac{(P_d + P_l - P_0)^2}{(P_1 - P_0)^2} = 1 \tag{51}$$

where h_1, P_0, and P_1 are defined in Section II. From (51), $P_d + P_l$ can be determined as

$$P_d + P_l = P_1 + \frac{(P_0 - P_1)\sqrt{(h_1 - h_0)^2 - (h - h_0)^2}}{h_0 - h_1}. \tag{52}$$

kh achieves the minimum value at h_0, therefore, $(d(kh)/dh)|_{h_0} = 0$. By utilizing this result, the derivative $x_0 = (dP_s/dh)|_{h_0}$ can be obtained as shown in (28). The short-circuit power around the power-optimal point is approximated as

$$P_s = P_s(h_0) + x_0(h - h_0). \tag{53}$$

From (52) and (53), the derivative of $P_{\rm total}$ can be determined as

$$\frac{dP_{\rm total}}{dh} = x_0 - \frac{(h - h_0)(P_0 - P_1)}{(h_0 - h_1)\sqrt{(h_1 - h_0)^2 - (h - h_0)^2}}. \tag{54}$$

Setting (54) to zero, the power optimal solution (27)–(29) can be obtained.

References

[1] H. B. Bakoglu and J. D. Meindl, "Optimal interconnection circuits for VLSI," *IEEE Trans. Electron Devices*, vol. ED-32, no. 5, pp. 903–909, May 1985.

[2] Y. I. Ismail and E. G. Friedman, "Effects of inductance on the propagation delay and repeater insertion in VLSI circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 8, no. 2, pp. 195–206, Apr. 2000.

[3] P. Kapur, G. Chandra, and K. C. Saraswat, "Power estimation in global interconnects and its reduction using a novel repeater optimization methodology," in *Proc. ACM/IEEE Des. Autom. Conf.*, Jun. 2002, pp. 461–466.

[4] V. Adler and E. G. Friedman, "Repeater design to reduce delay and power in resistive interconnect," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 45, no. 5, pp. 607–616, May 1998.

[5] A. Nalamalpu and W. Burleson, "A practical approach to DSM repeater insertion: Satisfying delay constraints while minimizing area and power," in *Proc. IEEE ASIC/SOC Conf.*, Sep. 2001, pp. 152–156.

[6] A. Nalamalpu, S. Srinivasan, and W. P. Burleson, "Boosters for driving long onchip interconnects—Design issues, interconnect synthesis, and comparison with repeaters," *IEEE Trans. Comput.-Aided Des.*, vol. 21, no. 1, pp. 50–62, Jan. 2002.

[7] Y. Ismail, E. G. Friedman, and J. L. Neves, "Exploiting the on-chip inductance in high-speed clock distribution networks," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 9, no. 12, pp. 963–973, Dec. 2001.

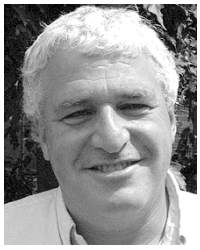
[8] *The International Technology Roadmap for Semiconductors*, 2003.

[9] K. Banerjee and A. Mehrotra, "A power-optimal repeater insertion methodology for global interconnects in nanometer designs," *IEEE Trans. Electron Devices*, vol. 49, no. 11, pp. 2001–2007, Nov. 2002.

[10] G. Chen and E. G. Friedman, "Low power repeaters driving *RC* interconnect with delay and bandwidth constraints," in *Proc. IEEE Int. SOC Conf.*, Sep. 2004, pp. 335–339.
[11] ——, "Low power repeaters driving *RLC* interconnect with delay and bandwidth constraints," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2005, pp. 596–599.
[12] Berkeley Predictive Technology Model [Online]. Available: http://www-device.eecs.berkeley.edu/~ptm
[13] Y. Cao *et al.*, "New paradigm of predictive MOSFET and interconnect modeling for early circuit design," in *Proc. IEEE Custom Integr. Circuits Conf.*, May 2000, pp. 201–204.
[14] T. Sakurai and A. R. Newton, "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas," *IEEE J. Solid-State Circuits*, vol. 25, no. 2, pp. 584–594, Apr. 1990.
[15] T. Sakurai, "Closed-form expressions for interconnection delay, coupling, and crosstalk in VLSI's," *IEEE Trans. Electron Devices*, vol. 40, no. 1, pp. 118–124, Jan. 1993.
[16] S. O. Nakagawa *et al.*, "On-chip crosstalk noise model for deep-submicrometer ULSI interconnect," *Hewlett-Packard J.*, pp. 39–45, Aug. 1998.
[17] H. J. M. Veendrick, "Short-circuit dissipation of static CMOS circuitry and its impact on the design of buffer circuits," *IEEE J. Solid-State Circuits*, vol. SC-19, no. 4, pp. 468–473, Aug. 1984.
[18] K. Nose and T. Sakurai, "Analysis and future trend of short-circuit power," *IEEE Trans. Comput.-Aided Des.*, vol. 19, no. 9, pp. 1023–1030, Sep. 2000.
[19] P. R. O'Brien and T. L. Savarino, "Modeling the driving-point characteristic of resistive interconnect for accurate delay estimation," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Des.*, Apr. 1989, pp. 512–515.
[20] J. Qian, S. Pullela, and L. Pillage, "Modeling the effective capacitance for the *RC* interconnect of CMOS gates," *IEEE Trans. Comput.-Aided Des.*, vol. 13, no. 12, pp. 1526–1535, Dec. 1994.
[21] A. Ferré and J. Figueras, "Leakage power bounds in CMOS digital technologies," *IEEE Trans. Comput.-Aided Des.*, vol. 21, no. 6, pp. 731–738, Jun. 2002.
[22] N. H. Mahmoud and Y. I. Ismail, "Accurate rise time and overshoots estimation in *RLC* interconnects," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2003, pp. 477–480.
[23] M. Kamon, M. J. Tsuk, and J. White, "FastHenry: A multipole accelerated 3-D inductance extraction program," *IEEE Trans. Microw. Theory Tech.*, vol. 42, no. 9, pp. 1750–1758, Sep. 1994.
[24] M. A. El-Moursy and E. G. Friedman, "Shielding effect of on-chip interconnect inductance," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 3, pp. 396–400, Mar. 2005.
[25] X. Yang *et al.*, "Hurwitz stable reduced order modeling for *RLC* interconnect trees," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Des.*, Nov. 2000, pp. 222–228.
[26] Language Multiplier [Online]. Available: http://mathworld.wolfram.com/LagrangeMultiplier.html

Guoqing Chen received the B.S. (with honors) and M.S. degrees in electronic engineering from Tsinghua University, Beijing, China, in 1998 and 2001, respectively. He is working toward the Ph.D. degree in the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY.

His current research interests are in the areas of high-speed interconnect modeling, signal integrity, on-chip optical interconnect, and other design issues in high-performance ICs.



Eby G. Friedman (S'78–M'79–SM'90–F'00) received the B.S. degree from Lafayette College, Easton, PA, in 1979, and the M.S. and Ph.D. degrees from the University of California, Irvine, in 1981 and 1989, respectively, all in electrical engineering.

He is the author of more than 300 papers and book chapters, several patents, and the author or editor of seven books in the fields of high-speed and low-power CMOS design techniques, high-speed interconnect, and the theory and application of synchronous clock and power distribution networks.

Dr. Friedman is a Fullbright Scholar. He is the Regional Editor of the *Journal of Circuits, Systems and Computers*, a member of the editorial boards of *Analog Integrated Circuits and Signal Processing, Microelectronics Journal*, and *Journal of VLSI Signal Processing*, Chair of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS steering committee, and a member of the technical program committee of a number of conferences. He previously was the Editor-in-Chief of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, a member of the editorial board of the PROCEEDINGS OF THE IEEE and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: ANALOG AND DIGITAL SIGNAL PROCESSING, a member of the Circuits and Systems (CAS) Society Board of Governors, CAS liaison to the Solid-State Circuits Society, Chair of the VLSI Systems and Applications CAS Technical Committee, Chair of the Electron Devices Chapter of the IEEE Rochester Section, Program and Technical chair of several IEEE conferences, and Guest Editor of several special issues in a variety of journals. He was a recipient of the Howard Hughes Master's and Doctoral Fellowships, an IBM University Research Award, an Outstanding IEEE Chapter Chairman Award, a University of Rochester College of Engineering Teaching Excellence Award, and the University of Rochester Graduate Teaching Award.