

## REFERENCES

- [1] P. Larsson and C. Svensson, "Noise in digital dynamic CMOS circuits," *IEEE J. Solid-State Circuits*, vol. 29, no. 6, pp. 655–662, Jun. 1994.
- [2] K. L. Shepard and V. Narayanan, "Noise in deep submicron digital design," in *Proc. ICCAD*, 1996, pp. 524–531.
- [3] A. Devgan, "Efficient coupled noise estimation for on-chip interconnects," in *Proc. ICCAD*, 1997, pp. 147–151.
- [4] S. H. Choi, B. C. Paul, and K. Roy, "Dynamic noise with capacitive and inductive coupling," in *Proc. Asia-South Pac. Des. Autom. Conf. VLSI*, 2002, pp. 65–65.
- [5] K. C. Saraswat, "Effects of scaling of interconnects on the time delay of VLSI circuits," *IEEE J. Solid-State Circuits*, vol. SC-17, no. 2, pp. 275–280, Apr. 1982.
- [6] N. D. Arora, K. V. Raol, R. Schumann, and L. M. Richardson, "Modeling and extraction of interconnect capacitance for multilayer VLSI circuits," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 15, no. 1, pp. 58–67, Jan. 1996.
- [7] E. Barke, "Line-to-ground capacitance calculation for VLSI: A comparison," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 7, no. 2, pp. 295–298, Feb. 1988.
- [8] J. H. Chern, J. Huang, L. Arledge, P. C. Li, and P. Yang, "Multi-level metal capacitance models for CAD design synthesis systems," *IEEE Electron Device Lett.*, vol. 13, no. 1, pp. 32–34, Jan. 1992.
- [9] T. Sakurai and K. Tamaru, "Simple formulas for two- and three-dimensional capacitances," *IEEE Trans. Electron Devices*, vol. ED-30, no. 2, pp. 183–185, Feb. 1983.
- [10] R. Kumar, "Interconnect and noise immunity design for the Pentium 4 processor," *Intel Tech. J.*, Jan. 2001.
- [11] A. B. Kahng, S. Muddu, E. Sarto, and R. Sharma, "Interconnect tuning strategies for high-performance ICs," in *Proc. Des. Autom. Test Eur. (DATE) Timing Crosstalk Interconnect Session*, 1998, pp. 471–478.
- [12] D. Sylvester, C. Hu, O. S. Nakagawa, and S. Y. Oh, "Interconnect scaling: Signal integrity and performance in future high-speed CMOS designs," in *Proc. Symp. VLSI Technol.*, 1998, pp. 42–43.
- [13] M. H. Chowdhury, Y. I. Ismail, C. V. Kashyap, and B. L. Krauter, "Performance analysis of deep sub micron VLSI circuits in the presence of self and mutual inductance," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS) Low-Noise Circuits Interconnect Issues*, 2002, pp. 197–200.
- [14] T. Sakurai and A. R. Newton, "Alpha-power law MOSFET model and its application to CMOS inverter delay and other formulas," *IEEE J. Solid-State Circuits*, vol. 25, no. 2, pp. 584–594, Apr. 1990.

## Crosstalk Modeling for Coupled *RLC* Interconnects With Application to Shield Insertion

Junmou Zhang and Eby G. Friedman

**Abstract**—On-chip interconnect delay and crosstalk noise have become significant bottlenecks in the performance and signal integrity of deep submicrometer VLSI circuits. A crosstalk noise model for both identical and nonidentical coupled resistance–inductance–capacitance (*RLC*) interconnects is developed based on a decoupling technique exhibiting an average error of 6.8% as compared to SPICE. The crosstalk noise model, together with a proposed concept of effective mutual inductance, is applied to evaluate the effectiveness of the shielding technique.

**Index Terms**—Capacitive coupling, crosstalk analysis, decoupling technique, inductive coupling, resistance–inductance–capacitance (*RLC*) interconnect, shield insertion.

### I. INTRODUCTION

It is well accepted that on-chip interconnect plays an important role in the performance and signal integrity of deep submicrometer VLSI circuits. With faster rise times and lower resistance, long wide wires in the upper metal layers exhibit significant inductive effects. An efficient resistance–inductance–capacitance (*RLC*) model of the on-chip interconnect is therefore critical in high-level design, logic synthesis, and physical design.

A closed-form expression for the crosstalk noise between two identical *RLC* lines is developed in [1], assuming that the two interconnects are loosely coupled ( $(L_m/L)(C_c/C) < 0.1$ ). In [2], a time domain expression for the output of two coupled *RLC* interconnects is developed without explicitly requiring the Laplace transform of the transfer function. Delay and crosstalk noise expressions, however, ignore the effect of the capacitive load at the receiver end, and the peak crosstalk noise is assumed to occur at the time of flight  $t_f$ . In [3], the crosstalk noise model includes the effect of orthogonal lines above and below the interconnects. In [4], a technique to decouple coupled *RLC* interconnects into independent interconnects is developed based on a modal analysis. This decoupling method, however, assumes a TEM mode approximation ( $LC = (1/\mu\epsilon)$ ), which is only valid in a two-dimensional (2-D) structure with a perfect current return path in the ground plane directly beneath the conductors [5]. (Although a modal decomposition which is not based on a TEM approximation is possible for two coupled interconnects.)

An estimate of crosstalk noise among multiple *RLC* interconnects is required to efficiently implement shielding techniques. Shield insertion is an effective method to reduce crosstalk noise and signal delay uncertainty, and has become common practice when routing critical signal and power lines [6]. Inserting shield lines can greatly reduce both capacitive coupling [7] and mutual inductive coupling by providing a closer current return path for both the aggressor and victim

Manuscript received December 30, 2004; revised June 6, 2005. This work was supported in part by the Semiconductor Research Corporation under Contract 2003-TJ-1068 and 2004-TJ-1207, by the National Science Foundation (NSF) under Contract CCR-0304574, by the Fulbright Program under Grant 87481764, by a grant from the New York State Office of Science, Technology and Academic Research to the Center for the CAT in Electronic Imaging Systems, and by grants from Xerox Corporation, IBM Corporation, Intel Corporation, Lucent Technologies Corporation, Eastman Kodak Company, and Manhattan Routing.

The authors are with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY 14627 USA (e-mail: juzhang@ece.rochester.edu).

Digital Object Identifier 10.1109/TVLSI.2006.878223

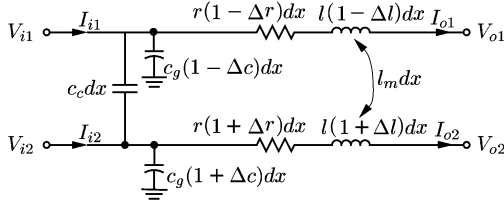


Fig. 1. Infinitesimally small segment of two coupled *RLC* interconnects.

lines. Far reaching inductive coupling, however, cannot be completely eliminated, and can produce substantial crosstalk noise on a quiescent victim line. An efficient estimate of the crosstalk noise between coupled interconnects including the effects of shield insertion is therefore critical during the routing and verification phase to guarantee signal integrity. Guidelines are therefore required to determine when a shield line should be inserted and whether a one-sided shield or two-sided shield is appropriate.

An *ABCD* matrix is often used to characterize a single transmission line since segments can be conveniently cascaded [8]. The convenience of the *ABCD* matrix remains for two or more coupled interconnects. Compared with the modal analysis described in [4], the *ABCD* matrix does not require a TEM approximation. Based on the *ABCD* parameter matrix, a decoupling technique for both identical and nonidentical coupled *RLC* interconnects is developed in Section II. With this decoupling technique, an accurate crosstalk noise model for two coupled interconnects is developed in Section III. In Section IV, the crosstalk noise model, together with a proposed effective mutual inductance model, is used to evaluate the effectiveness of the shield insertion process on reducing crosstalk noise in the presence of capacitive and inductive coupling. Some conclusions are offered in Section V.

## II. DECOUPLING TECHNIQUE

Two-coupled *RLC* interconnects with a coupled capacitance per unit length  $c_c$ , mutual inductance  $l_m$ , resistance  $r(1 + \Delta r)$  and  $r(1 - \Delta r)$ , self-inductance  $l(1 + \Delta l)$  and  $l(1 - \Delta l)$ , and ground capacitances  $c_g(1 + \Delta c)$  and  $c_g(1 - \Delta c)$ , respectively, are shown in Fig. 1. The *ABCD* matrix  $E$ , for an infinitesimally small segment of these two coupled interconnects, can be obtained, as shown in (1) at the bottom of the page. Furthermore, the matrix  $E$  can be diagonalized as

$$E = W\Lambda W^{-1} \quad (2)$$

where

$$\Lambda = \begin{bmatrix} (1 - \theta_1 dx) & 0 & 0 & 0 \\ 0 & (1 + \theta_1 dx) & 0 & 0 \\ 0 & 0 & (1 - \theta_2 dx) & 0 \\ 0 & 0 & 0 & (1 + \theta_2 dx) \end{bmatrix} \quad (3)$$

$$W = \frac{1}{2} \begin{bmatrix} -Z_{o1} & Z_{o1} & Z_{o2} & -Z_{o2} \\ -Z_{o1} & Z_{o1} & -Z_{o2} & Z_{o2} \\ 1 & 1 & -1 & -1 \\ 1 & 1 & 1 & 1 \end{bmatrix}. \quad (4)$$

In general,  $\theta_1$  and  $\theta_2$  are functions of the interconnect impedance parameters (resistances, capacitance, and inductances) and are difficult to solve analytically. If nonidentical coupled interconnects are part of a bus structure with the same width, height, and length, the resistance of the two nonidentical interconnects are equal, i.e.,  $\Delta r = 0$ . Under the condition of  $\Delta r = 0$ , and a moment matching approximation  $\theta_1$ ,  $\theta_2$ ,  $Z_{o1}$ , and  $Z_{o2}$  can be approximated as

$$\theta_1 = \sqrt{sC'_g(r + s(l' + l'_m))} \quad (5)$$

$$\theta_2 = \sqrt{s(C'_g + 2C'_c)(r + s(l' - l'_m))} \quad (6)$$

$$Z_{o1} = \sqrt{\frac{(r + s(l' + l'_m))}{sC'_g}} \quad (7)$$

$$Z_{o2} = \sqrt{\frac{(r + s(l' - l'_m))}{s(C'_g + 2C'_c)}} \quad (8)$$

where  $c'_g$ ,  $c'_c$ ,  $l'$ , and  $l'_m$  are

$$c'_g = c_g \left( 1 + \frac{c_c}{c_g} - \sqrt{\frac{c_c^2}{c_g^2} + \Delta c^2} \right) \quad (9)$$

$$c'_c = c_c \sqrt{\left( 1 + \frac{c_g^2}{c_c^2} \Delta c^2 \right)} \quad (10)$$

$$l' = l \quad (11)$$

$$l'_m = l_m \frac{c_c}{\sqrt{c_c^2 + c_g^2 \Delta c^2}} - l \frac{c_g \Delta c \Delta l}{\sqrt{c_c^2 + c_g^2 \Delta c^2}}. \quad (12)$$

The physical meaning of  $\theta_1$  ( $Z_{o1}$ ) is the propagation constant (characteristic impedance) of coupled interconnects when both inputs switch in the same direction. The physical meaning of  $\theta_2$  ( $Z_{o2}$ ) is the propagation constant (characteristic impedance) of coupled interconnects when both inputs switch in opposite directions. These two decoupled interconnects can therefore be used to determine the output waveforms of two coupled interconnects.

## III. CROSSTALK NOISE MODEL OF TWO-COUPLED INTERCONNECTS

Based on the decoupling technique, the crosstalk noise model is first developed for two identical coupled *RLC* interconnects. The crosstalk noise model is then applied to nonidentical coupled *RLC* interconnects and compared with SPICE, exhibiting an average error of 6.8%.

### A. Crosstalk Noise Model of Two Identical Coupled Interconnects

For the coupled interconnects shown in Fig. 1 with  $\Delta r = 0$ ,  $\Delta c = 0$ , and  $\Delta l = 0$ , the transient response at the two outputs can be expressed using the normalized variables listed in Table I. Furthermore, in order to characterize the effect of inductance on the crosstalk noise, a parameter  $\zeta$ , described in [9], is used, where  $\zeta$  is defined as

$$\zeta = \frac{R_T + R_T C_T + R_R C_T + 0.5 R_R}{2\sqrt{(1 + C_T)}}. \quad (13)$$

$$E = \begin{bmatrix} 1 & 0 & [r(1 - \Delta r) + sl(1 - \Delta l)]dx & sl_m dx \\ 0 & 1 & sl_m dx & [r(1 + \Delta r) + sl(1 + \Delta l)]dx \\ s[c_g(1 - \Delta c) + c_c]dx & -sc_c dx & 1 & 0 \\ -sc_c dx & s[c_g(1 + \Delta c) + c_c]dx & 0 & 1 \end{bmatrix}. \quad (1)$$

TABLE I  
NORMALIZED VARIABLES FOR TWO COUPLED INTERCONNECTS

Variable	Definition	Physical Meaning
$Z_o$	$\sqrt{l/c_g}$	Characteristic impedance
$t_f$	$h\sqrt{lc_g}$	Time of flight
$R_R$	$hr/Z_o$	Normalized line resistance
$R_T$	$R_s/Z_o$	Normalized driver resistance
$C_T$	$C_L/(hc_g)$	Normalized load capacitance
$K_C$	$c_c/c_g$	Normalized coupling capacitance
$K_L$	$l_m/l$	Normalized coupling inductance

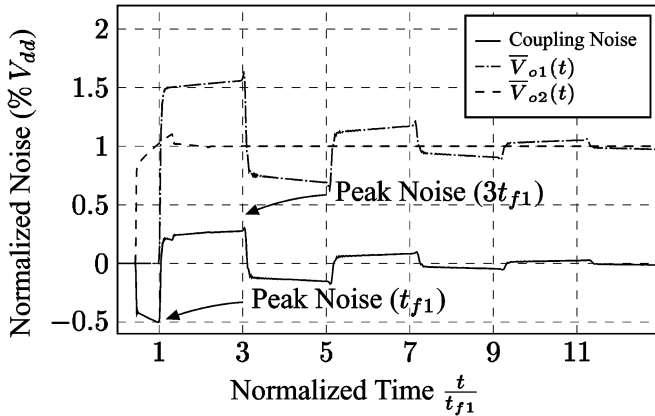


Fig. 2. Output waveform of decoupled interconnects and waveform of coupled noise between two coupled interconnects when  $t_{f1} > t_{f2}$  ( $K_L = 0.769$  and  $K_C = 0.217$ ). The input of the victim line remains at ground while the input of the aggressor line is a step input.

The crosstalk noise can therefore be expressed using only five variables,  $\zeta$ ,  $C_T$ ,  $R_T$ ,  $K_C$ , and  $K_L$ .

The decoupled interconnects can be used to determine the peak crosstalk noise. For two strongly inductively coupled interconnects ( $K_L \gg K_C$  such that  $t_{f1} > t_{f2}$ ), the waveform of the coupling noise and the output waveforms,  $\bar{V}_{o1}(t)$  and  $\bar{V}_{o2}(t)$ , of the decoupled interconnects are shown in Fig. 2, where  $t_{f1}$  and  $t_{f2}$  are

$$t_{f1} = h\sqrt{(l+l_m)c_g} \quad (14)$$

$$t_{f2} = h\sqrt{(l-l_m)(c_g+2c_c)}. \quad (15)$$

$t_{f1}$  and  $t_{f2}$  are the times of flight of two decoupled interconnects, respectively.

Based on the traveling-wave model of a transmission line, the traveling wave is reflected at the load, returns to the source, and then returns to the load, causing the output to overshoot and undershoot at the times of  $t_f$  and  $3t_f$ , respectively. During the interval between  $t_f$  and  $3t_f$ , the output of a lossy transmission line with a capacitive load behaves as an RC line, and the output increases due to RC charging [10].

The waveform of the coupling noise can be determined by subtracting the decoupled voltage  $\bar{V}_{o2}(t)$  from  $\bar{V}_{o1}(t)$ . The negative peak of the coupling noise occurs at time  $t_{f1}$ , as shown in Fig. 2, and is

$$V_{\text{noise}}(t_{f1}) = -\frac{1}{2}\bar{V}_{o2}(t_{f1}). \quad (16)$$

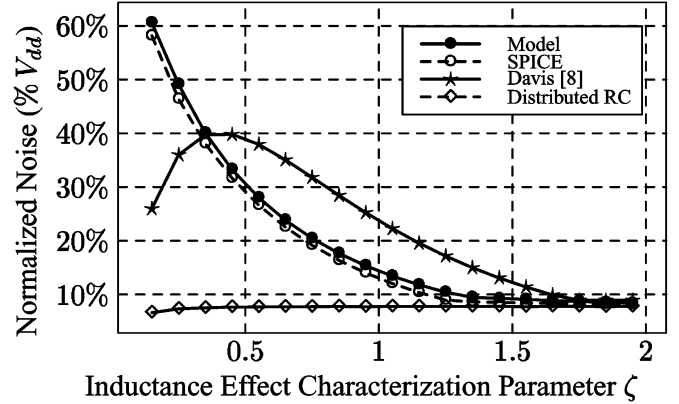


Fig. 3. Comparison of crosstalk model to SPICE, Davis [2], and distributed RC model for different values of  $\zeta$  ( $K_C = 0.217$ ,  $K_L = 0.769$ ,  $C_T = 0.05$ , and  $R_T = 0.25$ ).

At the time of  $3t_{f1}$ , the decoupled voltage  $\bar{V}_{o1}(t)$  is maximum. The positive peak of the coupling noise is

$$V_{\text{noise}}(3t_{f1}) = \frac{1}{2}(\bar{V}_{o1}(3t_{f1}) - \bar{V}_{o2}(3t_{f1})). \quad (17)$$

Combining (16) and (17), the peak crosstalk noise of two strongly inductively coupled interconnects is

$$V_{\text{peak}} = \max\{V_{\text{noise}}(t_{f1}), V_{\text{noise}}(3t_{f1})\}. \quad (18)$$

An analysis of the crosstalk noise when  $t_{f1} < t_{f2}$  is similar to an analysis of the crosstalk noise with the positive and negative peak noise occurring at  $t_{f2}$  and  $3t_{f2}$ , respectively. The peak crosstalk noise between two coupled interconnects (either  $t_{f1} > t_{f2}$  or  $t_{f1} < t_{f2}$ ) can be unified and is

$$t_{f_{\text{max}}} = \max\{t_{f1}, t_{f2}\} \quad (19)$$

$$V_{\text{peak}} = \max\{V_{\text{noise}}(t_{f_{\text{max}}}), V_{\text{noise}}(3t_{f_{\text{max}}})\}. \quad (20)$$

The peak noise in (20) is determined from the transient response of the two decoupled interconnects. In order to determine the precise value of the decoupled voltages  $\bar{V}_{o1}(t)$  and  $\bar{V}_{o2}(t)$  at  $t_{f_{\text{max}}}$  and  $3t_{f_{\text{max}}}$ , a traveling wave-based approximation technique (TWA), as described in [10], is used to construct the transient output response of the two decoupled interconnects. Through the TWA technique, the peak crosstalk noise is compared to SPICE for various values of the five variables  $\zeta$ ,  $C_T$ ,  $R_T$ ,  $K_C$ , and  $K_L$ , as shown in Figs. 3 and 4. These cases consider most practical on-chip interconnect scenarios, ranging from those cases where the inductance effect can be ignored to highly inductive cases. The line dimensions of the coupled interconnects vary for each case. The dimensions of the example line for the coupled interconnects are a length of  $5000 \mu\text{m}$ , a width of  $2 \mu\text{m}$ , and a height of  $2 \mu\text{m}$ . The crosstalk noise model developed by Davis [2] is also shown in Fig. 3 for comparison. In [2], the crosstalk is assumed to occur at the time of flight  $t_f$ , and is valid only when the two propagation modes have the same time of flight.

The interconnect is divided into segments with a length of  $10 \mu\text{m}$ , where each segment is modeled by a  $\pi$  circuit with resistance, ground capacitance, coupling capacitance, partial self-inductance, and partial mutual inductance. The coupled interconnects are simulated using SPICE. The peak crosstalk noise of two coupled RLC interconnects

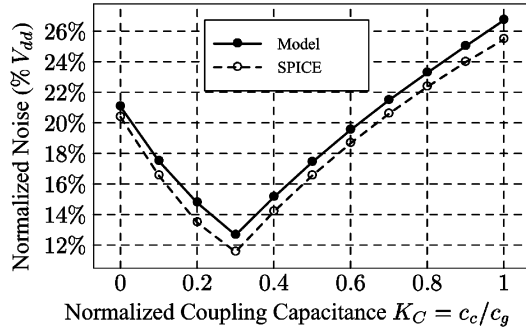


Fig. 4. Comparison of crosstalk model to SPICE for different values of  $K_C$  ( $K_L = 0.769$ ,  $\zeta = 1$ ,  $C_T = 0.05$ , and  $R_T = 0.25$ ).

decreases when the inductance effect characterization parameter  $\zeta$  increases (producing a smaller inductance effect), as shown in Fig. 3. As expected, the distributed  $RC$  interconnect model can be used to determine the peak crosstalk noise when  $\zeta$  is sufficient large ( $\zeta > 1.5$ ). The peak noise is almost constant for the normalized load capacitance  $C_T$  varying over the practical range of  $0 < C_T \leq 0.1$ , and decreases with larger normalized driver resistance  $R_T$ . The peak crosstalk noise does not increase monotonically with an increase in the normalized inductive coupling factor  $K_L$  or capacitive coupling factor  $K_C$  (as shown in Fig. 4).

#### B. Noise Model of Two Nonidentical Coupled Interconnects

Since two nonidentical coupled  $RLC$  interconnects can be approximately decoupled into two independent  $RLC$  interconnects, the crosstalk noise can be estimated similarly to the case of two identical coupled  $RLC$  interconnects. As listed in Table II, the crosstalk noise between two nonidentical coupled interconnects is determined from the decoupling technique represented by (5)–(8) and compared with SPICE for different  $R$ ,  $C_1/C_2$ , and  $L_1/L_2$ , where  $R$ ,  $C_1$  ( $L_1$ ), and  $C_2$  ( $L_2$ ) are the resistance and ground capacitances (self inductances), respectively, of the two nonidentical interconnects. For a bus structure, the range of variation of  $C_1/C_2$  and  $L_1/L_2$  in most cases is between 0.8 and 1.2. The physical parameters of two nonidentical interconnects are the driver resistance  $R_s = 11 \Omega$ , load capacitance  $C_l = 0.05$  pF, ground capacitance  $C_2 = 1$  pF, self-inductance  $L_2 = 2$  nH, coupling capacitance  $C_c = 0.22$  pF, and mutual inductance  $L_m = 1.2$  nH. The average error of the crosstalk noise model for two nonidentical coupled interconnects is 3.1% as compared to SPICE.

For multiple parallel signal lines, the crosstalk analysis can be decomposed into pairs of victim signal lines and every other signal line. The amplitude and time of the coupling noise waveform between each pair of two coupled interconnects can be determined. The crosstalk noise of multiple signal lines can therefore be analyzed through superposition.

#### IV. APPLICATION TO SHIELD INSERTION

In Section III, a crosstalk noise model for two coupled  $RLC$  interconnects is developed, as shown in (20). The crosstalk noise model can be used to evaluate the effectiveness of the shield insertion process in reducing coupling noise among coupled  $RLC$  interconnects. In this section, the concept of an effective mutual inductance is presented, followed by an estimate of crosstalk noise for coupled  $RLC$  interconnects with shield lines, and a discussion of the effect of shield insertion on reducing crosstalk noise.

Current is distributed among multiple return paths so as to minimize the total impedance  $Z(\omega) = R + j\omega L$ . At high frequencies, where the inductance dominates ( $R \ll j\omega L$ ), the return current seeks the

TABLE II  
COMPARISON OF CROSSTALK NOISE BETWEEN TWO NONIDENTICAL COUPLED INTERCONNECTS WITH VARIATIONS OF  $R$ ,  $C_1/C_2$ , AND  $L_1/L_2$

$R(\Omega)$	$\frac{C_1}{C_2}$	$\frac{L_1}{L_2}$	SPICE (% $V_{dd}$ )	Analytic (% $V_{dd}$ )	Error (%)
54	1.1	0.8	29.24	30.77	5.23
		0.9	31.14	31.51	1.19
		1	32.31	32.22	0.28
		1.1	32.92	32.81	0.33
		1.2	33.10	33.36	0.79
		1.2	33.10	32.29	2.15
	1.2	0.8	30.81	29.80	3.28
		0.9	32.23	30.59	5.09
		1	32.97	31.33	5.23
		1.1	33.21	31.87	4.03
		1.2	33.10	32.29	2.15
		145	1.1	0.8	11.99
0.9	12.83			13.62	6.16
1	13.49			14.09	4.45
1.1	14.01			14.54	3.78
1.2	14.40			14.97	3.96
1.2	14.47			14.28	1.33
1.2	0.8		12.52	12.51	0.08
	0.9		13.24	13.03	1.59
	1		13.77	13.53	1.74
	1.1		14.17	13.92	1.76
	1.2		14.47	14.28	1.33

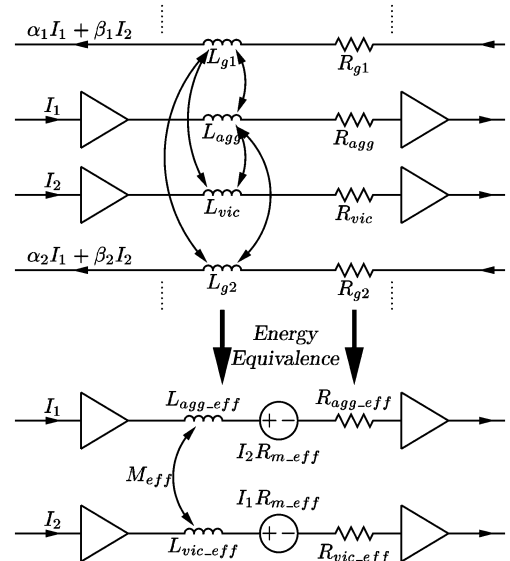


Fig. 5. Simplification of multiple interconnects into two coupled signal lines with effective self inductances, effective mutual inductance, and effective resistances based on the equivalence of the magnetic energy stored in these two systems.

paths of least inductance. The distribution of the current return paths for both the aggressor and victim lines can be determined [11]. The current distribution, rather than techniques to determine the current distribution [11], is the input to the effective mutual inductance model discussed in this section.

With knowledge of the current return paths, the coupled  $RLC$  signal lines with the surrounding ground lines can be converted into two coupled  $RLC$  lines using the law of energy equivalence. As illustrated in Fig. 5, inductive interactions between two signal lines and the surrounding ground lines can be incorporated into two coupled signal lines

TABLE III  
EFFECT OF SHIELD INSERTION ON EFFECTIVE MUTUAL INDUCTANCE AND CROSSTALK NOISE

No. of Shields	Effective Inductance (nH)						Crosstalk Noise (% $V_{dd}$ )		
	Mutual			Self			Analytic	SPICE	Error
	Analytic	FastHenry	Error	Analytic	FastHenry	Error			
No shield	2.655	2.655	0.00%	4.839	4.839	0.00%	38.66%	36.83%	4.73%
One shield	0.086	0.089	3.37%	2.269	2.273	0.18%	14.38%	15.15%	5.08%
Two shields	0.437	0.437	0.00%	2.115	2.118	0.14%	16.10%	15.06%	6.91%
Three shields	-0.048	-0.045	6.67%	1.634	1.636	0.12%	10.83%	9.61%	12.70%

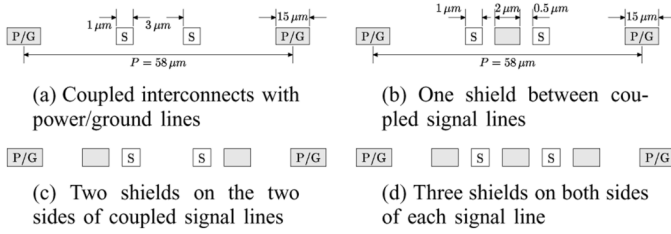


Fig. 6. Different structures for inserting shield lines to reduce crosstalk noise.

with effective self inductances and an effective mutual inductance, permitting an estimate of the crosstalk noise between two lines. Assuming the current flowing through the aggressor line is  $I_1$  with a ground return current distribution  $\alpha$ , and the current through the victim line is  $I_2$  with a ground return current distribution  $\beta$ , the magnetic field energy stored in the original system is

$$\begin{aligned}
 W_m &= \frac{1}{2} \mathbf{I}_b^T \mathbf{L} \mathbf{I}_b \\
 &= \frac{1}{2} (\alpha I_1 + \beta I_2)^T \mathbf{L} (\alpha I_1 + \beta I_2) \\
 &= \frac{1}{2} \alpha^T \mathbf{L} \alpha I_1^2 + \frac{1}{2} \beta^T \mathbf{L} \beta I_2^2 + \frac{1}{2} (\alpha^T \mathbf{L} \beta + \beta^T \mathbf{L} \alpha) I_1 I_2.
 \end{aligned} \quad (21)$$

The magnetic field energy stored in the equivalent system is

$$\begin{aligned}
 W'_m &= \frac{1}{2} \begin{bmatrix} I_1 & I_2 \end{bmatrix} \begin{bmatrix} L_{agg\_eff} & M_{eff} \\ M_{eff} & L_{vic\_eff} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \\
 &= \frac{1}{2} L_{agg\_eff} I_1^2 + \frac{1}{2} L_{vic\_eff} I_2^2 + M_{eff} I_1 I_2.
 \end{aligned} \quad (22)$$

By using the equivalence of magnetic energy stored in these two systems  $W_m = W'_m$ , the effective self-inductance and the effective mutual inductance are

$$L_{agg\_eff} = \alpha^T \mathbf{L} \alpha \quad (23)$$

$$L_{vic\_eff} = \beta^T \mathbf{L} \beta \quad (24)$$

$$M_{eff} = \alpha^T \mathbf{L} \beta. \quad (25)$$

Similarly, the effective resistance can be determined from the equivalence of the power consumed in these two systems, where

$$R_{agg\_eff} = \alpha^T \mathbf{R} \alpha, \quad (26)$$

$$R_{vic\_eff} = \beta^T \mathbf{R} \beta, \quad (27)$$

$$R_{m\_eff} = \alpha^T \mathbf{R} \beta. \quad (28)$$

Based on the decoupling technique described in Section II, two coupled  $RLC$  interconnects with resistive coupling ( $r_m$ ) can be decoupled into two isolated  $RLC$  interconnects with physical parameters of  $(c_g, r + r_m, l + l_m)$  and  $(c_g + 2c_c, r - r_m, l - l_m)$ , respectively. The crosstalk noise model discussed in Section III can therefore be applied to analytically estimate the crosstalk noise among coupled  $RLC$  interconnects using the effective inductance and resistance.

Three cases of shield insertion (and one unshielded case) for coupled  $RLC$  interconnects are shown in Fig. 6. Coupled interconnects with a length of  $5000 \mu\text{m}$  are shielded using one, two, and three ground lines, respectively. The effectiveness of these shielding lines in reducing crosstalk noise are investigated based on the proposed crosstalk noise models.

With the effective inductance and capacitance, an estimate of the crosstalk noise voltage can be analytically obtained from the crosstalk model described in Section III. Applying (20) to the effective inductance matrix and effective capacitance matrix for the four structures illustrated in Fig. 6, with a driver resistance of  $25 \Omega$  and a load capacitance of  $50 \text{ fF}$ , the crosstalk noise is compared in Table III.

As listed in Table III, inserting a shield line in the vicinity of a signal line can greatly reduce the effective mutual inductance, significantly reducing the coupling noise. A shield inserted between the aggressor line and the victim line, as shown in Fig. 6(b), has a greater effect on reducing the effective mutual inductance than inserting shield lines along the other side of the signal lines, as shown in Fig. 6(c). The two-shield scenario also does not eliminate capacitive coupling, which contributes to a higher crosstalk noise than the one-shield scenario. The three shield interconnect structure shown in Fig. 6(d) exhibits the lowest crosstalk noise. This structure, however, requires the greatest silicon area. The two-shield structure shown in Fig. 6(c) reduces the crosstalk noise to a level comparable with the three-shield structure, suggesting that a pattern of a shield line for every two global signal lines is a desirable structure to control crosstalk noise. Another interesting phenomenon is that the effective self-inductance drops with each inserted shield line, reducing the inductance of the signal lines.

## V. CONCLUSIONS

A decoupling technique for both identical and nonidentical coupled  $RLC$  interconnects is developed based on the  $ABCD$  matrix of interconnects. Based on the decoupling technique, an analytic crosstalk noise model is presented, with the peak noise occurring at the time of flight  $t_f$  or  $3t_f$ . The model exhibits an average error of 6.8% as compared to SPICE. The crosstalk noise model is used to evaluate the effectiveness of shield insertion on reducing crosstalk noise by applying the proposed effective mutual inductance model. Guidelines are provided for inserting shields among coupled  $RLC$  interconnects in the presence of both capacitive and inductive coupling. It is shown that a shield line in the vicinity of the signal lines can greatly reduce inductive coupling. A pattern of a shield line for every two global signal lines in the upper metal layers is shown to be desirable for controlling crosstalk noise.

## REFERENCES

- [1] K. T. Tang and E. G. Friedman, "Peak crosstalk noise estimation in CMOS VLSI circuits," in *Proc. IEEE Int. Conf. Electron. Circuits Syst.*, 1999, pp. 1539–1542.
- [2] A. J. Davis and D. J. Meindl, "Compact distributed RLC interconnect models-Part II: Coupled line transient expressions and peak crosstalk in multilevel networks," *IEEE Trans. Electron Devices*, vol. 47, no. 11, pp. 2078–2087, Nov. 2000.

- [3] A. Naeemi, J. A. Davis, and J. D. Meindl, "Analysis and optimization of coplanar RLC lines for GSI global interconnection," *IEEE Trans. Electron Devices*, vol. 51, no. 6, pp. 985–994, Jun. 2004.
- [4] J. Chen and L. He, "A decoupling method for analysis of coupled RLC interconnects," in *Proc. ACM Great Lakes Symp. VLSI*, 2002, pp. 41–46.
- [5] W. Jin, S. Yoon, and J. Kim, "Experimental characterization and modeling of transmission line effects for high-speed VLSI circuit interconnects," *Inst. Electron. Informat. Commun. Eng. Trans. Electron.*, vol. 83, no. 5, pp. 728–735, May 2000.
- [6] P. Saxena and S. Gupta, "On integrating power and signal routing for shield count minimization in congested regions," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 2, pp. 437–445, Apr. 2003.
- [7] J. Zhang and E. G. Friedman, "Crosstalk noise model for shielded interconnects in VLSI-based circuits," in *Proc. IEEE Int. SOC Conf.*, 2003, pp. 243–244.
- [8] A. B. Kahng and S. Muddu, "An analytical delay model for RLC interconnects," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 16, no. 12, pp. 1507–1514, Dec. 1997.
- [9] Y. I. Ismail and E. G. Friedman, "Effects of inductance on the propagation delay and repeater insertion in VLSI circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 8, no. 2, pp. 195–206, Apr. 2000.
- [10] Y. Eo, J. Shim, and W. R. Eisenstadt, "A traveling-wave-based waveform approximation technique for the timing verification of single transmission lines," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 21, no. 6, pp. 723–730, Jun. 2002.
- [11] B. Krauter and S. Mehrotra, "Layout based frequency dependent inductance and resistance extraction for on-chip interconnect timing analysis," in *Proc. ACM/IEEE Des. Automat. Conf.*, 1998, pp. 303–308.

## A Process Variation Compensating Technique With an On-Die Leakage Current Sensor for Nanometer Scale Dynamic Circuits

Chris H. Kim, Kaushik Roy, Steven Hsu, Ram Krishnamurthy, and Shekhar Borkar

**Abstract**—This paper describes a process compensating dynamic (PCD) circuit technique for maintaining the performance benefit of dynamic circuits and reducing the variation in delay and robustness. A variable strength keeper that is optimally programmed based on the die leakage, enables 10% faster performance, 35% reduction in delay variation, and 5× reduction in the number of robustness failing dies, compared to conventional designs. A new leakage current sensor design is also presented that can detect leakage variation and generate the keeper control signals for the PCD technique. Results based on measured leakage data show 1.9–10.2× higher signal-to-noise ratio (SNR) and reduced sensitivity to supply and p-n skew variations compared to prior leakage sensor designs.

**Index Terms**—CMOS digital integrated circuits, leakage currents, micro-processors, VLSI.

### I. INTRODUCTION

Increasing  $I_{off}$  with process scaling, has forced designers to upsize the keeper in dynamic circuits to obtain an acceptable robustness for the worst case leakage corner. However,  $20X + I_{off}$  variation in

Manuscript received August 4, 2005. This work was supported in part by the Semiconductor Research Corporation and by the Intel Ph.D. fellowship.

C. Kim is with the Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, MN 55455 USA (e-mail: chriskim@umn.edu).

K. Roy is with the Department of Electrical and Computer Engineering, Purdue University, Lafayette, IN 47906 USA.

S. Hsu, R. Krishnamurthy, and S. Borkar are with Circuit Research, Intel Labs, Hillsboro, OR 97124 USA.

Digital Object Identifier 10.1109/TVLSI.2006.878226

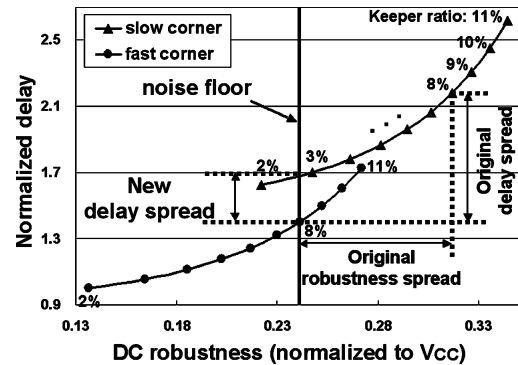


Fig. 1. Impact of keeper ratio on dynamic circuit delay and robustness for slow- and fast-corner processes.

nanoscale CMOS technologies indicates that: 1) a large number of low leakage dies suffer from the unnecessarily strong keeper and 2) the excess leakage dies still cannot meet the robustness requirements even with a keeper which is (typically) designed for the fast corner.

To overcome the suboptimality in current dynamic circuit designs, we propose a process compensating dynamic (PCD) circuit technique [1] that restores the robustness of worst case leakage dies and simultaneously improves performance in low-leakage dies. Unlike prior fixed-strength keeper techniques [2], our proposed PCD technique optimally adjusts the keeper strength based on the die leakage. The keeper strength is tuned using a digitally programmable 3-bit keeper which offers just the right keeper strength to meet a given target noise robustness under large die-to-die (D2D) leakage variations. Optimal keeper width is one-time programmed via fuses during the wafer level test. The PCD technique can also compensate within-die (WID) variation by locally generating the keeper control bits using a self-contained on-die leakage current sensor distributed across a die.

For the PCD technique to become viable, a circuit that can accurately measure the process variation based on nMOS pull-down leakage and generate the 3-bit keeper control signals is essential. There have been several previous approaches on measuring process variation for post silicon-tuning techniques. However, these techniques are not suitable for the proposed PCD technique due to limited resolution, susceptibility to process and voltage (PV) fluctuations, and high testing cost. In this paper, we present a new leakage current sensing technique for accurately measuring D2D and WID process variations [3]. Results based on measured leakage data show: 1) 1.9–10.2× higher SNR and 2) reduced sensitivity to supply and p-n skew variations compared to prior designs, while the proposed sensor only requires a single-bias generator even for multibit resolution sensing.

### II. LEAKAGE VARIATION AND KEEPER SIZING

Fig. 1 shows the impact of keeper sizing on the delay and dc robustness of a conventional 8-way dynamic bitline at worst case slow and fast process corners in a 1.2 V, 90-nm CMOS technology [4]. The dc robustness of a domino gate, corresponds to the unity gain noise (UGN) which is defined as the dc input noise voltage generating the equal level of noise in the final output of the domino gate. The keeper ratio is defined as the pMOS keeper width normalized to the entire pull-down nMOS width. A discrepancy in delay and robustness is observed across the slow-to-fast corner dies for a conventional static keeper. For example, a keeper ratio of 8% is required for the fast corner dies to meet the target noise floor. However, the 8% keeper sized for the fast corner leakage, leads to unnecessarily high robustness and large delay penalty in the slow-corner die. Instead of using the strong keeper, a downsized keeper