Design Methodology for Global Resonant H-Tree Clock Distribution Networks

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***Abstract*—Design guidelines for resonant H-tree clock distribution networks are presented in this paper. A distributed model of a two-level resonant H-tree structure is described, supporting the design of low power, skew, and jitter resonant H-tree clock distribution networks. Excellent agreement is shown between the proposed model and SpectraS simulations. A case study is presented that demonstrates the design of a two-level resonant H-tree network, distributing a 5-GHz clock signal in a 0.18-μm CMOS technology. This example exhibits an 84% decrease in power dissipation as compared to a standard H-tree clock distribution network. The design methodology enables tradeoffs among design variables to be examined, such as the operating frequency, the size of the on-chip inductors and capacitors, the output resistance of the driving buffer, and the interconnect width. A sensitivity analysis of resonant H-tree clock distribution networks is also provided. The effect of the driving buffer output resistance, on-chip inductor and capacitor size, and signal and shielding transmission line width and spacing on the output voltage swing and power consumption is described.**

***Index Terms*—H-tree sector, on-chip inductors and capacitors, resonant clock distribution networks, sensitivity.**

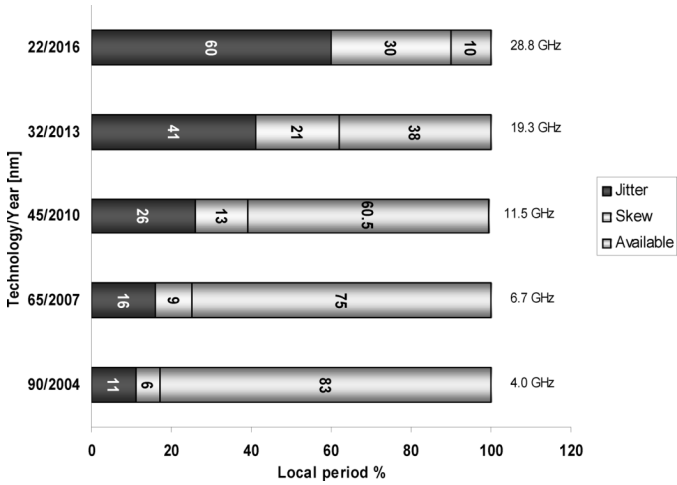

Fig. 1. 2002 ITRS predictions for skew and jitter [4].

I. Introduction

CLOCK signals in digital systems are simultaneously distributed to physically remote locations across an integrated circuit (IC). The clock signal provides a time reference that permits different parts of a circuit to operate in the correct order, thereby producing correct logical operation [1]. A clock signal is usually distributed from a common global source through metal interconnect networks and clock drivers, introducing delay. Unfortunately, the delay at every point on an IC cannot be precisely maintained, resulting in delay uncertainty [2]. Clock skew, which is the difference in the clock arrival times between sequentially adjacent registers, can lead to catastrophic logic failure [1]. Another undesirable effect is clock jitter which occurs when the edges of the clock signal fluctuate in time. This behavior occurs due to imperfections in the clock generator and power supply noise [3]. Previous work treating skew and jitter in resonant clock distribution networks is provided in [8]–[11]. Changes in the coupling capacitance and variations of the input capacitance of the registers also add random noise and increase jitter.

ITRS 2002 predictions regarding skew and jitter for different future technologies are shown in Fig. 1 [4]. According to these trends, by the year 2013 at a critical node technology of 32 nm, the skew and jitter will dominate synchronous performance, consuming 62% of the total clock period.

Synchronizing digital circuits at high frequencies has become more difficult since interconnect geometries do not scale as easily as transistors, producing longer wire delays. The capacitive load of the clock distribution has significantly increased, requiring a greater number of buffers. Additionally, during each cycle, the entire clock capacitance is charged and discharged to ground, dissipating the stored energy as heat. The focus of this paper is a design methodology for *low-power* resonant clock distribution networks.

To combat these phenomena, clock generation and distribution networks based on *LC* oscillators in the form of transmission line systems have been considered. In salphasic clock distribution networks [5], a sinusoidal standing wave is established within a transmission line. Coupled standing oscillators of this type are used in [6] to distribute a high frequency clock signal. A similar approach uses traveling waves in coupled transmission line loops [7] driven by distributed cross coupled inverters. Comprehensive and systematic investigation of the impact of width, spacing, and loading of a resonant clock tree on skew and energy consumption is presented in [8] and [9]. In [10] and [11], a resonant global clock distribution network is described,

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where on-chip spiral inductors and decoupling capacitors are connected to traditional clock trees.

The strategy presented in [10] is to design the H-tree sector and the clock grid for sufficient bandwidth to support distributed square waveform slew rates. Hence, distributing a square clock signal with a slew of t_r requires a bandwidth of at least $0.5/t_r$. From the Fourier theorem, as the bandwidth increases, the time domain response more closely resembles an ideal square wave signal. Unfortunately, the output resistance of the driving buffer and the rise time both have a major effect on the bandwidth.

A comprehensive and robust design methodology for resonant H-tree clock distribution networks is presented in this paper [12]. The methodology is based on the transfer function of a two-level H-tree, defined here as a sector, such that the fundamental harmonic of the input square wave is transferred to the output. The output signal at the leaf nodes exhibits a sinusoidal behavior. Inverters are placed at the leaf nodes to convert the sinusoidal waveform into a quasi-square waveform. On-chip spiral inductors and capacitors are used to resonate the clock signal around the harmonic frequency.

Significant variations are exhibited in modern high performance, high complexity integrated circuits fabricated in nanometer processes. With technology scaling, process variations have become a significant design factor that should be considered in the design process. Imperfections in the manufacturing process and environmental changes can degrade overall system performance [13]. Interconnect process variations can affect, for example, timing analysis, buffer insertion, high density SRAMs, and clock distribution networks [12]–[16]. Resonant H-tree structures tolerant to process variations are, therefore, important for high performance resonant clock distribution networks.

This paper is organized into six sections. The background and problem formulation of the resonant clock network are presented in Section II. In Section III, design guidelines are provided. In Section IV, a case study is presented. The sensitivity of a resonant clock distribution network to certain design parameters is examined in Section V. Some conclusions are offered in Section VI. A derivation of the H-tree sector model is described in Appendix A, while the rms input voltage is characterized in Appendix B. A model of an equivalent shorted interconnect is provided in Appendix C.

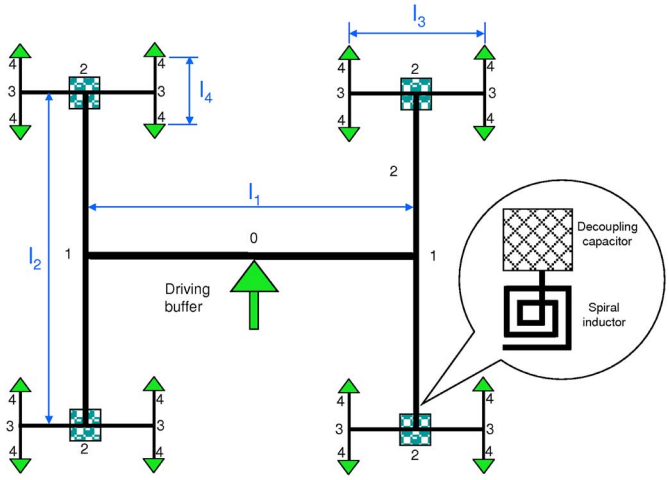


Fig. 2. H-tree sector with on-chip inductors and capacitors.

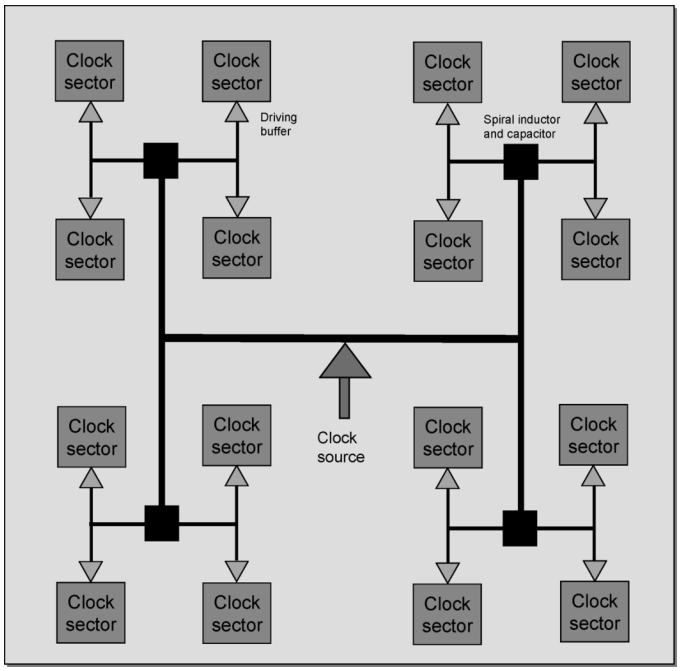


Fig. 3. Global clock distribution network, consisting of 16 resonant clock sectors and a total of 256 leafs.

II. Background and Problem Formulation

The concept of exploiting resonant transmission lines was first introduced by Chi in 1994 [5]. A global resonant clock distribution network was later introduced in 2003 by Chan *et al.* [10]. In this circuit, a set of discrete on-chip spiral inductors and capacitors is attached to a traditional H-tree structure, as depicted in Fig. 2. On-chip spiral inductors are connected at four points in the tree, while decoupling capacitors are attached to the other side of the spiral inductors.

The capacitance of the clock distribution network resonates with the inductance, while the on-chip capacitors establish a mid-rail dc voltage around which the grid oscillates. This approach lowers the power consumption, since the energy alternates between the electric and magnetic fields rather than dissipates as heat. Consequently, the number of gain stages is reduced, resulting in further reductions in power consumption, skew, and jitter.

In this paper, the proposed resonant sector (such as the network shown in Fig. 2) can be used as a building block, in a modular sense, to construct a much larger global clock distribution network, as shown in Fig. 3. In this example, the entire network is divided into sectors of 16 leaves. Hence, the design flow is bottom to top, starting with the H-tree sectors at the leaf portion of the tree network and moving up to the central sector (or trunk).

The design methodology considers the physical geometry of the structure and the technology, and can be formulated as

$$\text{H-Tree Sector} = f\left(w_i, l_i, h_i, f_o, C_l\right) \forall i \tag{1}$$

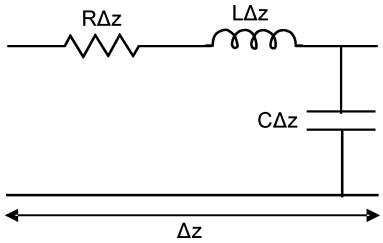


Fig. 4. Distributed model of a transmission line.

where w_i, l_i, and h_i are the width, length, and thickness of each section of the H-tree sector, respectively, f_o is the clock frequency, and C_l is the capacitive load at each leaf node. The index i varies between one and four, representing each section of the H-tree sector (see Fig. 2). The H-tree sector function is used to determine the value of the on-chip spiral inductors (considering the effective series resistance), capacitors, and driving buffer resistance that produces the minimum power consumption.

III. Design Guidelines for H-Tree Sector

A methodology for designing resonant H-tree clock distribution networks is described in this section. In Section III-A, a distributed model is presented for the H-tree sector, while an on-chip spiral inductor model is presented in Section III-B. Applying the proposed models and a graphical representation of the design space, the optimum value of the on-chip inductors, capacitors, and output resistance of the driving buffer for minimum power consumption is determined as described in Section III-C.

A. H-Tree Sector Model

As clock signal frequencies exceed the multigigahertz regime, distributed models of interconnects are required to incorporate high frequency effects into the system behavior. The proposed model uses the classical distributed model, where an incremental section of line length Δz is modeled as a lumped element circuit, as shown in Fig. 4. In this model, *R, L,* and *C* is the resistance, inductance, and capacitance per unit length, respectively. The lumped resistance represents the lossy component of the transmission line.

The proposed model is applied to a two-level H-tree network, as depicted in Fig. 2. The distributed *RLC* network shown in Fig. 5 is used to model the clock tree depicted in Fig. 2. The parameters R_i, L_i, and C_i are the resistance, inductance, and capacitance per unit length, respectively, where i varies from 1 to 4. The parameter N is the depth of the tree, which, in the example shown in Fig. 2, equals four, while the number of leafs is 2^N.

Since the two nodes labeled 1 in Fig. 5 are symmetric, the waveforms at these nodes are assumed to be identical, and as a result, can be assumed to be shorted [19]. The same assumption applies to nodes 2, 3, and 4. This simplification is exploited to transform the circuit shown in Fig. 5 into a distributed *RLC* transmission line as shown in Fig. 6, making the analysis considerably simpler.

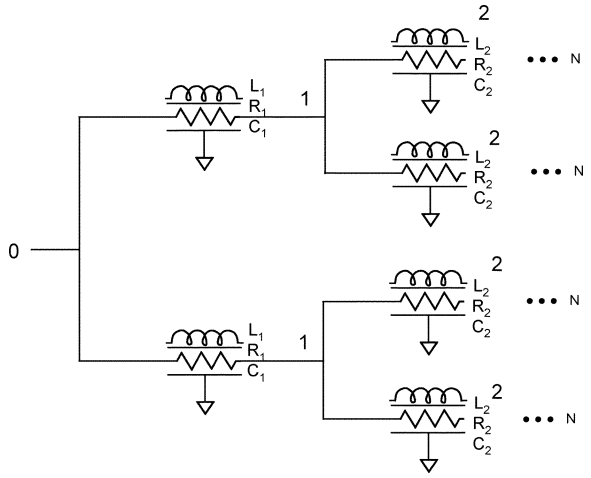


Fig. 5. Distributed *RLC* network representation of an H-tree network.

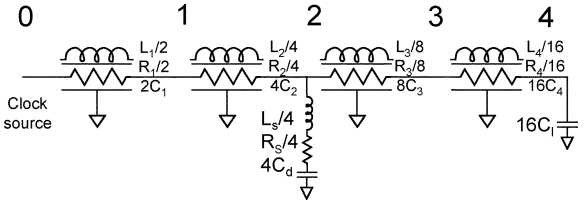


Fig. 6. Resonant H-tree network simplified to a distributed *RLC* line.

Since the interconnect lines between each pair of nodes are assumed to be connected in parallel, the capacitance per unit length is increased by a factor of two, while the resistance and inductance per unit length is decreased by a factor of two at each level of the hierarchy. A proof of the equivalent shorted interconnect is provided in Appendix C.

An analytic model of this structure is developed based on $ABCD$ parameters [20]. From transmission line theory, the $ABCD$ matrix for the overall structure is a product of the individual matrices

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = M_1 \cdot M_2 \cdot M_s \cdot M_3 \cdot M_4 \cdot M_l \tag{2}$$

where M_i $(i = 1, \ldots, 4)$, M_s, and M_l are the $ABCD$ matrix of the four sections, the on-chip inductors and capacitors, and the load, respectively.

From the overall $ABCD$ parameters, the transfer function $H(s)$ and input impedance $Z(s)$ of the system is, respectively

$$H(s) = \frac{1}{A} = K(s) \cdot \frac{a_2 \cdot s^2 + a_1 \cdot s + a_0}{b_3(s) \cdot s^3 + b_2(s) \cdot s^2 + b_1(s) \cdot s + b_0(s)} \tag{3}$$

$$Z_{\text{in}}(s) = \frac{A}{C} = \frac{b_3(s) \cdot s^3 + b_2(s) \cdot s^2 + b_1(s) \cdot s + b_0(s)}{d_3(s) \cdot s^3 + d_2(s) \cdot s^2 + d_1(s) \cdot s + d_0(s)} \tag{4}$$

where a_0, a_1, and a_2 are constants and the parameters K, b_0, b_1, b_2, b_3, d_0, d_1, d_2, and d_3 are functions of frequency, the geometry of the structure, and the on-chip inductors and capacitors.

TABLE I
ESRs OF SPIRAL INDUCTORS AT 5 GHz

L_s nH	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0	5.5	6.0	6.5	7.0	7.5	8.0	8.5	9.0	9.5	10
ESR Ω	8	8	8	19	20	24	28	32	35	61	72	52	84	98	109	113	160	169	226

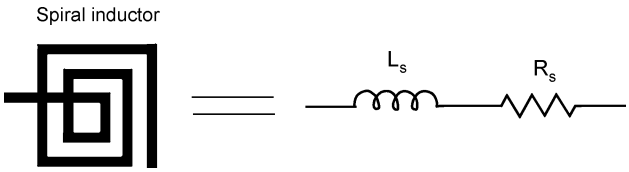


Fig. 7. Simplified model of an on-chip spiral inductor.

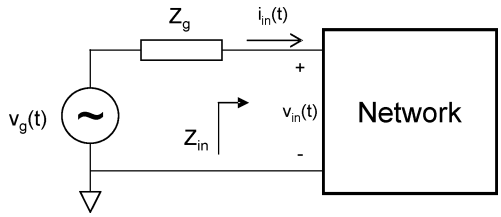


Fig. 9. One-port network driven by a voltage source.

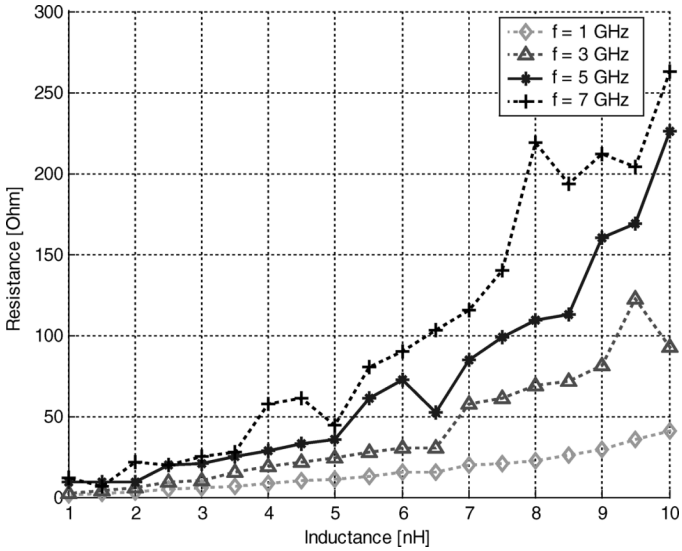


Fig. 8. Effective series resistance of spiral inductors.

These functions and the corresponding M_i matrices can be determined from (2), as described in Appendix A.

B. Model of H-Tree Spiral Inductor

On-chip spiral inductors play an important role in the design of silicon-based RF ICs. On-chip spiral inductors can be integrated into the fabrication process of a standard CMOS technology. Unfortunately, particularly in processes with a heavily doped silicon substrate, substrate losses resulting from eddy-current effects can be significant [21], [22]. It is, therefore, important to accurately model the resistive losses of the on-chip spiral inductors.

A resistive-inductive model of the spiral inductor, as shown in Fig. 7, is used in this analysis. In order to provide a tractable solution, the parasitic capacitance is omitted from the model and treated as part of the on-chip decoupling capacitor C_d. The parasitic resistance of a spiral inductor greatly affects the behavior of the resonant clock sector, and is included in the circuit model of the inductor. To determine the value of the on-chip spiral inductors and the effective series resistance (ESR), customized extraction software, Asitic, is used.[1]

In this example, the spiral inductors, occupying an area of $250 \times 250\ \mu\text{m}^2$, are optimized for maximum Q. The ESR for a range of inductor values at certain frequencies is shown in Fig. 8. Note that as the frequency increases, the ESR also increases. At low frequencies, the ESR exhibits a linear dependency with frequency, while at higher frequencies the relationship behaves quadratically. The values of ESR extracted at 5 GHz are used in the case study presented in Section IV. The ESRs for the different inductors at a 5-GHz operating frequency are listed in Table I.

C. On-Chip Inductor, Capacitor, and Output Resistance of the Driving Buffer

Since the transmission line network of a resonant H-tree is a passive linear network (assuming the inverter at the leaf node is modeled as a constant gate capacitance), a one-port network, as depicted in Fig. 9, is used to model the H-tree sector.

The driving buffer of the resonant clock tree is modeled as a voltage source $V_g(t)$ with a finite output impedance. The output impedance of the voltage source Z_g, and the input impedance of the network Z_{in} can be expressed, respectively, as

$$Z_g = R_g + jX_g \tag{5}$$

$$Z_{\text{in}} = R_{\text{in}} + jX_{\text{in}} \tag{6}$$

where R_g and R_{in} is the voltage source and input resistance, respectively, and X_g and X_{in} are the voltage source and input reactance, respectively. The rate at which energy is absorbed is the power and is [23]

$$P_{\text{net}} = \frac{1}{2} V_{\text{in,rms}}^2 \cdot \Re\left\{\frac{1}{Z_{\text{in}}}\right\} \tag{7}$$

where $V_{\text{in,rms}}$ is the effective or rms value of any periodic voltage function and is

$$V_{\text{in,rms}} = \left(\frac{1}{T}\int_{t_0}^{t_0+T} |v_{\text{in}}(t)|^2\, dt\right)^{1/2} \tag{8}$$

[1][Online]. Available: http://rfic.eecs.berkeley.edu/~niknejad/asitic.html

where T is the time period of the periodic function $v_{\rm in}(t)$. The input voltage $v_{\rm in}(t)$ (see Fig. 9) can be expressed in terms of the voltage source function $v_g(t)$, and is

$$v_{\rm in}(t) = v_g(t) \cdot \frac{Z_{\rm in}}{Z_{\rm in} + Z_g}. \tag{9}$$

Substituting (8) and (9) into (7) results in

$$P_{\rm net} = \frac{1}{2} V_{{\rm rms},g}^2 \cdot \left| \frac{Z_{\rm in}}{Z_{\rm in} + Z_g} \right|^2 \cdot \Re \left\{ \frac{1}{Z_{\rm in}} \right\} = \frac{1}{2} V_{{\rm rms},g}^2 \cdot \rho \tag{10}$$

where ρ is the effective [including R_g in (5)] real part of the input admittance of the H-tree sector

$$\rho = \frac{R_{\rm in}}{(R_{\rm in} + R_g)^2 + (X_{\rm in} + X_g)^2}. \tag{11}$$

Note from (10) that in order to reduce the power consumption $P_{\rm net}$, ρ should be made smaller. A second constraint is that the magnitude of the transfer function should be equal to or greater than 0.9 at the operating frequency in order to achieve a full swing response at the output. To justify a value of 0.9, consider a Fourier series representation of a periodic square waveform $x(t)$ with an amplitude of $V_{\rm DD}$

$$x(t) = \sum_{k=-\infty}^{\infty} a_k e^{jk\omega_0 t}, a_k = V_{\rm DD} \frac{1}{\pi k} \sin(k\omega_0 T_1) \tag{12}$$

where ω_0 is the radian frequency and T_1 is a quarter of the period of the square wave. The transfer function of the H-tree sector at the resonant frequency is designed to transfer the fundamental harmonic of the square wave $k = \pm 1$, amplifying the spectral elements

$$a_{\pm 1} = V_{\rm DD} \frac{1}{\pi}. \tag{13}$$

From (13), the amplitude transferred to the output equals $2V_{\rm DD}/\pi$. The sinusoidal amplitude at the output ranges from -0.1 to 1.9 V (1 V mean-to-peak) to allow the buffers at the leaf nodes to charge and discharge the load at frequencies as high as 5 GHz in a 0.18-μm CMOS technology. The required peak value of the magnitude of the transfer function can be derived from $(2V_{\rm DD}/\pi) \cdot |H'(j\omega_0)| = 1$

$$|H'(j\omega_0)| = \frac{\pi}{2V_{\rm DD}} = \frac{\pi}{2 \cdot 1.8} \approx 0.9. \tag{14}$$

Since the power consumption is inversely proportional to the output resistance, (11) suggests that the output resistance of the driving buffer should be maximized. These design constraints for a resonant H-tree network are summarized in (15)

$$\begin{cases} \min(P_{\rm net}) & \text{(15a)} \\ \max(R_g) & \text{(15b)} \\ |H'(j\omega_0)| \geq 0.9. & \text{(15c)} \end{cases}$$

In (15c), $|H'(j\omega)|$ is

$$\begin{aligned} |H'(j\omega)| &= \left| \frac{Z_{\rm in}}{Z_{\rm in} + Z_g} \right| \cdot |H(j\omega)| \\ &= \left| \frac{R_{\rm in} + jX_{\rm in}}{(R_{\rm in} + R_g) + j(X_{\rm in} + X_g)} \right| \cdot |H(j\omega)| \\ &= \sqrt{\frac{R_{\rm in}^2 + X_{\rm in}^2}{(R_g + R_{\rm in})^2 + (X_g + X_{\rm in})^2}} \cdot |H(j\omega)| \end{aligned} \tag{16}$$

where $|H(j\omega)|$ is described in (3) in the S-domain.

The three conditions in (15) can be used to determine the optimal value of the on-chip inductors, capacitors, and driving buffer resistance that produces a full swing sinusoidal waveform while dissipating minimum power. Since closed-form analytic expressions for the input impedance and the transfer function, given by (3) and (4), are somewhat cumbersome, the solution to (15) is graphically evaluated. In this manner, the design space and related tradeoffs among the different parameters can be explored.

Three design variables L_s, C_d, and R_g, are solved simultaneously to satisfy (15). In order to graphically represent the design space, one of the three design variables is eliminated. Equating $|H'(j\omega)|$ to 0.9 and solving for R_g (assuming $X_g = 0$)

$$R_g = \left(\sqrt{\frac{|H(j\omega)|^2}{0.9^2} \cdot (R_{\rm in}^2 + X_{\rm in}^2) - X_{\rm in}^2} \right) - R_{\rm in}. \tag{17}$$

Substituting (17) into (11) yields

$$\rho = \frac{0.9^2 \cdot R_{\rm in}}{|H(j\omega)|^2 \cdot (R_{\rm in}^2 + X_{\rm in}^2)}. \tag{18}$$

Note from (18) that ρ is only a function of the on-chip spiral inductor and capacitor at a specific frequency.

Once (18) is obtained, ρ and R_g are plotted as a function of the possible on-chip inductor values based on (3), (17), and (18). The inductor value varies from 1 to 10 nH, considering the ESR for each value (as described in Section III-B). Two graphs corresponding to the different on-chip capacitor values are obtained. In this way, the entire design space is conveniently represented graphically. Note that the condition (15b) is already included in (17) and (18), resulting in only two design graphs. Note also that according to (11), maximizing R_g results in minimizing ρ. From these two graphs, the optimal value for the on-chip inductor, capacitor, and output resistance can be determined.

IV. Case Study

In this section, a 5-GHz resonant H-tree sector is designed as a basic building block of a large global clock distribution network. The design guidelines and principles presented in Section III are demonstrated in this case study. The resistance, inductance, and capacitance per unit length of the transmission lines are extracted using HENRY and METAL from the OEA software suite.[2]

[2][Online]. Available: http://www.oea.com

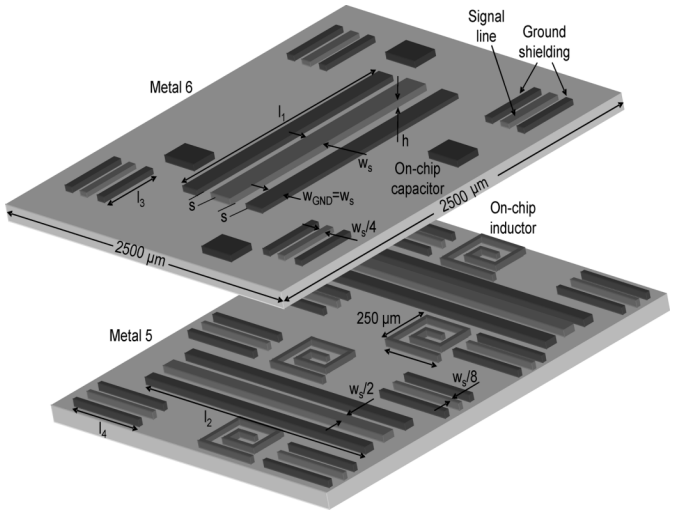


Fig. 10. Structure of resonant H-tree sector.

TABLE II
RESONANT H-TREE PARAMETERS

l_1, w_1 [μm]	l_2, w_2 [μm]	l_3, w_3 [μm]	l_4, w_4 [μm]
1600, 16	1600, 8	800, 4	800, 2

The layout geometry and configuration of a symmetric balanced resonant H-tree sector is schematically illustrated in Fig. 10. Assuming a 5-GHz clock signal, the design of a resonant H-tree based on a 0.18-μm CMOS technology is described.

The H-tree sector including the on-chip inductors and capacitors occupies two metal layers, metal 5 and metal 6, for a total area of 2500×2500 μm^2. The horizontal transmission line and capacitors are placed on metal 6, while the vertical transmission lines and spiral inductors are located on metal 5. This strategy reduces the coupling between the lines. In order to further reduce coupling noise, each signal line is shielded by two parallel ground lines. The separation distance s between the ground and signal lines is constant and is 4 μm, while the signal and ground line lengths and widths are the same in each section, i.e., $w_{\mathrm{GND}} = w_s = w_i$, where i varies between 1 and 4. The height of each metal line is $h = 0.5$ μm. These values are typical for a 0.18-μm CMOS technology. The capacitors are connected to ground, while the other end of the spiral inductors is connected to a signal line, namely, to l_4 (the connection is not shown in Fig. 10).

Finally, note that the width of the signal lines is reduced by two at each branching point in order to reduce reflections caused by differences between the characteristic impedance at the branch points. The individual interconnect widths and lengths, indicated in Fig. 10 and used in this example, are listed in Table II.

For the technology and geometry previously described (see Fig. 10), the extracted interconnect parameters are listed in Table III. The total load capacitance of the H-tree network is 2 pF. Inverters are located at the leaf nodes of the H-tree sector,

TABLE III
RESONANT H-TREE EXTRACTED TRANSMISSION LINE PARAMETERS

i	R_i [mΩ/μm]	L_i [pH/μm]	C_i [fF/μm]
1	3.19	1.19	0.28
2	6.37	1.43	0.30
3	12.75	1.53	0.13
4	25.50	1.78	0.14

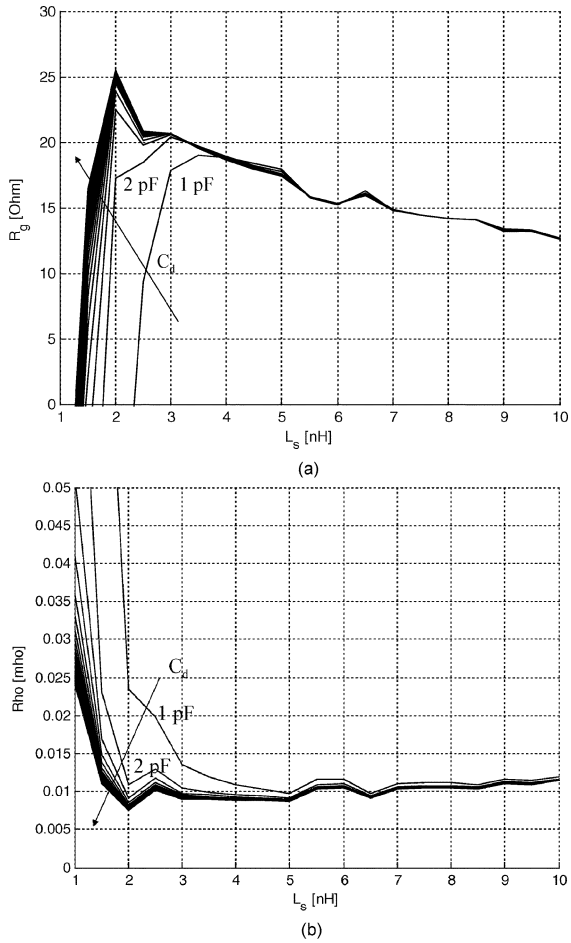


Fig. 11. Design tradeoffs for an H-tree sector. (a) Output resistance as a function of the spiral inductor. (b) ρ as a function of the on-chip spiral inductor.

each driving a capacitive load of 20 fF. A 20-fF load is chosen at the leaf nodes to satisfy a 5-GHz switching frequency of the buffers. If required, a larger load could be further partitioned into smaller loads. Expressions (17) and (18) at a 5-GHz operating frequency as a function of the spiral inductance are plotted in Fig. 11 over a wide range of capacitance values (1–40 pF).

In order to satisfy condition (15a), the spiral inductance is chosen to be $L_s = 2$ nH, thereby minimizing ρ and maximizing R_g, as evident from Fig. 11. Consequently, the maximum output resistance is $R_g \approx 25$ Ω. Evident from Fig. 11, as the on-chip capacitor increases, the curves converge. To determine the required on-chip capacitance, ρ and R_g are plotted as a function of the capacitance (see Fig. 12). For the chosen on-chip capacitor $C_d = 15$ pF, ρ and R_g saturate to a constant value.

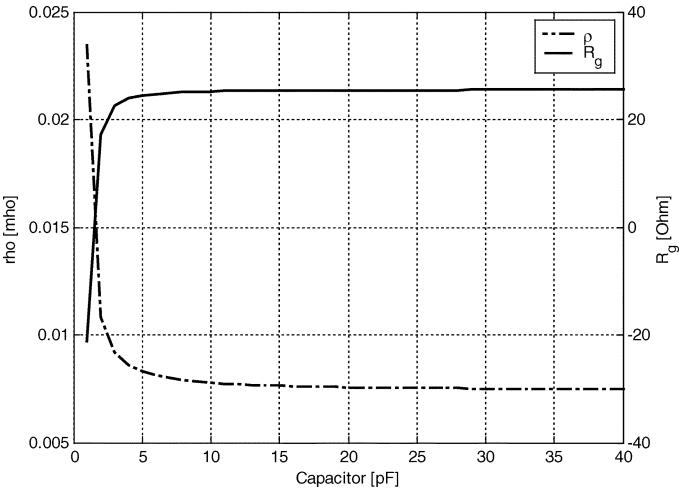


Fig. 12. Output resistance and ρ as a function of the on-chip capacitance with $L_s = 2$ nH.

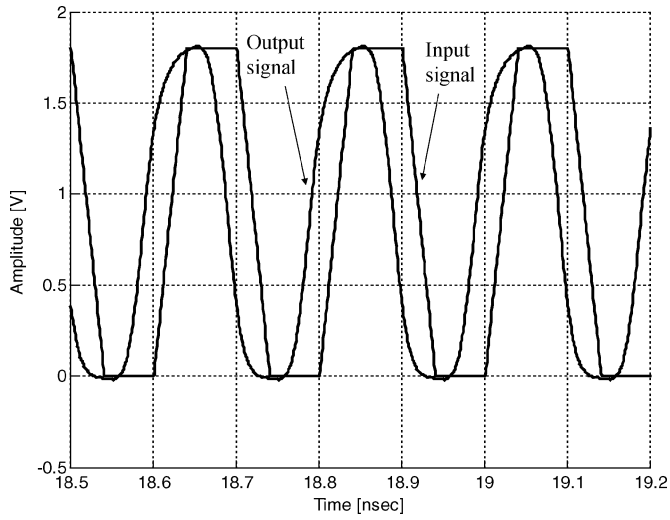


Fig. 13. Output waveform at the leaf nodes.

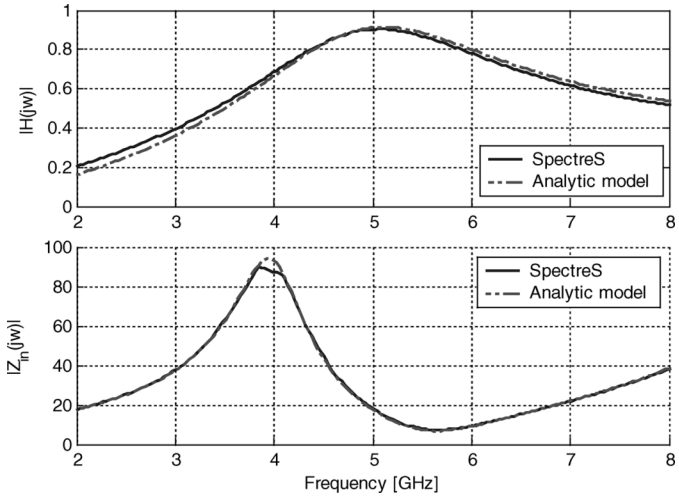


Fig. 14. Magnitude of the transfer function and input impedance.

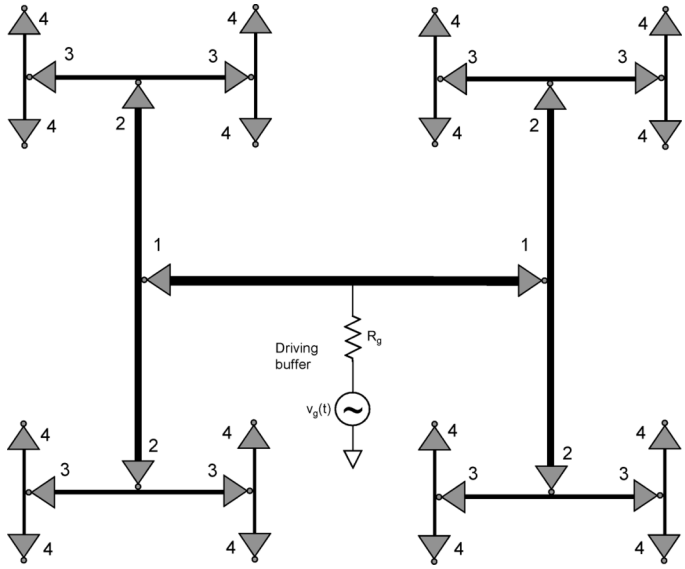


Fig. 15. Nonresonant H-tree sector with buffers.

The output waveform at the leaf nodes described in the time domain is shown in Fig. 13. Note that the square clock waveform is distributed to the leaf node, achieving a full rail-to-rail voltage swing. Also, note that the output waveform exhibits a quasi-sinusoidal characteristic common in nonresonant multigigahertz clock distribution networks [10].

In the frequency domain, the magnitude of the transfer function and input impedance around a 5-GHz operating frequency is shown in Fig. 14. Good agreement between simulation and the proposed analytic expressions is achieved, exhibiting less than 5% error. Note that the magnitude of the transfer function reaches 0.9 at a 5-GHz frequency. As predicted by the design expressions and verified by simulation, the power consumption in this example is $P_{\text{net}} \approx 15$ mW (including buffers) as compared to a nonresonant H-tree sector, where the power consumption is 93 mW (84% less than the nonresonant circuit).

The size, spacing between the signal and shielding lines, and the driver resistance R_g in the nonresonant network are maintained the same as in the resonant case. In order to drive the clock signal at a 5-GHz operating frequency, buffers are added at each branching point, as shown in Fig. 15. The size of these buffers is determined by simulations such that the rise time, 50% duty cycle, and amplitude of the clock signal at the leaf nodes are the same as the resonant network. For each buffer, the ratio of the pMOS and nMOS widths is 2.5, whereas the width of the nMOS transistors is listed in Table IV. The channel length of all of the buffers is 0.18 μm.

TABLE IV
BUFFER SIZES IN THE NONRESONANT CASE

w_1 [μm]	w_2 [μm]	w_3 [μm]	w_4 [μm]
3	8	20	50

Note that by eliminating the need for buffers in a resonant clock network, significant power savings can be achieved. As compared to a nonresonant network, the number of buffers is reduced. The skew and jitter will, therefore, also be smaller. This behavior is assumed since fewer devices will suffer process variations as well as coupling noise from the power supply.

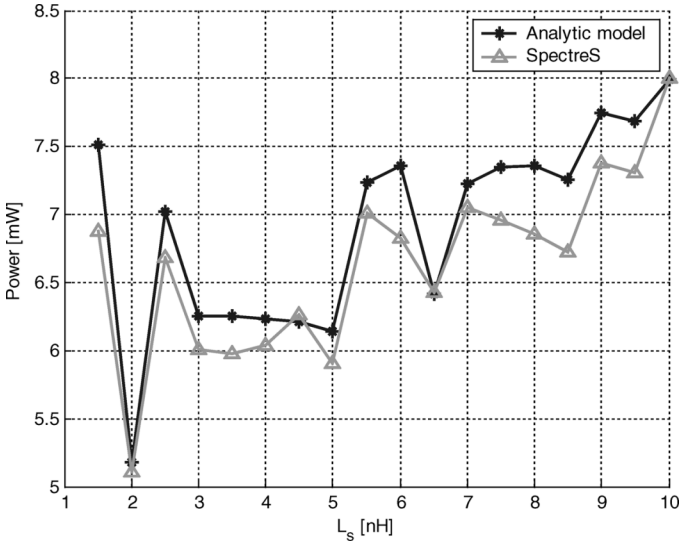


Fig. 16. Comparison of power consumption between analytic model and SpectreS Spice simulation.

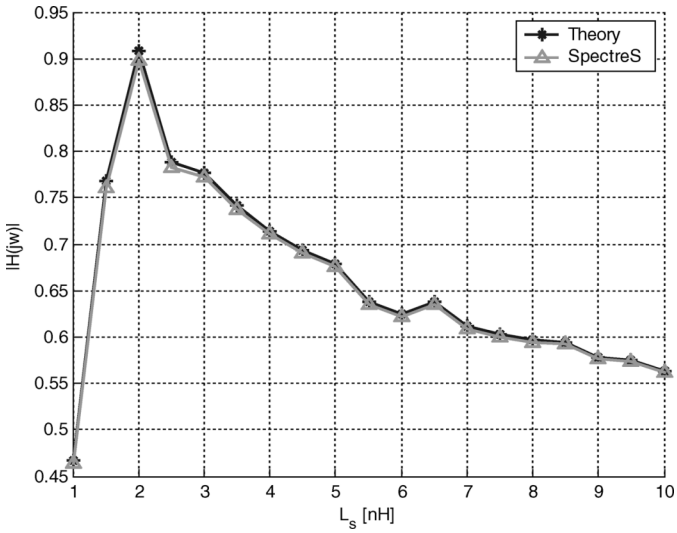


Fig. 18. Magnitude of the transfer function as a function of the inductance at a 5-GHz operating frequency.

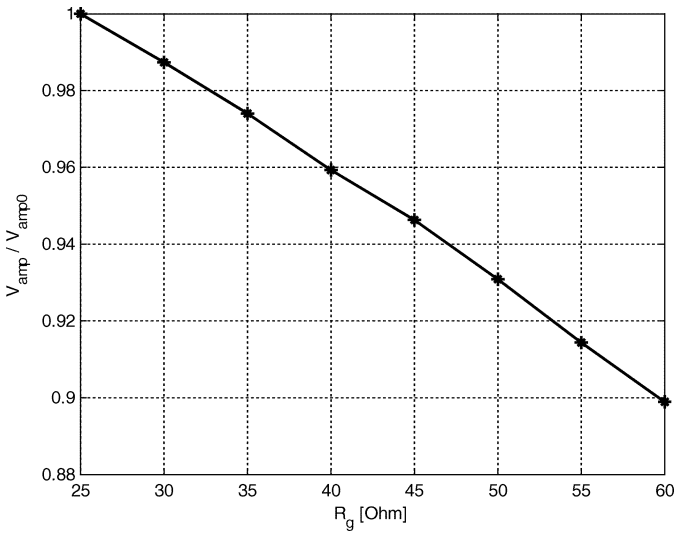


Fig. 17. Normalized voltage swing at the leaf node.

The power consumption as a function of the size of the on-chip inductors as expressed by (10) is shown in Fig. 16. Note that the maximum resistance of the output buffer is determined for each value of inductance. Good agreement between simulation and (10) is illustrated, exhibiting less than 10% error. As indicated in Fig. 16, the minimum power consumption for the circuit illustrated in Fig. 2 is about 5 mW (not including the buffers at the leaf nodes). Characterization of $V_{\mathrm{rms},g}$ in (10) is described in Appendix B.

To evaluate the performance and accuracy represented by this example, the normalized voltage swing as a function of R_g and the magnitude of the transfer function as a function of the on-chip inductance are shown, respectively, in Figs. 17 and 18. The normalized voltage swing is linearly decreasing with the output resistance, as shown in Fig. 17. At an output resistance $R_g = 25\ \Omega$, the network distributes a full voltage swing to the leaf nodes. The voltage swing degrades as R_g increases beyond 25 Ω, unable to achieve a full voltage swing. This result agrees with the design constraints described in (15).

The effect of the on-chip inductor on the magnitude of a transfer function is shown in Fig. 18. Increasing inductance degrades the magnitude of the transfer function, as indicated in Fig. 18. The magnitude of the transfer function reaches 0.9 with a 2-nH on-chip inductance, as obtained from Fig. 11. Note that for other values of inductance, the magnitude of the transfer function is smaller than 0.9. This behavior implies that the H-tree network can only deliver a full swing voltage waveform with an on-chip inductance of $L_s = 2$ nH. Also, note that the model closely agrees with the simulation (exhibiting a maximum error of 1.15%), as shown in Fig. 18.

V. Sensitivity of H-Tree Sector

The effect of process variations on the performance of a resonant H-tree sector is explored in this section. In particular, six types of circuit variations are considered: the driving buffer output resistance, on-chip inductor and capacitor size, and signal and shielding transmission line width and spacing. These variations are examined with respect to two performance related figures of merit: the clock signal voltage swing at the leaf nodes and the power consumption.

The buffer driving the H-tree sector is modeled as a voltage source with an effective output resistance. This simple model, however, does not consider process variations in the channel length and transistor doping concentration. Both of these effects can change the effective output resistance and thereby the performance.

To evaluate the effect of this variation on the resonant H-tree performance, the output resistance is varied over a range of ±25% of the optimal value (25 Ω), as shown in Fig. 19. The voltage swing at the leaves and variations in the power dissipation are considered as two performance metrics. The voltage swing is measured with respect to the clock output swing in Fig. 13 (1.8 V), while variations in the power consumption are

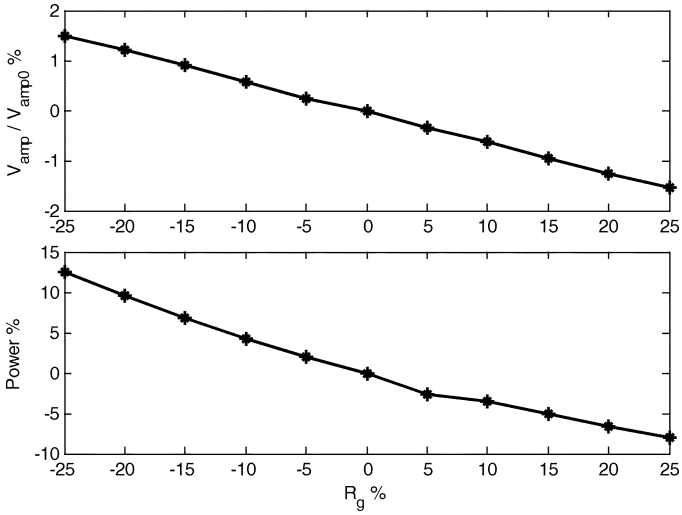


Fig. 19. Voltage swing and power consumption as a function of variations in the output resistance.

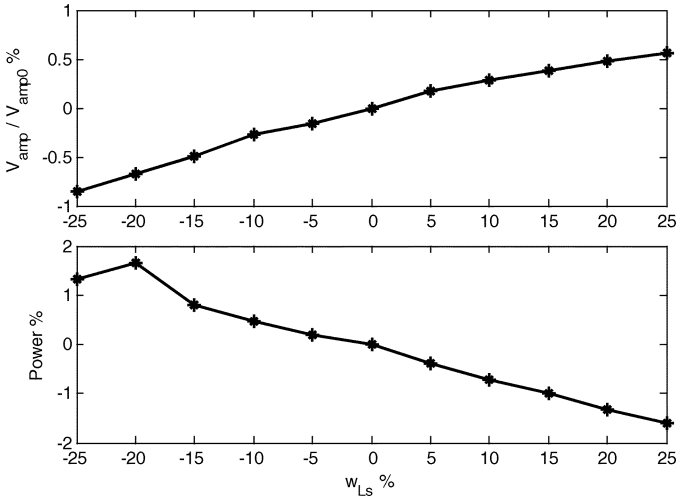


Fig. 20. Voltage swing and power consumption as a function of variations in the on-chip inductor width.

measured with respect to the optimal power consumption of 15 mW.

When the output resistance increases, the power consumption decreases. This behavior occurs since the power consumption is inversely proportional to the output resistance of the driving buffer. Note that the variation of the voltage swing is $\pm 1.25\%$, even at the extrema of the variations in the output resistance. The model can, therefore, be used to accurately represent the driving buffer.

To examine the effects of variations in the on-chip inductors and capacitors, consider Figs. 20 and 21. Variations in the spiral inductor, assuming a uniform distribution, are shown in Fig. 20. Process variations may alter the spiral wire width, changing the inductance and, therefore, the parasitic ESR. The change in inductance may occur due to the dependence of inductance on the specific geometry of the spiral.[1]

The inductance and ESR, extracted using Asitic, are a function of the variation in spiral width. For a $\pm 25\%$ change in the wire width, the output voltage swing varies less than $\pm 1\%$,

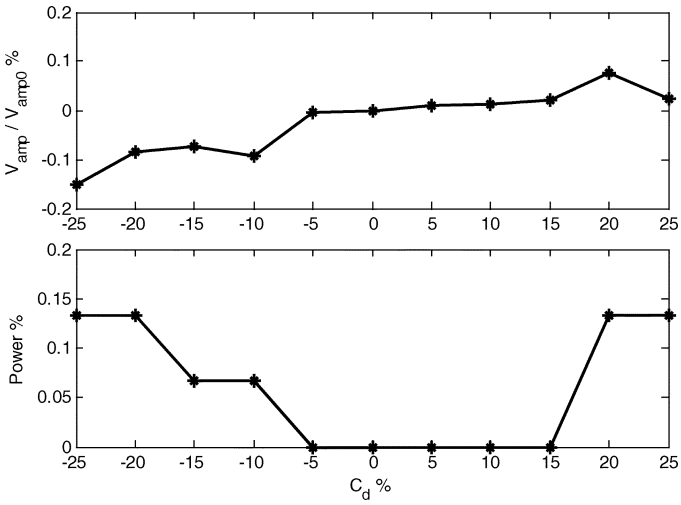


Fig. 21. Voltage swing and power consumption as a function of variations of the on-chip capacitor.

while the power consumption varies less than $\pm 2\%$. This behavior indicates that a resonant H-tree is highly tolerant to significant variations in the on-chip spiral inductor and suffers only a minor degradation in performance. Note that the inductance increases as the spiral inductor wire width increases, saving additional energy, as shown in Fig. 20.

In modern semiconductor fabrication processes, the on-chip capacitor can vary by up to $\pm 20\%$. To examine the effect of this variation on the behavior of the resonant H-tree, consider Fig. 21. The on-chip capacitors are swept over $\pm 25\%$ of the optimal value (15 pF). As observed from Fig. 21, the performance of the resonant H-tree is almost insensitive to these changes since the voltage swing varies by less than $\pm 0.15\%$, while the power consumption varies by less than $+0.15\%$. This behavior occurs since the transfer function of the entire network is a weak function of the magnitude of the on-chip capacitors. As previously mentioned, the primary purpose of the on-chip capacitors is to establish a dc voltage around which the clock signal oscillates. Another illustration of the insensitivity of a resonant H-tree network to on-chip capacitor variations is illustrated in Fig. 11. Note in Fig. 11 that as the on-chip capacitor increases, the characteristic become independent of C_d, hardly affecting the performance. This behavior occurs since at high frequencies and large capacitors, the impedance of C_d decreases, shunting the H-tree structure to ground.

To explore the effect of transmission line variations on the behavior of the H-tree sector, the dependence of three variations are evaluated. Specifically, the width of the signal and shield lines, and the spacing between the signal and shield lines are varied. As described by (1), these parameters affect the performance of the resonant H-tree. In the following investigation, it is assumed that the variations are uniformly distributed along the lines.

The impact of variations in the interconnect width (see Fig. 10) on H-tree performance is illustrated in Fig. 22. The H-tree interconnect width is varied by $\pm 10\%$, exhibiting a voltage swing and power variations of 0% to -0.25% and -0.9% to $+0.5\%$, respectively. Note that the resonant H-tree

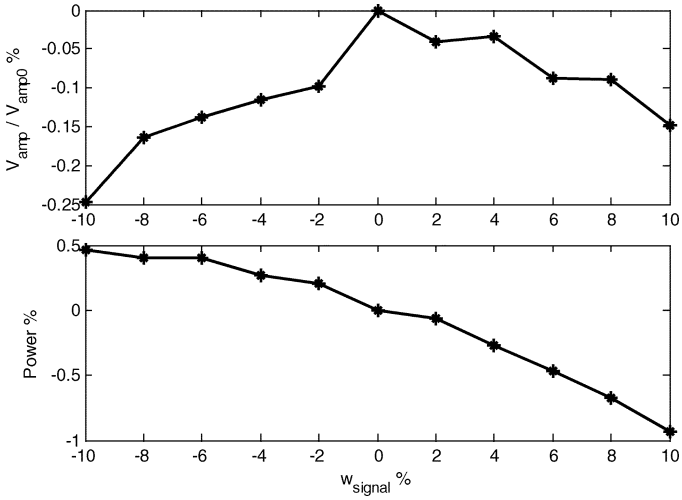


Fig. 22. Voltage swing and power consumption as a function of variations in the signal line width.

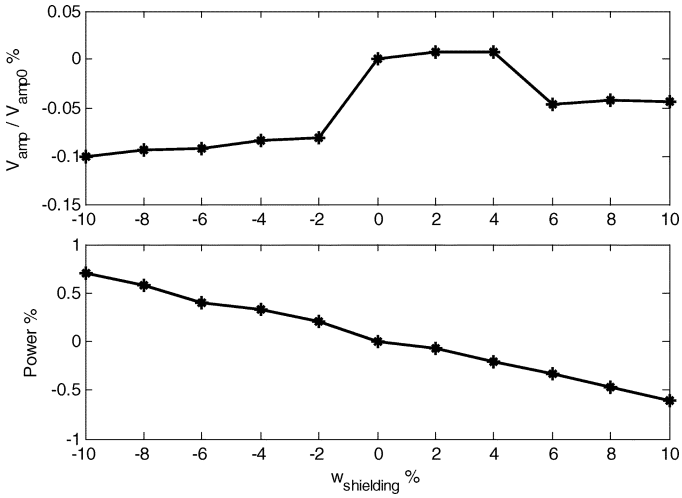


Fig. 23. Voltage swing and power consumption as a function of variations in the shield line width.

performance is not significantly affected, demonstrating the negligible effect of the interconnect width on a resonant H-tree sector. Note also that since the wire resistance is inversely proportional to the wire cross-sectional area, an increase in the interconnect width decreases the resistance, resulting in lower wire losses, thereby decreasing the power dissipation (see Fig. 22).

The impact of interconnect width variations on the shield lines is shown in Fig. 23. Similar to the signal line variations, the H-tree exhibits a voltage swing and power variations of about 0.1% and -0.6% to $+0.8\%$, respectively. Hence, the performance of the resonant H-tree network is preserved under these variations.

From a power consumption perspective, note that as the shield line width increases, the power dissipation decreases. This behavior occurs since the total equivalent resistance of the structure is increasing with wider shield lines, resulting in lower power consumption. The increase and decrease in the equivalent capacitance and inductance, respectively, has an insignificant effect on the total power dissipation.

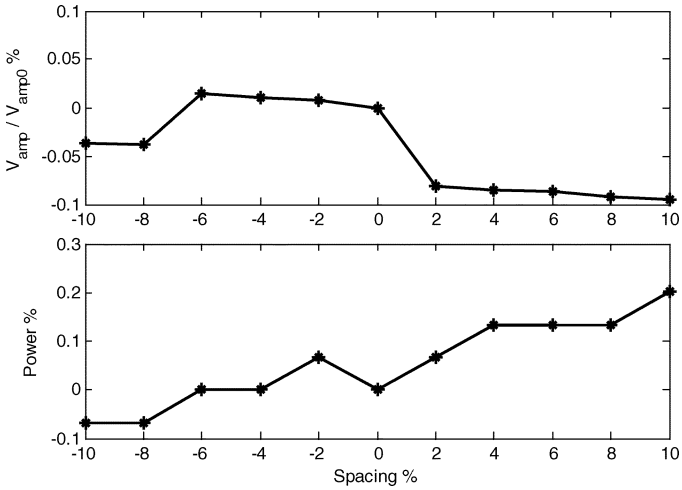


Fig. 24. Voltage swing and power consumption as a function of spacing variations between the signal and shield lines.

TABLE V
SENSITIVITY EVALUATION OF RESONANT H-TREE NETWORK

Category	Variation range	Voltage swing variations	Power consumption variations
R_g	±25%	-1.5 to 1.5%	-8 to 13%
W_{Ls}	±25%	-0.8 to 0.6%	-1.5 to 1.9%
C_d	±25%	-0.15 to 0.1%	0 to 0.14%
W_{signal}	±10%	-0.25 to 0%	-0.9 to 0.5%
$W_{shielding}$	±10%	-0.1 to 0%	-0.6 to 0.7%
Spacing	±10%	-0.1 to 0.01%	-0.08 to 0.2%

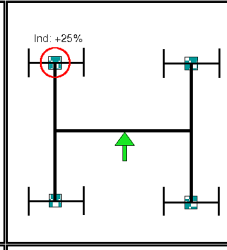
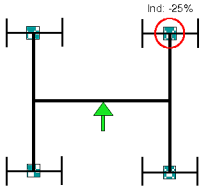
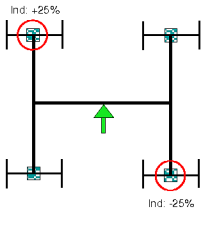
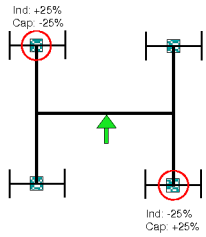
The space between the shield line and the signal lines determines the magnitude of the coupling capacitance, the mutual inductance, and the noise coupled to the signal line (see Fig. 10). With spacing variations, the H-tree network exhibits a voltage swing and power variations of about -0.1% to $+0.03\%$ and -0.08% to $+0.2\%$, respectively.

The spacing between the signal and shield lines does not significantly affect the performance of a resonant clock network. The shield lines around the H-tree interconnects should therefore be used to lower noise rather than increase the speed of the resonant H-tree network. Note, also, that as the spacing between the signal and shield lines increases, the capacitance of the structure decreases, resulting in increased power consumption, as depicted in Fig. 24. The different design criteria and variation characteristics presented in this subsection are summarized in Table V.

As predicted by theory and verified by OEA extraction tools, HENRY and METAL, and SpectreS simulations, the following trends are observed. As the width of the signal or shield lines increases, the resistance and inductance decreases while the capacitance increases. As the separation between the signal and shield lines increases, the resistance remains constant while the inductance increases and the capacitance decreases.

In order to explore the effects of multiple simultaneous variations on the performance of a resonant H-tree network, three simulation cases are considered, as shown in Fig. 25. The buffer

TABLE VI
FOUR CASES OF UNBALANCED INDUCTOR AND CAPACITOR VARIATIONS

	Case 1	Case 2	Case 3	Case 4
				
Voltage swing	0.84%	0.13%	0.98%	0.76%
Power consumption	-1.2%	-0.4%	-0.81%	-0.79%

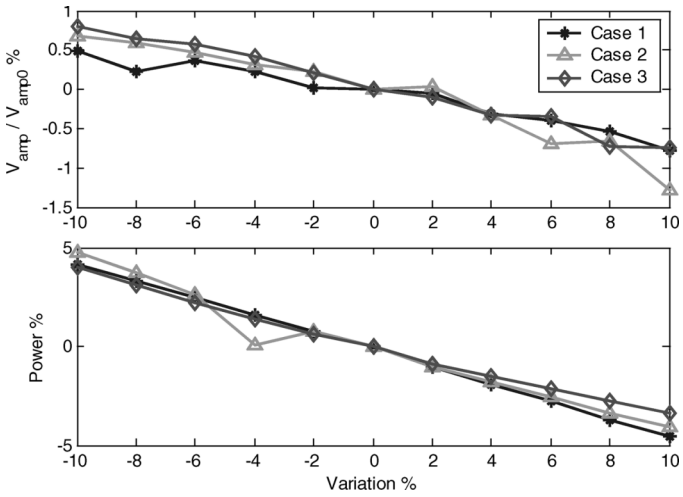


Fig. 25. Three cases of voltage swing and power consumption as a function of four simultaneous variations. Case 1: buffer output resistance, spiral inductors, capacitors, and signal line width are varied. Case 2: buffer output resistance, spiral inductors, capacitors, and shield line width are varied. Case 3: buffer output resistance, spiral inductors, capacitors, and spacing are varied.

output resistance, on-chip spiral inductors, and capacitors are varied simultaneously with the signal width (case 1), shield line width (case 2), or spacing (case 3).

The H-tree network exhibits the maximum voltage swing and power variations of about $\pm 1.3\%$ and $\pm 5\%$, respectively, (see Fig. 25) for all three cases. As expected, the dominant source of deviation (as illustrated in Fig. 19) from the optimal behavior of the resonant H-tree sector is due to variations in the driving buffer output resistance. The other parameters have a much smaller effect on the performance of the H-tree network. These results confirm that the nature of a resonant H-tree network is robust and relatively tolerant to process variations.

To explore the response of a resonant H-tree network to unbalanced on-chip inductor and capacitor variations, four cases are considered, as shown in Table VI. In the first case, only the upper left inductor width is increased by 25%. In the second case, only the width of the upper right inductor is decreased by 25%. In the third case, the left upper and right lower inductors widths are varied by 25% and -25%, respectively. Finally, in the fourth case, the left upper inductor width and capacitor are varied by 25% and -25%, respectively, while the lower right inductor width and capacitor are varied by -25% and 25%, respectively. The range of voltage swing and power consumption variations is 0.13% to 0.84% and -1.2% to -0.4%, respectively. These results demonstrate that, at least for this example, the H-tree sector is almost insensitive to highly unbalanced on-chip inductor and capacitor variations.

VI. CONCLUSION

Resonant H-tree clock distribution networks may be a suitable alternative to traditional clock distribution networks. By exploiting the resonance behavior, a significant decrease in power consumption can be achieved as compared to standard H-tree networks. A methodology is described for designing resonant H-tree clock distribution sectors. These H-tree structures form the basic building block of a resonant network. An accurate model is developed which utilizes a transmission line model to characterize high frequency effects. The high accuracy and analytic nature of the model enables the exploration of tradeoffs in the design of a resonant H-tree sector. The optimal on-chip inductors and capacitors as well as the maximum driving buffer output resistance are determined for a specific example circuit. This set of impedances produces the minimum power at the target clock frequency.

A case study demonstrating the proposed design methodology is described. A 5-GHz H-tree network exhibits significantly improved performance in terms of power consumption and voltage swing. A comparison to a nonresonant H-tree sector is also provided, exhibiting 84% lower power consumption. The major overhead as compared to a nonresonant network is the area. This overhead is due to the four inductors connected to the network. Minimizing the area occupied by these inductors is a topic for future research.

The sensitivity of a resonant H-tree sector to six design criteria is further explored. These design criteria include the buffer output resistance, on-chip inductor and capacitor size, and the signal and shield line width and spacing. Simulations demonstrate that a resonant H-tree sector exhibits acceptable robustness and relatively low sensitivity to process and environmental variations for a 5-GHz operating frequency. The maximum voltage swing and power dissipation are $+1.5\%$ and $+13\%$, respectively. These variations occur when the driving buffer output resistance varies by $\pm 25\%$. For the remaining parameters, the resonant H-tree sector exhibits insignificant

variations as compared to the optimal performance with no variations. Simultaneous process variations demonstrate that resonant clock networks are highly tolerant and robust. Finally, unbalanced inductor width and capacitor variations illustrate the insensitivity of a resonant H-tree clock distribution network to process variations.

APPENDIX A

An $ABCD$ matrix is composed for each section of the structure illustrated in Fig. 6. From transmission line theory, the $ABCD$ matrix for the entire structure is a product of the individual matrices. Hence, the $ABCD$ matrix for each section illustrated in Fig. 6 is

$$M_i = \begin{bmatrix} \cosh\gamma_i l_i & Z_{0i}\sinh\gamma_i l_i \\ \left(\frac{1}{Z_{0i}}\right)\sinh\gamma_i l_i & \cosh\gamma_i l_i \end{bmatrix} \forall i = 1,2,3,4 \quad \text{(A-1)}$$

where Z_{0i}, γ_i, and l_i are the characteristic impedance, propagation constant, and length, respectively, of the ith transmission line. These constants are given by

$$\gamma_i = \sqrt{\left(\frac{R_i}{2^i} + s\left(\frac{L_i}{2^i}\right)\right) s\left(2^i \cdot C_i\right)} \quad \text{(A-2)}$$

$$Z_{0i} = \sqrt{\frac{\frac{R_i}{2^i} + s\left(\frac{L_i}{2^i}\right)}{s\left(2^i \cdot C_i\right)}}. \quad \text{(A-3)}$$

The $ABCD$ matrix of the lumped series inductance, resistance, and capacitance at node 2 (see Fig. 6) is

$$M_s = \begin{bmatrix} 1 & 0 \\ Y_s & 1 \end{bmatrix} \quad \text{(A-4)}$$

where the admittance Y_s is

$$Y_s = \frac{s}{\left(\frac{L_s}{4}\right)\cdot s^2 + \left(\frac{R_s}{4}\right)\cdot s + \frac{1}{(4C_d)}}. \quad \text{(A-5)}$$

The $ABCD$ matrix of the effective lumped load at node 4 is

$$M_l = \begin{bmatrix} 1 & 0 \\ Y_l & 1 \end{bmatrix} \quad \text{(A-6)}$$

where the admittance Y_l is

$$Y_l = 16 \cdot C_l \cdot s. \quad \text{(A-7)}$$

The $ABCD$ matrix of the entire structure is given by (2) and repeated here for convenience

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = M_1 \cdot M_2 \cdot M_s \cdot M_3 \cdot M_4 \cdot M_l. \quad \text{(A-8)}$$

The constants a_0, a_1, and a_2 and the functions K, b_0, b_1, b_2, b_3, d_0, d_1, d_2, and d_3 in (3) and (4) are extracted from the $ABCD$ matrix in (A8). In order to represent (A8) in a convenient manner, certain additional auxiliary functions are provided. The constants a_0, a_1, and a_2 represent the on-chip capacitor, effective series resistance, and on-chip inductor, respectively

$$a_2 = L_s \quad a_1 = R_s \quad a_0 = \frac{1}{C_d}. \quad \text{(A-9)}$$

The auxiliary functions are defined as

$$k_1 \equiv \cosh\gamma_1 l_1 \cdot \cosh\gamma_2 l_2 + \left(\frac{Z_{01}}{Z_{02}}\right)\cdot \sinh\gamma_1 l_1 \cdot \sinh\gamma_2 l_2 \quad \text{(A-10a)}$$

$$k_2 \equiv Z_{02} \cdot \cosh\gamma_1 l_1 \cdot \sinh\gamma_2 l_2 + Z_{01} \cdot \sinh\gamma_1 l_1 \cdot \cosh\gamma_2 l_2 \quad \text{(A-10b)}$$

$$k_3 \equiv \cosh\gamma_3 l_3 \quad \text{(A-10c)}$$

$$k_4 \equiv \cosh\gamma_4 l_4 \quad \text{(A10d)}$$

$$k_5 \equiv \sinh\gamma_3 l_3 \quad \text{(A-10e)}$$

$$k_6 \equiv \sinh\gamma_4 l_4 \quad \text{(A-10f)}$$

and an additional set of functions is defined as

$$p_1 \equiv \left(\frac{1}{Z_{01}}\right)\cdot \sinh\gamma_1 l_1 \cdot \cosh\gamma_2 l_2 + \left(\frac{1}{Z_{02}}\right)\cdot \cosh\gamma_1 l_1 \cdot \sinh\gamma_2 l_2 \quad \text{(A-11a)}$$

$$p_2 \equiv \left(\frac{Z_{02}}{Z_{01}}\right)\cdot \sinh\gamma_1 l_1 \cdot \sinh\gamma_2 l_2 + \cosh\gamma_1 l_1 \cdot \cosh\gamma_2 l_2. \quad \text{(A-11b)}$$

Finally, K, b_0, b_1, b_2, b_3, d_0, d_1, d_2, and d_3 in (3) and (4) are

$$K \equiv \frac{1}{(Z_{03}\cdot Z_{04})} \quad \text{(A-12)}$$

$$b_3 \equiv C_l \cdot a_2 \cdot Z_{03} \cdot Z_{04} \cdot (1 + Z_{04}\cdot k_1 \cdot k_3 \cdot k_6 + \left(\frac{Z_{04}}{Z_{03}}\right)\cdot k_2 \cdot k_5 \cdot k_6 + Z_{03}\cdot k_1 \cdot k_4 \cdot k_5) \quad \text{(A-13a)}$$

$$b_2 \equiv Z_{04}\cdot a_2 \cdot k_4 \cdot (k_2 \cdot k_5 + Z_{03}\cdot k_1 \cdot k_3) + \mathrm{C}_l \cdot Z_{04} \cdot k_2 \cdot k_5 \left(Z_{03}^2 \cdot k_4 + Z_{04}\cdot a_1 \cdot k_6\right) + \mathrm{C}_l \cdot Z_{03} \cdot Z_{04}^2 \cdot k_3 \cdot k_6 \cdot (a_1 \cdot k_1 + k_2) + Z_{03}\cdot(k_2\cdot k_3 + Z_{03}\cdot k_1\cdot k_5)\cdot(k_6 \cdot a_2 + \mathrm{C}_l \cdot Z_{04}\cdot a_1 \cdot k_4) \quad \text{(A-13b)}$$

$$b_1 \equiv C_l \cdot Z_{04}\cdot a_0 \cdot k_5 \left(Z_{04}\cdot k_2 \cdot k_5 + Z_{03}^2 \cdot k_1 \cdot k_4\right) + C_l \cdot Z_{03}\cdot Z_{04}\cdot a_0 \cdot k_3 \cdot (k_2 \cdot k_4 + Z_{04}\cdot k_1 \cdot k_6) + \mathrm{Z}_{03}\cdot k_2 \cdot k_6 \cdot \left(Z_{03}\cdot k_5 + a_1 \cdot k_3 + \frac{(Z_{04}\cdot k_3 \cdot k_4)}{k_6}\right) + a_1 \cdot \left(\mathrm{Z}_{04}\cdot k_4 \cdot (k_2 \cdot k_5 + k_1 \cdot k_3) + Z_{03}^2 \cdot k_1 \cdot k_5 \cdot k_6\right) \quad \text{(A-13c)}$$

$$b_0 \equiv Z_{04}\cdot a_0 \cdot k_4 \cdot (Z_{03}\cdot k_1 \cdot k_3 + k_2 \cdot k_5) + Z_{03}\cdot a_0 \cdot k_6 \cdot (k_2 \cdot k_3 + k_1 \cdot k_5) \quad \text{(A-13d)}$$

and

$$d_3 \equiv C_l \cdot Z_{04}^2 \cdot a_2 \cdot k_6 \cdot (p_2 \cdot k_5 + Z_{03}\cdot p_1 \cdot k_3) + C_l \cdot Z_{03}\cdot Z_{04}\cdot a_2 \cdot k_4 \left(Z_{03}\cdot p_1 \cdot k_5 + p_2 \cdot k_3\right) \quad \text{(A-14a)}$$

$$d_2 \equiv \mathrm{C}_l \cdot Z_{04}\cdot a_1 \cdot p_2 \cdot (Z_{04}\cdot k_5 \cdot k_6 + Z_{03}\cdot k_3 \cdot k_4) + \mathrm{Z}_{04}\cdot a_2 \cdot k_4 \cdot (Z_{03}\cdot p_1 \cdot k_3 + p_2 \cdot k_5) + \mathrm{Z}_{03}\cdot a_2 \cdot k_6 \cdot (Z_{03}\cdot p_1 \cdot k_5 + p_2 \cdot k_3) + C_l\cdot Z_{03}\cdot Z_{04}\cdot(a_1\cdot p_1 + p_2)\cdot(Z_{04}\cdot k_3 \cdot k_6 + Z_{03}\cdot k_4 \cdot k_5) \quad \text{(A-14b)}$$

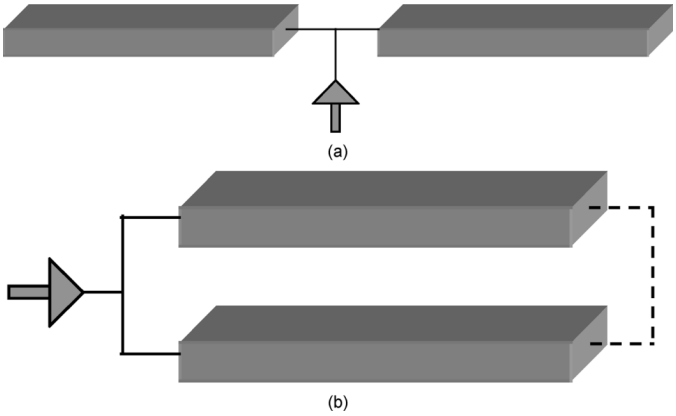


Fig. 26. First level of the resonant H-tree sector. (a) Two identical interconnects driven by a buffer. (b) Two symmetric interconnects effectively shorted.

$$d_1 \equiv C_l \cdot Z_{04}^2 \cdot a_0 \cdot k_6 \cdot (Z_{03} \cdot p_1 \cdot k_3 + p_2 \cdot k_5) + C_l \cdot Z_{03} \cdot Z_{04} \cdot a_0 \cdot k_4 \cdot (Z_{03} \cdot p_1 \cdot k_5 + p_2 \cdot k_3) + \mathrm{a}_1 \cdot p_2 \cdot (Z_{04} \cdot k_4 \cdot k_5 + Z_{03} \cdot k_3 \cdot k_6) + \mathrm{Z}_{03} \cdot (a_1 \cdot p_1 + p_2) \cdot (Z_{04} \cdot k_3 \cdot k_4 + Z_{03} \cdot k_5 \cdot k_6) \quad \text{(A-14c)}$$

$$d_0 \equiv Z_{04} \cdot a_0 \cdot k_4 \cdot (p_2 \cdot k_5 + Z_{03} \cdot p_1 \cdot k_3) + \mathrm{Z}_{03} \cdot a_0 \cdot k_6 \cdot (\mathrm{Z}_{03} \cdot p_1 \cdot k_5 + p_2 \cdot k_3). \quad \text{(A-14d)}$$

Appendix B

The input clock signal driving the resonant H-tree clock sector is a square periodic waveform

$$V_{\mathrm{in}}(t) = \begin{cases} \dfrac{t}{\tau} V_{\mathrm{dd}}, & nT \le t < nT + \tau \quad \text{(B-1a)} \\ V_{\mathrm{dd}}, & nT + \tau \le t < \left(n + \dfrac{1}{2}\right) T \quad \text{(B-1b)} \\ \left(1 - \dfrac{t}{\tau} + \dfrac{T}{2\tau}\right) V_{\mathrm{dd}}, & \left(n + \dfrac{1}{2}\right) T \le t < \left(n + \dfrac{1}{2}\right) T + \tau \quad \text{(B-1c)} \\ 0, & \left(n + \dfrac{1}{2}\right) T + \tau \le t < (n+1) T \quad \text{(B-1d)} \end{cases}$$

where T is the period of $V_{\mathrm{in}}(t)$, n is an integer, and τ is the transition time. In the case study described in Section IV, T and τ are 200 and 40 ps, respectively, and $V_{\mathrm{dd}} = 1.8$ V. Substituting (B-1) into (8)

$$V_{\mathrm{rms},g} = \sqrt{1.404}\ \mathrm{V}. \quad \text{(B-2)}$$

Appendix C

Assuming that the interconnect lines between each pair of nodes are effectively in parallel (see Figs. 5 and 26), the capacitance per unit length is increased by a factor of two, while the resistance and inductance per unit length is decreased by a factor of two at each level of the hierarchy. To justify this assumption, consider the interconnect model of Fig. 26(b) as depicted in Fig. 27.

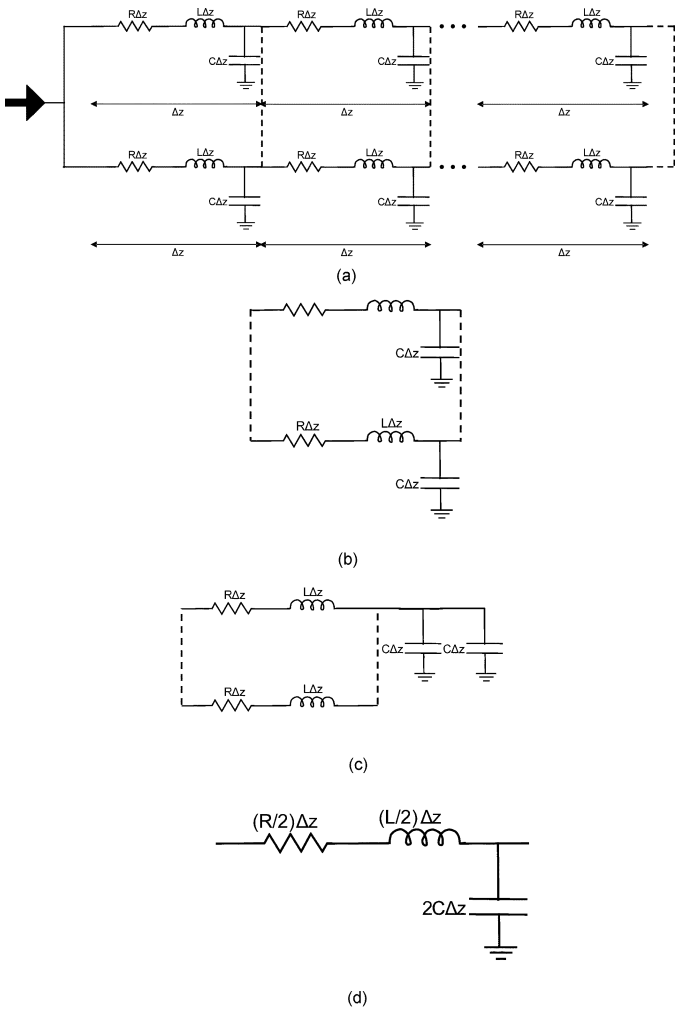


Fig. 27. Distributed model of two shorted interconnects. (a) Model of two identical shorted interconnects. (b) Two shorted infinitesimally small sections. (c) Two shorted sections in a different configuration. (d) Equivalent model of two shorted sections.

Since all of the nodes in Fig. 27(a) are symmetric, the waveforms at these nodes are identical. As a result, the infinitesimally small sections can be assumed to be effectively shorted (as illustrated by the dashed lines). The total impedance of each of the two shorted sections is determined from the circuit depicted in Fig. 27(c). The total shunted capacitance is

$$C_{\mathrm{tot}} = (2C)\,\Delta z \quad \text{(C-1)}$$

while the total series resistance and inductance is

$$Z_{R,L,\mathrm{tot}} = \frac{1}{\left(\frac{1}{R\Delta z + sL\Delta z} + \frac{1}{R\Delta z + sL\Delta z}\right)} = \left(\frac{R}{2}\right)\Delta z + s\left(\frac{L}{2}\right)\Delta z. \quad \text{(C-2)}$$

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