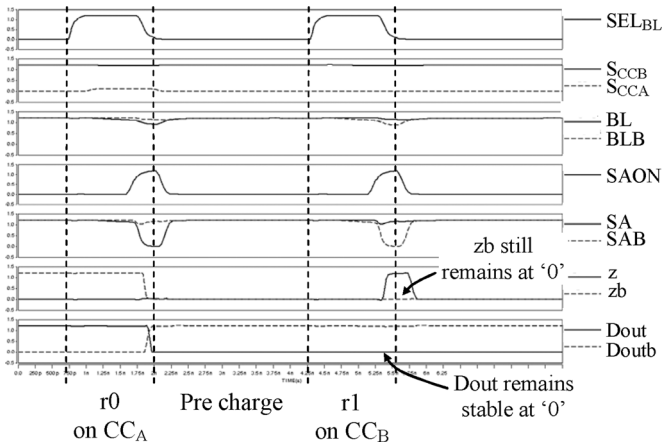

Fig. 6. Waveforms of $\langle 0r0, 1r1/1/0 \rangle$ simulation (Df4).

B. March Test Solution

As shown previously, a d2cIRF2 may occur in the presence of defects Df4--Df9. Such a faulty behavior is sensitized and observed with specific sequences of read operations:

1) "r0r1" for defects belonging to group 1;
2) "r1r0" for defects belonging to group 2.

Here both operations have to be performed on two distinct core cells sharing the same sense amplifier.

As previously done, we can try to find less stringent detection sequences. Nevertheless, as defects impact pull up or pull down of *z* and *zb* nodes, any read or write operation may mask the fault effect.

Consequently, we have to find a March algorithm that contains two successive read operations with opposite data value. The March iC- algorithm described in Section IV is able to detect such faulty behavior. In fact, if we consider element M5 (see Fig. 5), the succession of operations applied at different addresses is

$$\begin{array}{cccccc} (\mathrm{r0}) & (\mathrm{r1}) & (\mathrm{r0}) & (\mathrm{r1}) & \ldots \\ \mathrm{Add1} & \mathrm{Add2} & \mathrm{Add3} & \mathrm{Add4} & \ldots . \end{array}$$

Two successive read operations have to be applied on the same sense amplifier. The simplest way to do that is also by using the line after line or the column after column addressing order.

VI. Conclusion

In this paper, we have analyzed and characterized the effects of resistive-open defects that may occur in the sense amplifiers of SRAMs. We have shown that several resistive-open defects may lead to new types of dynamic behavior. These faulty behaviors have been modeled as a d2cIRF1 and d2cIRF2. Such fault models are a consequence of failures in the sense amplifier that prevent it from performing any read operations (in case of type 1) or only a single type of read operation (either r0 or r1 in case of type 2). We have performed electrical simulations to give a complete understanding of such faulty behavior. Moreover, we have shown that the March C- with a specific datum (alternated datum value) and a specific addressing order (line after line or column after column) is able to detect all d2cIRFs that may affect the sense amplifiers of an SRAM.

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Identification of Dominant Noise Source and Parameter Sensitivity for Substrate Coupling

Emre Salman, Eby G. Friedman, Radu M. Secareanu, and Olin L. Hartin

***Abstract*—A simple, yet physically intuitive macrolevel model is presented to identify the dominant substrate coupling mechanism at the early stages of the design process, while simultaneously considering multiple parameters. Furthermore, the sensitivity of substrate noise to these parameters is evaluated, demonstrating the nonmonotonic dependence of noise on rise time. The design implications of the proposed analysis are discussed, identifying the preferred noise reduction technique for a specific set of operating points.**

***Index Terms*—Dominant substrate noise source, mixed-signal circuits, substrate noise coupling.**

I. Introduction

The increasing demand for higher performance and reduced cost is a primary driving force for integrating digital, analog, and RF circuits onto the same monolithic substrate. Single-die RF transceivers implemented in deep submicrometer technologies are common in modern wireless applications [1].

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Substrate coupling continues to be a primary concern for these mixed-signal systems-on-chips (SoCs) where sensitive analog/RF circuits coexist with aggressor digital circuits on the same substrate [2]. The baseband digital circuit injects noise into the substrate through three primary mechanisms [3]: 1) coupling from the source/drain junction capacitances of the transistors during switching; 2) coupling from the power and ground networks of the digital circuit; and 3) impact ionization, which is negligible as compared to the first two mechanisms [3]. The relative contribution of the first two mechanisms, however, have not been quantified in a sufficiently accurate manner.

A macrolevel model is presented to evaluate the dominant substrate coupling mechanism in the early stages of the design process, while considering multiple circuit parameters such as the number of simultaneously switching gates, rise time, on-chip decoupling capacitance, package and on-chip parasitic inductance and resistance, substrate resistance, substrate contact density, and the physical distance between the aggressor and victim blocks. Identification of the dominant noise coupling mechanism helps in comparing various substrate noise reduction techniques to determine the preferable technique. Furthermore, the sensitivity of substrate noise as a function of rise time and number of switching gates is evaluated. Design implications of the dominant noise source and sensitivity analysis are discussed.

The rest of the paper is organized as follows. Models to estimate the peak-to-peak substrate noise are presented in Section II. These expressions are used in Section III to identify the dominant noise generation mechanism. In Section IV, a sensitivity analysis validating the effects of these parameters on the substrate noise is presented. The design implications of these results are discussed in Section V, and the paper is concluded in Section VI.

II. Substrate Model to Estimate Noise

Coupling from the noisy ground network and source/drain junction coupling are considered to be the two primary noise generation mechanisms since the coupling from the power network is isolated due to the n-well capacitance. Specifically, ground coupling dominates the power coupling until a sufficiently high frequency is reached, beyond which both mechanisms affect the noise similarly, as described in [4].

A high-resistivity non-epi substrate is assumed to provide enhanced isolation making the model applicable to mixed-signal circuits. Note that the model of the substrate is resistive since the dielectric characteristics are negligible for frequencies below about 10 GHz for a high-resistivity substrate [5]. Models for ground bounce coupling and source/drain junction coupling for a single switching gate, and for multiple gates are described, respectively, in Sections II-A and II-B. Validation of the model is described in Section II-C.

A. Substrate Coupling for a Single Switching Gate

Noise on the ground network resistively couples into the substrate through the substrate contacts. The ground noise is quantified, assuming that the substrate network does not affect the ground noise due to the high impedance of the substrate as compared to the ground network. In Fig. 1, L_p, R_p, and L_g, R_g represent, respectively, the package and on-chip parasitic impedances of the power and ground network. C_d is the on-chip decoupling capacitor and R_d is the effective series resistance of the capacitor. The load circuit is represented by a current source with a rise time $(t_r)_i$ and peak current $(I_{\mathrm{swi}})_p$. The substrate resistance between the contact and bulk of the device is represented by R_{cb}. R_{dist} represents the equivalent substrate resistance between the bulk and the victim node of the sensitive analog circuit. R_{vc} is the equivalent substrate resistance between the victim node and the analog contact. Note that the victim node refers to the bulk node within the victim device. R_{ang} and L_{ang} represent the parasitic impedance of the analog ground network.

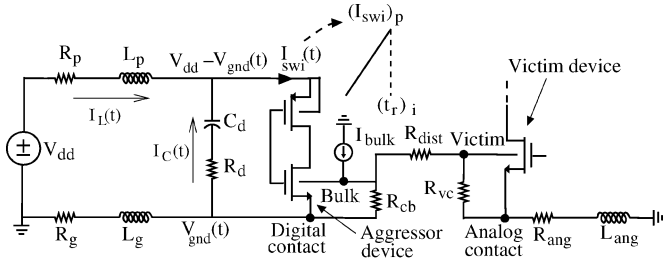

Fig. 1. Equivalent model to estimate ground coupling and source/drain junction coupling for a single switching gate.

The current provided by the decoupling capacitance $I_C(t)$ and the current flowing through the parasitic inductance $I_L(t)$ from the power supply are, respectively

$$I_C(t) = -C_d \frac{\partial V_C}{\partial t} \tag{1}$$

$$I_L(t) = \frac{1}{L_g} \int_0^t V_L(t) \partial t \tag{2}$$

where $V_C(t)$ and $V_L(t)$ are, respectively

$$V_C(t) = V_{\mathrm{dd}} - 2V_{\mathrm{gnd}}(t) + I_C(t)R_d \tag{3}$$

$$V_L(t) = V_{\mathrm{gnd}}(t) - I_L(t)R_p. \tag{4}$$

Assuming $R_p = R_g$, $L_p = L_g$, and a ramp function for the noise $V_{\mathrm{gnd}}(t) = [(V_{\mathrm{gnd}})_p/(t_r)_v]t$, where $(t_r)_v$ is the rise time and $(V_{\mathrm{gnd}})_p$ is the peak ground noise voltage, the capacitive and inductive currents are obtained by replacing, respectively, (3) in (1) and (4) in (2)

$$I_C(t) = (V_{\mathrm{gnd}})_p \left[\frac{2C_d}{(t_r)_v} \left(1 - e^{-t/(R_d C_d)} \right) \right] \tag{5}$$

$$I_L(t) = (V_{\mathrm{gnd}})_p \left[\frac{t}{(t_r)_v R_g} - \frac{L_g}{(t_r)_v R_g^2} \left(1 - e^{-t/\frac{L_g}{R_g}} \right) \right]. \tag{6}$$

Assuming the peak noise occurs when the switching current reaches the peak, e.g., $(t_r)_v = (t_r)_i = t_r$ and $I_C(t_r) + I_L(t_r) = (I_{\mathrm{swi}})_p$, the peak ground noise at $t = t_r$ can be expressed as

$$(V_{\mathrm{gnd}})_p = \frac{(I_{\mathrm{swi}})_p R_g^2 t_r}{2C_d R_g^2 (1 - e^{-t_r/(R_d C_d)}) - L_g \left(1 - e^{-t_r/\frac{L_g}{R_g}} \right) + R_g t_r}. \tag{7}$$

If the circuit is underdamped, oscillations occur due to a parallel combination of the parasitic inductance and the decoupling capacitor. In this case, the peak-to-peak ground noise voltage is

$$(V_{\mathrm{gnd}})_{\mathrm{pp}} = (V_{\mathrm{gnd}})_p [1 + e^{-\pi\zeta/\sqrt{1-\zeta^2}}] \tag{8}$$

where $\zeta = [(2R_g + R_d)/2]\sqrt{C_d/2L_g}$ is the damping factor. The substrate noise at the victim node due to ground coupling can be approximated as

$$(V_{\mathrm{s-gnd}})_{\mathrm{pp}} \approx \frac{(V_{\mathrm{gnd}})_{\mathrm{pp}}}{R_{\mathrm{cb}} + R_{\mathrm{dist}} + R_{\mathrm{vc}}} \left(R_{\mathrm{ang}} + R_{\mathrm{vc}} + \frac{L_{\mathrm{ang}}}{t_r} \right). \tag{9}$$

Noise couples into the substrate through the source/drain junction capacitance of the devices during switching. This noise source is modeled as a current source from within the bulk of a device with a peak current of $(I_{\mathrm{bulk}})_p$ and a rise time of t_r (which is assumed to be equal to

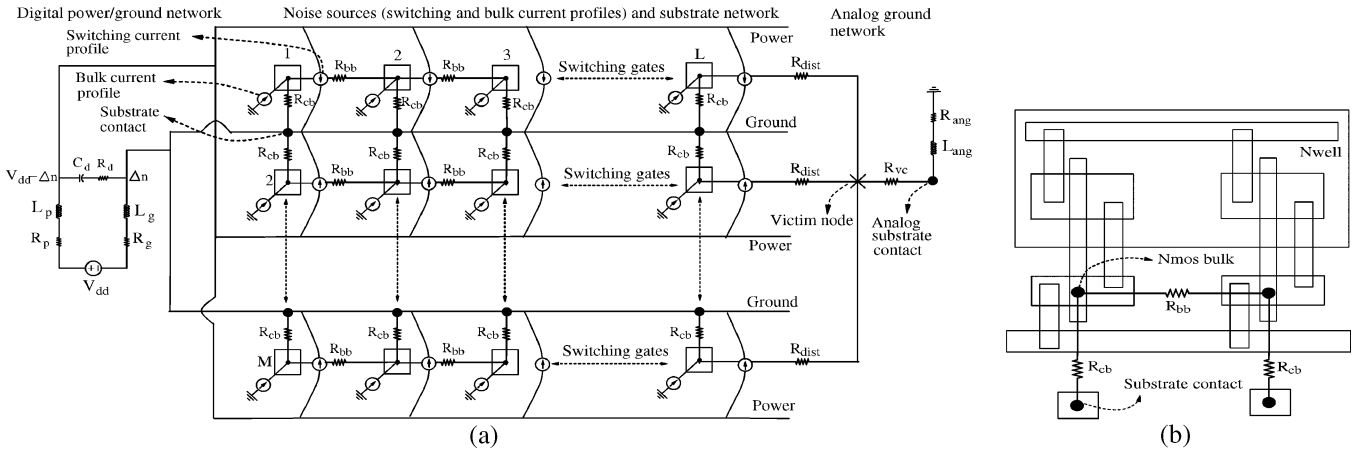

Fig. 2. Model for analysis and extraction. (a) Equivalent circuit model to estimate substrate noise for multiple switching gates. (b) Layout of two inverters to extract the substrate resistances $R_{\rm bb}$ and $R_{\rm cb}$.

the rise time of the switching current). The substrate noise at the victim node due to source/drain junction coupling can be approximated as

$$(V_{\rm s-bulk})_p \approx (I_{\rm bulk})_p \frac{R_{\rm cb}}{R_{\rm cb}+R_{\rm dist}+R_{\rm vc}} \times \left(R_{\rm ang}+R_{\rm vc}+\frac{L_{\rm ang}}{t_r}\right). \quad (10)$$

The total noise at the victim node is the summation of (9) and (10)

$$(V_{\rm s-total})_{\rm pp} \approx (V_{\rm s-gnd})_{\rm pp} + (V_{\rm s-bulk})_p. \quad (11)$$

TABLE I
EXTRACTED PARAMETERS CHARACTERIZING AN INVERTER

Parameter	Value
$(W/L)_{nmos}$	0.31 μm / 0.1 μm
$(W/L)_{pmos}$	0.44 μm / 0.1 μm
$(I_{swi-g})_p$	57.5 μA
$(I_{bulk-g})_p$	6.7 μA
R_{bb}	16.8 kΩ
R_{cb}	10.7 kΩ
R_{dist}	40 kΩ
R_{vc}	660 Ω

B. Substrate Coupling Model for Multiple Switching Gates

The model introduced for a single gate is extended to analyze the effect of simultaneously switching gates on the substrate noise characteristics. Each macromodel for a switching gate consists of two current sources, $I_{\rm swi-g}$ and $I_{\rm bulk-g}$, to represent the switching and bulk currents, respectively, and a substrate resistance $R_{\rm cb}$ between the contact and bulk, assuming the gate has a substrate contact.

These gates are connected as shown in Fig. 2(a) to obtain a model of substrate coupling for multiple gates, assuming the aggressor consists of standard cells. For a given number of switching gates n, L and M gates are placed in the horizontal and vertical directions, respectively, such that $L \times M = n$ and the resulting rectangle is as close as possible to a square in terms of the physical layout of the aggressor circuit. The bulk node of each gate located along the horizontal direction is connected through a substrate resistance $R_{\rm bb}$. The bulk of the gates located along the vertical direction which share the same local ground line is vertically connected through the resistance $2 \times R_{\rm cb}$. The ground noise $(V_{\rm gnd})_{\rm pp}$ at each substrate contact location is determined from (9) where the total peak current scales to $n(I_{\rm swi-g})_p$. Note that the switching gates are assumed in this analysis to be identical. The peak-to-peak substrate noise at the victim node $(V_{\rm victim})_{\rm pp}$ is the summation of the noise due to each contact and bulk current source

$$(V_{\rm victim})_{\rm pp} = [(V_{\rm gnd})_{\rm pp}TF_{c1} + \ldots + (V_{\rm gnd})_{\rm pp}TF_{\rm cn}] + [(I_{\rm bulk1})_{\rm pp}TF_{ib1} + \ldots + (I_{\rm bulkn})_{\rm pp}TF_{\rm ibn}] \quad (12)$$

where $TF_{c1},\ldots,TF_{\rm cn}$ represent the voltage noise transfer function from the corresponding contact location to the victim node, and $TF_{\rm ib1},\ldots.TF_{\rm ibn}$ represent the current noise transfer function from the corresponding bulk current source to the victim node. These transfer functions are determined from the resistive substrate network, as illustrated in Fig. 2(a). This model is used to quantify various noise sources and evaluate the dominant coupling mechanism.

C. Extraction of Parameters and Model Validation

An industrial 90 nm CMOS technology with a lightly doped (non-epi type) substrate is used to extract the parameters applied in this model. An inverter with NMOS size, W/L = 0.31 μm/0.1 μm, and PMOS size, W/L = 0.44 μm/0.1 μm, is used. The layout of the two cells, as shown in Fig. 2(b), is extracted using Assura and SubstrateStorm [6]. Related parameters are listed in Table I. The peak switching and bulk currents are obtained when the cell is driven by a ramp input with a 100 ps rise and fall time that drives an identical gate. The substrate resistances $R_{\rm dist}$ and $R_{\rm vc}$ are similarly extracted assuming the victim node is located 100 μm from the aggressor circuit, and placed within a $p+$ guard ring with 15 analog substrate contacts.

At a certain number of switching gates, the estimated peak-to-peak substrate noise is characterized by (12). This expression is compared with SPICE in Fig. 3, where $n = 200$, $L_g = L_{\rm ang} = 1$ nH, $C_d = 10$ pF, $R_g = R_{\rm ang} = 2.2\ \Omega$, and $R_d = 0.1\ \Omega$. The model accurately captures the nonmonotonic dependence of substrate noise on rise time, exhibiting a maximum error of 18.4%. Note that this error is due to approximating the noise as a ramp function (which is a better assumption for smaller rise times) and the feedback effect of the nonlinear devices, which is not captured in the model.

III. DOMINANT SUBSTRATE NOISE COUPLING MECHANISM

The models and expressions for ground and source/drain coupling are used in this section to evaluate the dominant substrate noise generation mechanism. Based on the model shown in Fig. 2(a), a specific number of switching gates exists beyond which the ground coupling

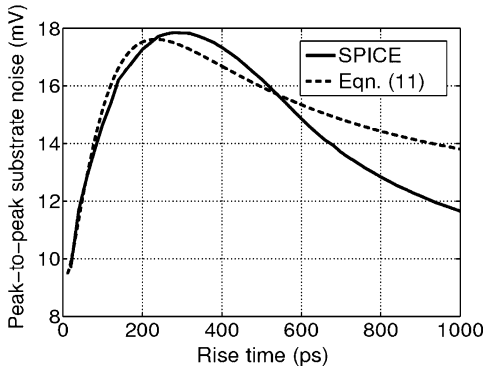

Fig. 3. Comparison of peak-to-peak substrate noise as a function of the rise time obtained from SPICE and (12).

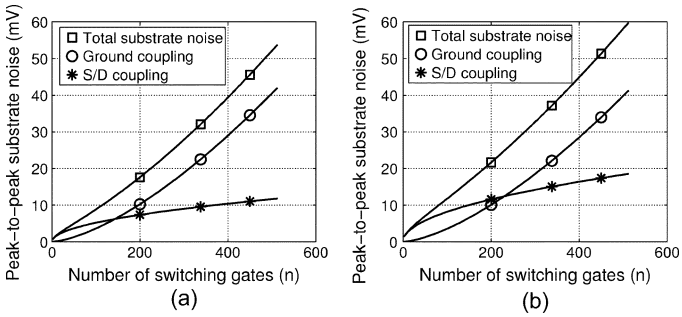

Fig. 4. Number of simultaneously switching gates versus substrate noise as predicted by (12) when $(t_r)_i = 250$ ps, $L_g = 1$ nH, $C_d = 10$ pF, $R_g = 2.2\ \Omega$, $R_d = 0.1\ \Omega$, $R_{\rm bb} = 16.8\ {\rm k}\Omega$, $R_{\rm cb} = 10.7\ {\rm k}\Omega$, $R_{\rm dist} = 40\ {\rm k}\Omega$, $R_{\rm vc} = 660\ \Omega$, $R_{\rm ang} = 2.2\ \Omega$, and $L_{\rm ang} = 1$ nH. (a) Each gate has a substrate contact. (b) Two gates share one substrate contact.

exceeds the source/drain coupling. As a greater number of gates simultaneously switch, the ground noise on each substrate contact increases due to the additional supply current. The ground coupling component of the substrate noise therefore increases with larger number of switching gates. Furthermore, each switching gate injects noise due to junction capacitances, increasing the source/drain junction coupling mechanism. Alternatively, a particular contact behaves as a noise filter for source/drain junction coupling and ground coupling from the other contacts, reducing the overall substrate noise.

The source/drain coupling, ground coupling, and the total noise versus the number of switching gates are shown in Fig. 4. For a small number of switching gates, source/drain coupling dominates over ground coupling. As the number of switching gates increases, ground coupling increases at a faster rate as compared to source/drain coupling due to an increase in the overall supply current and number of contacts. The noise injected from the source/drain coupling is primarily filtered by these contacts rather than propagated toward the victim node. Those gates closest to the victim node therefore cause the source/drain coupling noise. At a certain number of switching gates, the ground coupling becomes larger than the source/drain coupling. Note that this crossover number is higher in Fig. 4(b) where the two gates share one contact as opposed to Fig. 4(a) where a contact exists for each gate.

Ground coupling starts to dominate source/drain coupling beyond this crossover point. For large-scale circuits with a significant number of switching gates, ground coupling is expected to be the dominant substrate noise generation mechanism. Source/drain coupling is effective only for those small number of gates that are sufficiently close to the victim node. For localized noise analysis, however, the effect

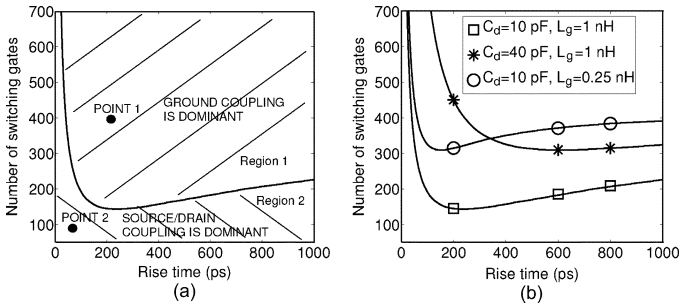

Fig. 5. Dominance regions for source/drain coupling and ground coupling. (a) Regions 1 and 2 represent, respectively, the area where ground and source/drain coupling is dominant. The operating parameters are $L_g = 1$ nH, $C_d = 10$ pF, $R_g = 2.2\ \Omega$, $R_d = 0.1\ \Omega$, $R_{\rm bb} = 16.8\ {\rm k}\Omega$, $R_{\rm cb} = 10.7\ {\rm k}\Omega$, $R_{\rm dist} = 40\ {\rm k}\Omega$, $R_{\rm vc} = 660\ \Omega$, $R_{\rm ang} = 2.2\ \Omega$, and $L_{\rm ang} = 1$ nH. (b) Effect of decoupling capacitance and parasitic inductance on the dominance regions.

of source/drain coupling cannot be neglected. Note that the specific number of switching gates where the crossover occurs is highly dependent on the rise time, parasitic inductance, and decoupling capacitance.

These crossover points are numerically determined at each rise time using (12) to quantify and compare the regions where ground and source/drain coupling are dominant. The results are illustrated in Fig. 5(a). For each rise time, the number of switching gates at which ground coupling is equal to source/drain coupling is illustrated. Hence, the area above the curve represents the region where ground coupling is dominant (region 1) and, correspondingly, source/drain coupling is dominant under the curve (region 2).

For sufficiently small rise times, the ground noise is relatively low since the decoupling capacitance effectively reduces the noise. The number of switching gates where the crossover occurs is therefore greatest for small rise times. This crossover point decreases as the rise time increases and is smallest at $t_r \approx 2\sqrt{(L_g C_d)}$ where the ground noise is greatest, maximizing the area of region 1. As the rise time further increases, the ground noise decreases due to lower $L\ di/dt$ noise, increasing the area of region 2. Note that for small rise times or, equivalently, at higher operating frequencies, source/drain coupling becomes the significant noise injection mechanism.

The same graph is obtained at a different decoupling capacitance and parasitic inductance to evaluate the effect of these parameters on the dominant noise generation mechanism, as illustrated in Fig. 5(b). As the parasitic inductance decreases or the decoupling capacitor increases, the area of region 1 decreases while the area of region 2 increases. Thus, for circuits with flip-chip packages and sufficiently high decoupling capacitance, source/drain coupling cannot be neglected and can become the dominant substrate noise generation mechanism.

IV. Parameter Sensitivity

As described in the previous section, the dominant noise injection mechanism is determined by multiple circuit parameters. Correspondingly, the noise sensitivity to these parameters varies with respect to the operating point and the dominant noise source. As such, a particular circuit-level noise reduction technique may be more efficient as compared to other techniques for a certain set of operating points. The normalized noise sensitivity as a function of rise time and number of switching gates is evaluated based on the model illustrated in Fig. 1. The normalized sensitivity of the substrate noise to a parameter p_i is

$$S_{p_i}^{(V_{\rm s-total})_{\rm pp}} = \lim_{\Delta p_i \to 0} \frac{\frac{\Delta (V_{\rm s-total})_{\rm pp}}{(V_{\rm s-total})_{\rm pp}}}{\frac{\Delta p_i}{p_i}} = \frac{p_i}{(V_{\rm s-total})_{\rm pp}} \frac{\partial (V_{\rm s-total})_{\rm pp}}{\partial p_i} \tag{13}$$

TABLE II
EFFECT OF THE DECOUPLING CAPACITANCE, PARASITIC INDUCTANCE, AND SUBSTRATE CONTACT DENSITY ON REDUCING THE PEAK-TO-PEAK SUBSTRATE NOISE AT VARIOUS OPERATING POINTS

Rise time (ps)	Number of switching gates								
	50			200			700		
	$C_d = 10$ pF	$C_d = 20$ pF	Reduction	$C_d = 10$ pF	$C_d = 20$ pF	Reduction	$C_d = 10$ pF	$C_d = 20$ pF	Reduction
70	4.5 mV	4.1 mV	8.9%	13.5 mV	10.4 mV	22.9%	55.5 mV	34.4 mV	38%
200	4.9 mV	4.5 mV	8.2%	17.5 mV	13.5 mV	22.8%	83.6 mV	56 mV	33%
400	4.8 mV	4.5 mV	6.3%	16.7 mV	14.3 mV	14.4%	78 mV	61.5 mV	21.2%
800	4.6 mV	4.4 mV	4.3%	14.4 mV	13.3 mV	7.6%	62.6 mV	55.1 mV	12%
	$L_g = 1$ nH	$L_g = 0.5$ nH	Reduction	$L_g = 1$ nH	$L_g = 0.5$ nH	Reduction	$L_g = 1$ nH	$L_g = 0.5$ nH	Reduction
70	4.5 mV	4.4 mV	2.2%	13.5 mV	12.6 mV	6.7%	55.5 mV	49.2 mV	11.4%
200	4.9 mV	4.6 mV	6.1%	17.5 mV	14.3 mV	18.3%	83.6 mV	61.7 mV	26.2%
400	4.8 mV	4.4 mV	8.3%	16.7 mV	13.4 mV	19.8%	78 mV	55.2 mV	29.2%
800	4.6 mV	4.3 mV	6.5%	14.4 mV	12.3 mV	14.6%	62.6 mV	47.7 mV	23.8%
	$d_{sc} = \frac{0.5}{gate}$	$d_{sc} = \frac{1}{gate}$	Reduction	$d_{sc} = \frac{0.5}{gate}$	$d_{sc} = \frac{1}{gate}$	Reduction	$d_{sc} = \frac{0.5}{gate}$	$d_{sc} = \frac{1}{gate}$	Reduction
70	6.6 mV	4.5 mV	31.8%	17.7 mV	13.5 mV	23.7%	63 mV	55.5 mV	11.9%
200	7.1 mV	4.9 mV	31%	21.6 mV	17.5 mV	19%	90.5 mV	83.6 mV	7.6%
400	6.9 mV	4.8 mV	30.4%	20.7 mV	16.7 mV	19.3%	85 mV	78 mV	8.2%
800	6.7 mV	4.6 mV	31.3%	18.5 mV	14.4 mV	22.2%	70 mV	62.6 mV	10.6%

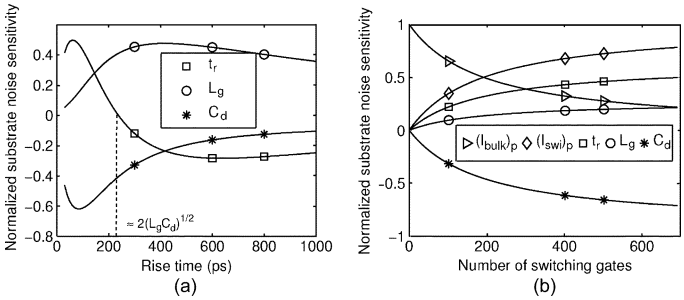

Fig. 6. Substrate noise sensitivity when $L_g = 1$ nH, $C_d = 10$ pF, $R_g = 2.2\,\Omega$, $R_d = 0.1\,\Omega$, $R_{\rm cb} = 10.7$ kΩ, $R_{\rm dist} = 40$ kΩ, $R_{\rm vc} = 660\,\Omega$, $R_{\rm ang} = 2.2\,\Omega$, and $L_{\rm ang} = 1$ nH. (a) As a function of rise time when $n = 400$. (b) As a function of the number of switching gates when $t_r = 100$ ps.

where $V_{\rm s-total}$ (the total substrate noise at the victim node) is given by (11). For multiple switching gates, the resistance $R_{\rm cb}$ is scaled by n where n is the number of switching gates tied to a substrate contact. Alternatively, $R_{\rm dist}$ remains the same, assuming that the analog circuit is sufficiently far from all of the switching gates.

The normalized sensitivity of the substrate noise, as determined by (13), is shown, respectively, in Fig. 6(a) and (b). The sensitivity of the noise to the decoupling capacitance is high at small rise times and decreases with increasing rise time. Alternatively, the sensitivity to the parasitic inductance is low at small rise times and increases with longer rise times. This behavior is due to the rise-time-dependent ratio of the switching current sourced by the decoupling capacitance and the power supply through the parasitic inductance. Note that the sensitivity to the rise time crosses over at zero when $t_r \approx 2\sqrt{(L_g C_d)}$, demonstrating the nonmonotonic dependence of noise on the rise time, as shown in Fig. 3.

The sensitivity to the switching current, parasitic inductance, decoupling capacitance, and rise time increases with a larger number of switching gates, as shown in Fig. 6(b), since the ground coupling starts to dominate for large-scale circuits. For a small number of switching gates, the sensitivity to the total bulk current is sufficiently high, increasing the significance of the substrate contacts to reduce noise in small-scale circuits, as described in the following section.

V. DESIGN IMPLICATIONS

The design implications of the proposed macrolevel model are discussed in this section. Specifically, the efficiency of increasing the substrate contact density, reducing the package and on-chip parasitic inductance, and placing additional on-chip decoupling capacitance are compared as a function of the rise time and number of switching gates. The noise reduction achieved by these techniques is listed in Table II. This comparison can be used to determine the preferable noise reduction technique at early stages of the design process, as further described in the following sections.

A. Increasing Substrate Contact Density

For those cases where source/drain coupling dominates, increasing the number of substrate contacts or placing a p+ guard ring around the aggressor circuit achieves enhanced noise reduction as compared to reducing the parasitic inductance or increasing the decoupling capacitance. Alternatively, if ground coupling is the dominant coupling mechanism, placing additional decoupling capacitance and reducing the parasitic inductance are more efficient techniques. This comparison is illustrated by points 1 and 2 in Fig 5(a), which represent, respectively, the dominance of ground coupling and source/drain coupling. For point 2, the peak-to-peak substrate noise is reduced by 31% by doubling the substrate contacts. Lowering the parasitic inductance by a factor of four reduces the noise by only 3.5%. Similarly, increasing the decoupling capacitance by a factor of four reduces the noise by 10.5%. Alternatively, for point 1, where ground coupling is dominant, doubling the number of substrate contacts achieves a 12.1% reduction in noise while reducing the parasitic inductance and increasing the decoupling capacitance, each by a factor of four, reduces the noise by, respectively, 34.1% and 42.8%. The efficiency of increasing the substrate contact density is compared with reducing the parasitic inductance and increasing the decoupling capacitance in Fig. 7(a), demonstrating the significance of the number of contacts on small-scale circuits where source/drain coupling is dominant.

B. Increasing Decoupling Capacitance Versus Reducing Parasitic Inductance

The efficiency of placing additional decoupling capacitance and reducing the parasitic inductance is a strong function of rise time, as illustrated by the sensitivities shown in Fig. 6(a). The efficiency of these two techniques is compared in Fig. 7(b). At $t_r = 70$ ps, doubling the decoupling capacitance achieves a 39% reduction in the peak-to-peak substrate noise where $2\sqrt{L_g C_d} = 200$ ps. Halving the parasitic inductance, however, achieves a reduction of only 11%. Alternatively, at $t_r = 800$ ps, halving the parasitic inductance achieves enhanced noise reduction of 23%, while doubling the decoupling capacitance reduces the noise by 12%. Specifically, increasing the decoupling capacitance is effective for $t_r \ll 2\sqrt{L_g C_d}$, while reducing the parasitic inductance is effective for $t_r \gg 2\sqrt{L_g C_d}$. This behavior is due to the changing

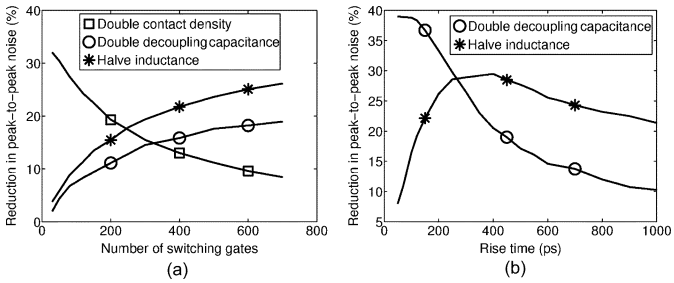

Fig. 7. Comparison of noise reduction techniques when $L_g = 1$ nH, $C_d = 10$ pF, $R_g = 2.2\ \Omega$, $R_d = 0.1\ \Omega$, $R_{\rm ang} = 2.2\ \Omega$, and $L_{\rm ang} = 1$ nH: (a) as a function of the number of switching gates at $t_r = 400$ ps; (b) as a function of the rise time when $n = 700$.

ratio of the switching current provided by the decoupling capacitance and the power supply with respect to the rise time.

VI. Conclusion

A substrate coupling model for multiple switching gates is presented for macrolevel analysis of the various substrate noise coupling mechanisms. The proposed model identifies the dominant noise source at the early stages of the design process as a function of multiple parameters. Identification of the dominant noise source and parameter sensitivity is used to determine the most efficient noise reduction technique.

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