Quasi-Resonant Interconnects: A Low Power, Low Latency Design Methodology

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***Abstract*—Design and analysis guidelines for quasi-resonant interconnect networks (QRN) are presented in this paper. The methodology focuses on developing an accurate analytic distributed model of the on-chip interconnect and inductor to obtain both low power and low latency. Excellent agreement is shown between the proposed model and SpectraS simulations. The analysis and design of the inductor, insertion point, and driver resistance for minimum power-delay product is described. A case study demonstrates the design of a quasi-resonant interconnect, transmitting a 5 Gb/s data signal along a 5 mm line in a TSMC 0.18-μm CMOS technology. As compared to classical repeater insertion, an average reduction of 91.1% and 37.8% is obtained in power consumption and delay, respectively. As compared to optical links, a reduction of 97.1% and 35.6% is observed in power consumption and delay, respectively.**

***Index Terms*—Latency, on-chip inductors, on-chip interconnects, power dissipation, resonance.**

I. Introduction

A PRIMARY challenge in high performance, high complexity integrated circuits (ICs) is the on-chip interconnect [1]. Transmitting clock, data, and communications signals over large die areas requires long interconnections among the various circuit modules. Consequently, as technology scales, the interconnect cross section decreases while operating frequencies increase. The impact of these trends on high performance systems is significant. Long interconnects with smaller cross sections exhibit increased capacitance and resistance, resulting in greater power consumption, latency, and signal attenuation. Furthermore, wire inductance can no longer be ignored due to high signal frequencies and long wire lengths. Two figures of merit that determine the length of interconnect in which inductance effects are significant have been described in [2].

Some of these challenges are evident in the international technology roadmap for semiconductors (ITRS) [1], as shown in Fig. 1. According to ITRS predictions, the total on-chip wire length will increase linearly with technology, reaching above 2000 m/cm^2 by the end of this decade [see Fig. 1(a)]. This trend supports the assumption that long interconnects will be significant in future technologies. A prediction for resistance–capacitance (*RC*) interconnect delay is depicted in Fig. 1(b). The *RC* delay increases quadratically with technology, reaching above 500 ps (for a 1 mm Cu global wire) by 2010. This trend supports the assumption that long interconnects with small cross sections exhibit increasing latency and delay uncertainty.

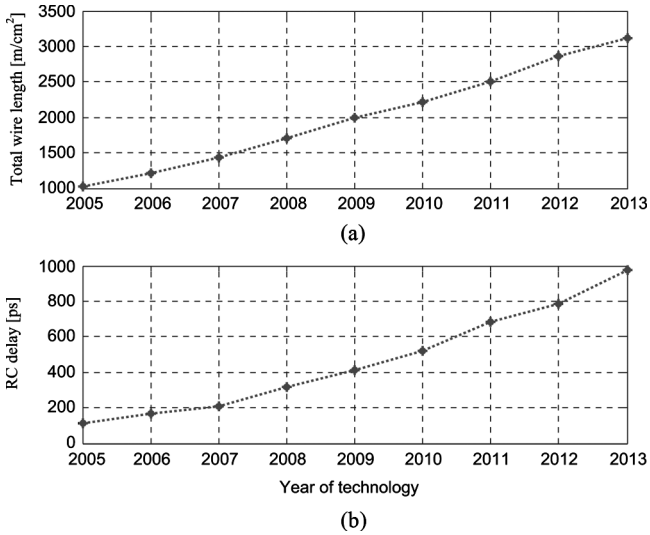

Fig. 1. 2005 ITRS predictions: (a) total interconnect length of metal 1 and 5 intermediate levels; (b) *RC* interconnect delay for a 1 mm Cu global wire.

To combat these phenomena, traditional repeater insertion methods have been widely developed [3]. Unfortunately, as interconnect lengths increase, a larger number of repeaters is required. This results in significant power dissipation, increased delay, and larger area. Low power techniques, therefore, in the form of low swing signaling, have been developed. In [4], current mode signaling in an ultra-low voltage environment is used to transmit high data rate signals. In this approach, a current sense amplifier at the far end of the line detects a current difference and converts it into a voltage difference. To improve both delay and energy dissipation, a transmitter generating a differential current detected by a current mode sense amplifier at the receiving end has been proposed in [5]. To accommodate differential operation, redundant circuitry is used.

To minimize static power dissipation associated with current mode signaling, an adaptive bandwidth bus architecture based on hybrid current voltage mode repeaters for long *RC* interconnect has been proposed in [6]. In this approach, the interconnect is divided into smaller segments. Appropriately spaced repeaters amplify the signal and drive the subsequent interconnect segment. An adaptive control unit is placed at the input

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of the line and connected to a control line, which is common to all of the repeater stages. Contrary to the current mode signaling approach, the authors of [7] and [8] suggest the use of low voltage signaling over long on-chip interconnects. In [7], a heuristic algorithm for buffer insertion that considers noise, delay, and power is proposed. The method proposed in [8] is based on the so-called swing limited interconnect accelerator. This circuit has a three stage cascade inverter configuration with keepers. The keepers limit the voltage on the interconnect to permit low swing operation. Additional inverters are placed at the output to restore the signal level to full swing.

A different approach exploiting wire inductance at high frequencies is introduced in [9]. Chang *et al.* [9] suggest that at lower frequencies the resistive part of the interconnect is dominant, behaving as a distributed *RC* network. At higher frequencies, the inductive component of the transmission line dominates, behaving as a distributed inductance–capacitance (*LC*) network. In this scheme, a 1-GHz link operating with phase shift keying modulation on a 7.5-GHz sinusoidal carrier is presented. This type of modulation, however, results in relatively large power dissipation and poor spectral efficiency. Alternatively, the authors of [10] propose mitigating the dispersion due to high frequencies by utilizing a return to zero (RZ) signaling scheme in which sharp current pulses transmit data. The transmitted data is modulated to higher frequencies, maximizing the effect of the wire inductance. This approach allows the interconnects to behave in a relatively dispersionless fashion.

As an alternative to electrical interconnects and related electrical limitations, optoelectronic links [11] have been considered. Optical interconnections promise to achieve high bandwidth by providing high density parallel communication channels. The interface between the electrical and optical signals however is a major issue in optoelectronic applications.

In this paper, a low power, low latency on-chip interconnect design methodology is proposed. The methodology is based on inserting an on-chip spiral inductor to resonate the interconnect around the fundamental harmonic of the transmitted signal. In this way, the interconnect capacitance resonates with the inserted on-chip inductance. The fundamental harmonic of the input signal is amplified and transmitted to the output. This approach lowers power consumption, since the energy resonates between the electric and magnetic fields rather than dissipates as heat. Consequently, buffers are eliminated, significantly reducing power consumption and signal latency.

This paper is organized into six sections. The use of on-chip resonance in integrated circuits as well as the principle of resonance for data transmission are presented in Section II. The interconnect and spiral inductor models are described in Section III. In Section IV, a quasi-resonant interconnect design methodology is described, followed by a case study demonstrating 5 Gbps data signal distribution along a 5-mm interconnect in Section V. Simulation results and a comparison to other schemes are presented in Section VI. Finally, some conclusions are offered in Section VII. In Appendix A, a receiver circuit is described. The *ABCD* matrices are reviewed in Appendix B and a derivation of the 50% delay is provided in Appendix C.

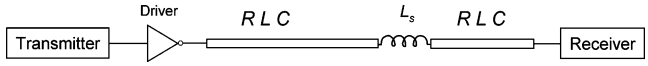

Fig. 2. Quasi-resonant network.

II. Principle of Quasi-Resonant Interconnects

Following the invention of the telegraph and the telephone, transmission techniques were developed to accommodate the increasing distance between the transmitter and receiver while supporting a higher transmission rate. Pupin introduced the concept of inserting reactance sources in series with long telegraphic lines in 1899 [12], [13]. Pupin suggested inserting inductance coils in a network composed of a uniform conductor with a telephonic transmitter and receiver. The inductance coils are inserted in series at periodically recurring locations. The electrical line parameters and the distance between the coils are adjusted to reduce signal attenuation, enabling transmission of speech waves over very long distances. The application of transmission lines with periodic inductors to microwave applications is described in [14], and is based on Pupin's invention.

The concept of exploiting standing waves in transmission lines was first introduced by Chi in 1994 [15]. A global resonant clock distribution network was later introduced in 2003 by Chan *et al.* [16]. In this circuit, a set of discrete on-chip spiral inductors and capacitors is attached to a traditional H-tree structure. The capacitance of the clock distribution network resonates with the inductance, while the on-chip capacitors establish a mid-rail dc voltage around which the grid oscillates. This approach lowers the power consumption, skew, and jitter.

Chueh *et al.* [17] designed and evaluated a two-phase resonant clock generation and distribution system with layout extracted inductor parameters in a 0.13-μm CMOS process. The circuit includes a programmable replenishing clock generator and tunable capacitors. Both skew and jitter are reduced with this approach.

A design methodology for resonant clock distribution networks is presented in [18]. Design guidelines based on an accurate distributed transmission model are proposed, supporting low power H-tree clock distribution networks. The design methodology provides tradeoffs among the operating frequency, the size of the on-chip inductors and capacitors, and the output resistance of the driving buffer. A sensitivity analysis of resonant H-tree clock distribution networks is also provided.

The proposed quasi-resonant interconnect network architecture is illustrated in Fig. 2. The transmitter at the near end of the interconnect modulates the input data signal. The signal modulation supports a quasi-periodic signal with a single resonant frequency. The transmitter is followed by an inverter driving the interconnect. The *RLC* distributed transmission line is separated by an on-chip spiral inductor L_s inserted at a specific point to resonate the network at a desired frequency for minimum power consumption and delay. The receiver at the far end of the interconnect demodulates the transmitted signal back into the original input bit stream.

Since the fundamental harmonic of the input signal is amplified by the magnitude of the transfer function, the network

resonates at a specific target frequency and magnitude. This behavior is required to transfer a full swing sinusoidal signal at the resonance frequency to the far end of the interconnect. To satisfy this objective, consider the output signal in the frequency domain

$$V_{\text{out}}(s) = H'(s) \cdot V_{\text{in}}(s) \tag{1}$$

where $H'(s)$ is the transfer function of the network between the transmitter and the receiver (including the driver), and $V_{\text{in}}(s)$ is the input data bit. The input data signal in the time domain can be represented by a Fourier series, assuming $V_{\text{in}}(s)$ is a periodic signal

$$v_{\text{in}}(t) = \sum_{k=-\infty}^{\infty} a_k e^{jk\omega_p t} \tag{2}$$

where a_k is the k^{th} harmonic of the signal and ω_p is the resonant radian frequency. In the case of a periodic square waveform with period time t_p, transition time t_t, and amplitude V_{dd}, the fundamental harmonic (positive and negative) is

$$a_{\pm 1} = \pm \frac{V_{\text{dd}} t_p}{2 t_t \pi^2} \left(e^{-j\omega_p t_t} - 1 \right). \tag{3}$$

Equation (1) implies that the required magnitude of the transfer function is

$$\left| H'(j\omega_p) \right| = \frac{\left(\frac{V_{\text{dd}}}{2} \right)}{\left(2 \left| a_1 \right| \right)} = \frac{V_{\text{dd}}}{4 \left| a_1 \right|}. \tag{4}$$

Substituting (3) into (4) results in

$$\left| H'(j\omega_p) \right| = \frac{t_t \pi^2}{t_p \sqrt{8 \left(1 - \cos\left(\omega_p t_t \right) \right)}}. \tag{5}$$

Equation (5) describes the magnitude of the transfer function at ω_p to transfer a full swing waveform. For example, at a 5-GHz operating frequency ($t_p = 200$ ps) and $t_t = 20$ ps, the magnitude of the transfer function is 0.8.

III. Interconnect and Spiral Inductor Models

Accurate models of the quasi-resonant network are presented in this section. Transmission line and on-chip spiral inductor models are described in Section III-A and III-B, respectively.

A. Interconnect Model

As data signal frequencies exceed the multigigahertz regime, distributed models of interconnects are required to accurately incorporate high frequency effects into the system behavior. The wire inductance can no longer be excluded from the model and traveling wave reflections should be characterized by a distributed structure. Using a classical distributed model, an incremental section of line length Δz is modeled as a lumped element circuit. In this representation, R, L, and C are the resistance, inductance, and capacitance per unit length, respectively. The lumped resistance represents the lossy component of the transmission line.

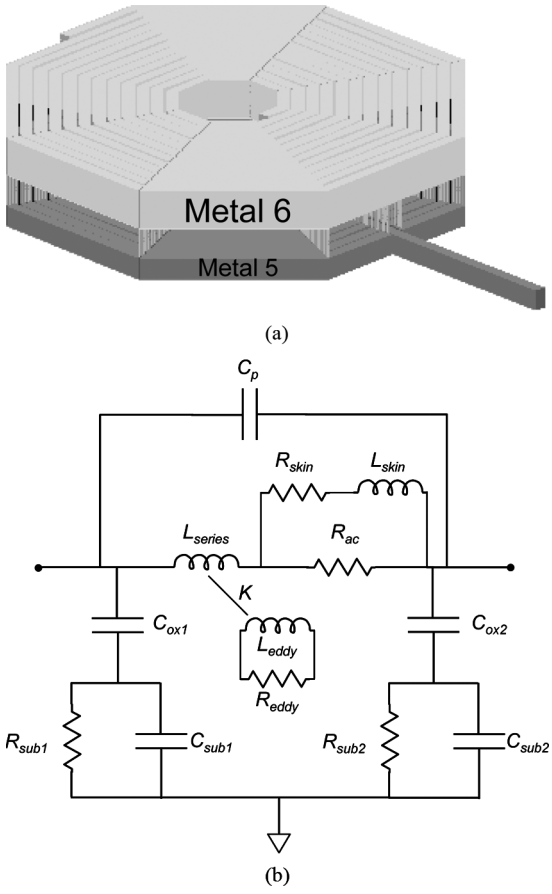

Fig. 3. Model of an on-chip spiral inductor: (a) structure of an octagonal on-chip spiral inductor; (b) lumped model of a spiral inductor.

B. On-Chip Spiral Inductor Model

To accurately account for the parasitic effects of the on-chip spiral inductor, a thirteen lumped element model is used. The physical structure and a lumped model of the on-chip inductor are illustrated in Fig. 3(a) and (b), respectively. Note that the octagonal on-chip spiral inductor shown in Fig. 3(a) utilizes Metal 5 and Metal 6 where the two layers are connected by vias. In this manner, the inductor can achieve a higher Q, as analyzed by SPIRAL, a 3-D spiral inductor design and synthesis tool.[1]

The capacitance C_p represents the capacitive coupling between the windings of the spiral inductor. The elements L_{series} and R_{ac} represent the inductance and parasitic resistance, respectively, while R_{skin} and L_{skin} model the skin effect. Also note that L_{series} incorporates the eddy current effect coupled to the inductor by the coefficient K. The parasitic capacitance between the lines and the substrate is modeled by C_{ox}. The parallel C_{sub} and R_{sub} combination models the parasitic resistance and capacitance to the substrate.

IV. Design Methodology

In this section, the quasi-resonant interconnect design methodology is described. The design of the transmitter and

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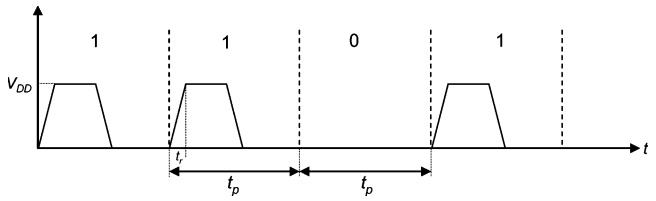

Fig. 4. Example of transmitting a "1011" bit stream.

receiver is presented in Section IV-A and IV-B, respectively. The input impedance and transfer function of the quasi-resonant network are analytically characterized in Section IV-C. Based on these expressions, a power consumption model followed by a closed-form analytic expression are developed in Section IV-D. In Section IV-E, closed-form analytic expressions for the signal delay are described. Finally, design guidelines for the quasi-resonant interconnect that minimizes the power-delay product is described in Section IV-F.

A. Transmitter Design

Proper operation of the network requires resonance at a single target frequency. As illustrated in Fig. 4, the return to zero (RZ) amplitude shift keying modulation scheme is chosen to support the single transmission frequency of the input data. In this scheme, the data is transferred at $1/t_p$ bits/s.

This scheme has three advantages when applied to the proposed quasi-resonant interconnect methodology. The transmitted signal has a single frequency (with amplitude variation, i.e., $V_{\rm dd}$ and 0 V to distinguish between logic one and zero, respectively) designed to match the resonance frequency of the network. Power is dissipated only during transmission of logic one, and only during half of the time period. Finally, no complex circuitry is required to produce this modulation scheme.

The transmitter generates the required modulated signal which is amplified by the buffer chain at the input of the driver (see Fig. 2). The proposed modulation scheme, transmitter circuit, transistor level circuit, and simulated signal waveforms are illustrated in Fig. 5.

To realize the modulation scheme shown in Fig. 5(a), an AND operation is performed between the clock and the input data followed by a buffer chain, as shown in Fig. 5(b). The high frequency data rate supported by the quasi-resonant interconnects requires a high speed transmitter and receiver. To maintain high speed operation, a transmission gate-based circuit (consisting of transistors $\rm M_{t1}$, $\rm M_{t2}$, $\rm M_{t3}$, and $\rm M_{t4}$) is used for the logic, as shown in Fig. 5(c). In the case where both the clock and data are at logic one, the transmission gate $\rm M_{t1}$ passes the logic one state to the input of the buffer chain, while the inverter (consisting of transistors $\rm M_{t3}$ and $\rm M_{t4}$) turns off transmission gate $\rm M_{t2}$. In all of the other cases, the logic zero state is passed to the input of the buffer chain.

Transistor $\rm M_{t5}$ restores the voltage (equal to $V_{\rm th}$) associated with the operation of transmission gates $\rm M_{t1}$ and $\rm M_{t2}$. The input data as well as the modulated signal are shown in Fig. 5(d). In this example, a "100100111" bit stream is modulated at a 5-GHz operating frequency. Note that the modulated signal follows the

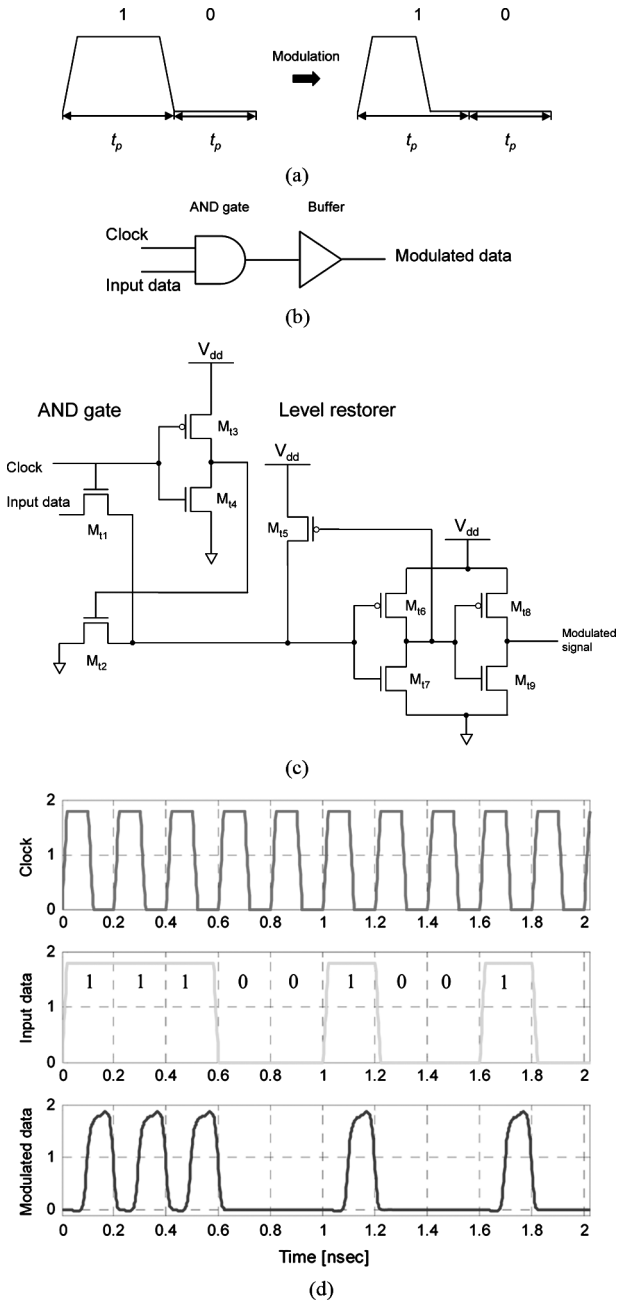

Fig. 5. Transmitter circuit: (a) modulation scheme; (b) gate level circuit; (c) transistor level circuit; (d) signal waveforms.

return to zero amplitude shift keying scheme, essential for quasi-resonant operation.

B. Receiver Design

The receiver located at the far end of the interconnect (see Fig. 2) demodulates the transmitted data into the original signal. A logic level description of the proposed receiver circuit, a transistor level circuit, and simulated signal waveforms are depicted in Fig. 6. The principle of the demodulation scheme is based on a sample and hold (S/H) operation, as shown in Fig. 6(a). When the clock is high, the switch closes and the data is sampled and transferred. The sampled signal charges (and discharges) the parasitic capacitance C_p. When the clock is low, the switch

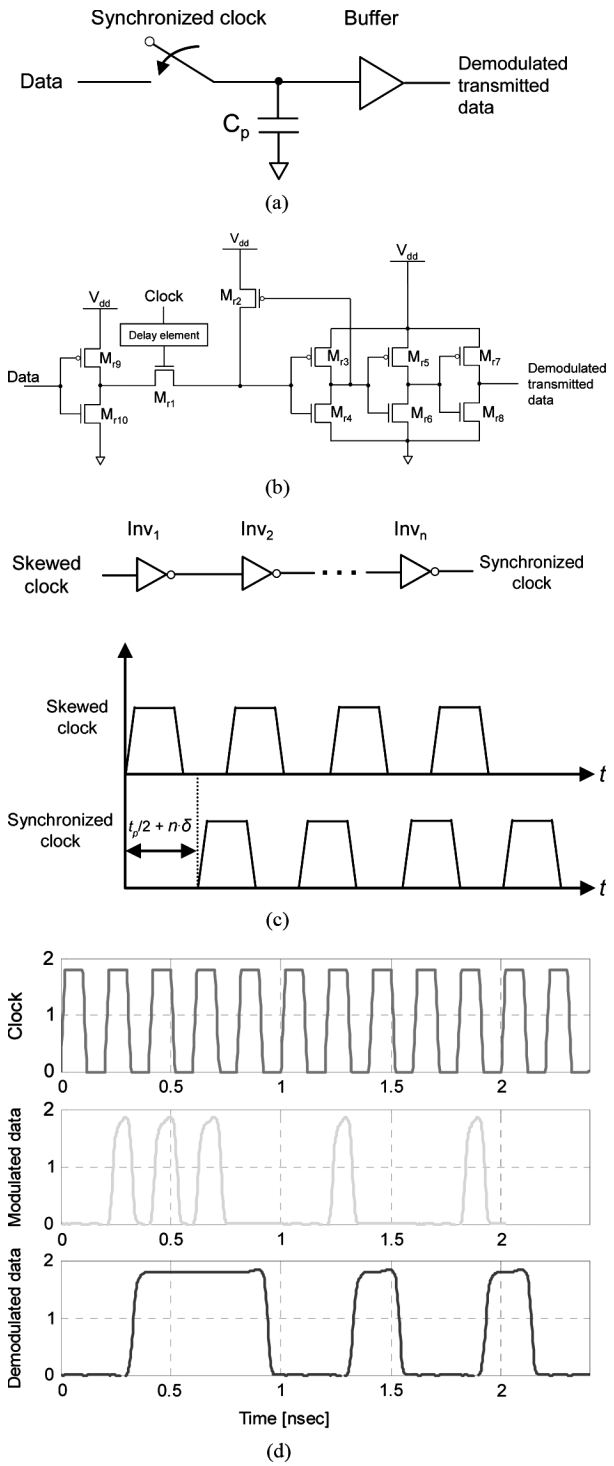

Fig. 6. Receiver circuit: (a) sample and hold circuit; (b) transistor level circuit; (c) delay element circuit and timing diagram; (d) signal waveforms.

is open and the logic state is stored (or held) until the following clock cycle. In this manner, the S/H circuit prolongs the duration of the high state signals over the entire clock cycle t_p without altering the duration of the low state signals.

The receiver circuit at the transistor level is shown in Fig. 6(b). In this circuit, when the clock state is high, transistor $\mathrm{M_{r1}}$ turns on and the data is sampled and transferred. When the data state is low, the restorer transistor $\mathrm{M_{r2}}$ turns on, maintaining the high state signal at the input of the second inverter (consisting of transistors $\mathrm{M_{r3}}$ and $\mathrm{M_{r4}}$). This mechanism serves a dual purpose. It restores the voltage associated with the transmission gate $\mathrm{M_{r1}}$, and prevents charge leakage by replenishing the charge on the parasitic capacitance of transistors $\mathrm{M_{r3}}$ and $\mathrm{M_{r4}}$ (through the feedback connection). When the clock logic is low, $\mathrm{M_{r2}}$ prevents the charge from leaking. When the data logic is high, transistor $\mathrm{M_{r2}}$ turns off and the logic low state is transferred to the output. Finally, when the clock state is low, the previous logic state is preserved until the following clock cycle.

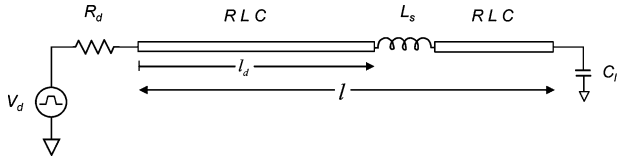

Fig. 7. Quasi-resonant network.

Note that for the receiver to operate properly, the allowed skew between the clock and the incoming modulated data should be less then one quarter of the clock cycle. This constraint is required since the demodulation circuit is level sensitive. To synchronize the clock with the data, a delay element is used, as depicted in Fig. 6(b). The delay of the arriving modulated data is determined from simulations or the analytic delay expressions presented in Section IV-E. A delay element based on inverters is used as shown in Fig. 6(c). The delay element provides a course and a fine delay. If course tuning is required (i.e., the delay of a half clock cycle, $t_p/2$), an odd number of inverters is used. If fine tuning is required (i.e., the intrinsic delay of the inverters), an even number of inverters is required. In this manner, for an odd number of inverters, a total delay of $t_p/2+n\delta$ is achieved. For an even number of inverters, a total delay of $n\delta$ is achieved. δ and n are the intrinsic delay of a single inverter and number of inverters, respectively.

Simulation results of this circuit are presented in Fig. 6(d). In this example, the output of the modulation circuit shown in Fig. 5(c) drives the demodulation circuit shown in Fig. 6(b). As depicted in Fig. 6(d), the output waveform is identical to the input data waveforms illustrated in Fig. 5(d). An alternative receiver circuit that does not require the interconnect and inverter delay element is presented in Appendix A.

C. Network Input Impedance and Transfer Function

To obtain analytic closed-form expressions of the power consumption and delay of the quasi-resonant interconnect, the input impedance and the transfer function of the network are determined in this subsection. The quasi-resonant network (QRN) (between the transmitter and receiver) including the driver is shown in Fig. 7. Note that the driver is modeled as a linearized voltage source V_d serially connected with a driver resistance R_d. The load of the interconnect is modeled as a capacitor C_l.

To analyze this type of structure, an accurate analytic model is developed based on *ABCD* parameters. From transmission line

theory, the *ABCD* matrix for the entire structure is a product of the individual matrices

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = M_{\text{int1}} \cdot M_s \cdot M_{\text{int2}} \cdot M_l \tag{6}$$

where M_{int1}, M_s, M_{int2}, and M_l are the *ABCD* matrix of the first interconnect section, the on-chip inductor [based on the model of Fig. 3(b)], the second interconnect section, and the load capacitance, respectively. These matrices are described in Appendix B. Matrices M_{int1} and M_{int2} are based on the distributed transmission line model presented in Section III-A. From the overall *ABCD* parameters, the transfer function $H(j\omega)$ (excluding the driver resistance) and the input impedance $Z_{\text{in}}(j\omega)$ of the system are, respectively

$$H(j\omega) = \frac{1}{A} \tag{7}$$

$$Z_{\text{in}}(j\omega) = R_{\text{in}} + jX_{\text{in}} = \frac{A}{C}. \tag{8}$$

The transfer function of the overall network shown in Fig. 7 (including the driver resistance) is given by (9), where R_d and R_{in} are the driver and input resistance, respectively, and X_{in} is the input reactance

$$\begin{aligned} |H'(j\omega)| &= \left| \frac{Z_{\text{in}}}{Z_{\text{in}} + R_d} \right| \cdot |H(j\omega)| \\ &= \left| \frac{R_{\text{in}} + jX_{\text{in}}}{(R_{\text{in}} + R_d) + jX_{\text{in}}} \right| \cdot |H(j\omega)| \\ &= \sqrt{\frac{R_{\text{in}}^2 + X_{\text{in}}^2}{(R_d + R_{\text{in}})^2 + X_{\text{in}}^2}} \cdot |H(j\omega)|. \end{aligned} \tag{9}$$

The driver resistance is extracted from (9). Equating $|H'(j\omega)|$ to the value obtained from (5) at a specific frequency ω_p and solving for R_d results in

$$R_d = \left(\sqrt{\frac{|H(j\omega_p)|^2}{|H'(j\omega_p)|^2} \cdot (R_{\text{in}}^2 + X_{\text{in}}^2) - X_{\text{in}}^2} \right) - R_{\text{in}} \tag{10}$$

where $H'(j\omega_p)$ and $H(j\omega_p)$ are given by (5) and (7), respectively.

D. Power Consumption Model

The average power consumed by the network shown in Fig. 1 is

$$P_{\text{total,avg}} = P_{\text{trx,avg}} + P_{\text{qrn,avg}} + P_{\text{rec,avg}} \tag{11}$$

where $P_{\text{trx,avg}}$ and $P_{\text{rec,avg}}$ are the average power consumption of the transmitter and receiver, respectively, and $P_{\text{qrn,avg}}$ is the average power consumption of the quasi-resonant network (including the driver).

The resonant interconnect network is a passive linear network. A one-port network, as depicted in Fig. 8, can therefore be used to determine $P_{\text{qrn,avg}}$. The output impedance of the driver R_d and the input impedance of the network Z_{in} determine the power consumption of the network.

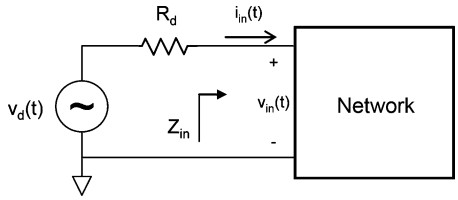

Fig. 8. One-port network driven by a voltage source.

Power, defined as the rate at which energy is absorbed [20], is

$$P_{\text{qrn,avg}} = \frac{1}{2} V_{\text{in,rms}}^2 \cdot \Re \left\{ \frac{1}{Z_{\text{in}}} \right\} \tag{12}$$

where $V_{\text{in,rms}}$ is the effective or root-mean square value of any periodic voltage and is

$$V_{\text{in,rms}} = \left(\frac{1}{T} \int_{t_0}^{t_0+T} |v_{\text{in}}(t)|^2 \, dt \right)^{1/2} \tag{13}$$

where T is the time period of the periodic function $v_{\text{in}}(t)$. The input voltage $v_{\text{in}}(t)$ (see Fig. 8) can be expressed in terms of the voltage source function $v_d(t)$, and is

$$v_{\text{in}}(t) = v_d(t) \cdot \frac{Z_{\text{in}}}{Z_{\text{in}} + R_d}. \tag{14}$$

Substituting (13) and (14) into (12) results in

$$\begin{aligned} P_{\text{qrn,avg}} &= \frac{1}{2} V_{\text{rms},d}^2 \cdot \left| \frac{Z_{\text{in}}}{Z_{\text{in}} + R_d} \right|^2 \cdot \Re \left\{ \frac{1}{Z_{\text{in}}} \right\} \\ &= \frac{1}{2} V_{\text{rms},d}^2 \cdot \frac{R_{\text{in}}}{(R_{\text{in}} + R_d)^2 + X_{\text{in}}^2}. \end{aligned} \tag{15}$$

Substituting (10) into (15) yields a simplified expression, depending solely on the input impedance of the network Z_{in}

$$P_{\text{qrn,avg}} = \frac{1}{2} V_{\text{rms},d}^2 \cdot \left| \frac{H'(j\omega_p)}{H(j\omega_p)} \right|^2 \cdot \frac{R_{\text{in}}}{(R_{\text{in}}^2 + X_{\text{in}}^2)}. \tag{16}$$

E. Signal Delay Model

The total signal delay of the network shown in Fig. 2 is

$$t_{d,\text{tot}} = t_{d,\text{trx}} + t_{d,\text{qrn}} + t_{d,\text{rec}} \tag{17}$$

where $t_{d,\text{trx}}$ and $t_{d,\text{rec}}$ are the transmitter and receiver signal delay, respectively, and $t_{d,\text{qrn}}$ is the signal delay of the quasi-resonant network (including the driver).

A derivation of a closed-form expression for $t_{d,\text{qrn}}$ is based on the work of Chen and Friedman [21]. Chen and Friedman [21] based their analysis on a Fourier series, where a time-domain waveform as well as the 50% delay is approximated by the summation of several sinusoids. Although this method is designed for interconnects driven by a periodic signal, it can also be applied to a quasi-resonant network. As shown in Fig. 4, the QRN is driven by a modulated signal periodic in time with two different symbols for logic one and zero. It can therefore be assumed that a quasi-resonant network is driven by a quasi-periodic signal.

The 50% delay can be expressed as

$$t_{d,\mathrm{qrn}} = \frac{\arctan x_0}{\omega_p} - \frac{t_r}{2} \tag{18}$$

where x_0 is a single real root of a third-order polynomial, as described in Appendix C. Note that the value of $\arctan x_0$ is in the range of $[0, \pi]$; otherwise, π should be added or subtracted from x_0. In the case of three real roots, the output waveform is not shaped like a square wave and can no longer represent a logic state. Note that the derivation of (18) assumes that the 50% delay is less than $t_p/2 - t_r/2$.

F. Design Guideline

The QRN design process is summarized as a flow diagram in Fig. 9. The interconnect geometries, i.e., length, width, and thickness, are designed according to technological constraints and requirements. Once the geometry and transmission frequency are specified, the next step is to determine the line resistance, inductance, and capacitance per unit length. A lookup table for different on-chip inductor magnitudes and the corresponding equivalent lump model parameters (such as depicted in Fig. 3) can be extracted from experimental measurements or an electromagnetic field solver.[1]

Expressions (16) and (18), developed in Section IV-C to IV-E, are used to optimize the QRN to minimize the power-delay product. Simultaneously solving (16) and (18) for different on-chip inductances and insertion points along the interconnect results in a power-delay product which can be described graphically. The equivalent driver resistance is determined from (10). The required magnitude of the on-chip inductor, insertion point, and driver resistance to enable optimum power-delay operation are inferred from these graphs.

If the on-chip inductance, insertion point, and driver resistance are not physically realizable, the design cycle is repeated with a different technology, transmission frequency, or interconnect geometry. Once the parameters are determined, the driver is designed based on the specified output resistance. Finally, the transmitter is designed based on the operating frequency and driver input capacitance.

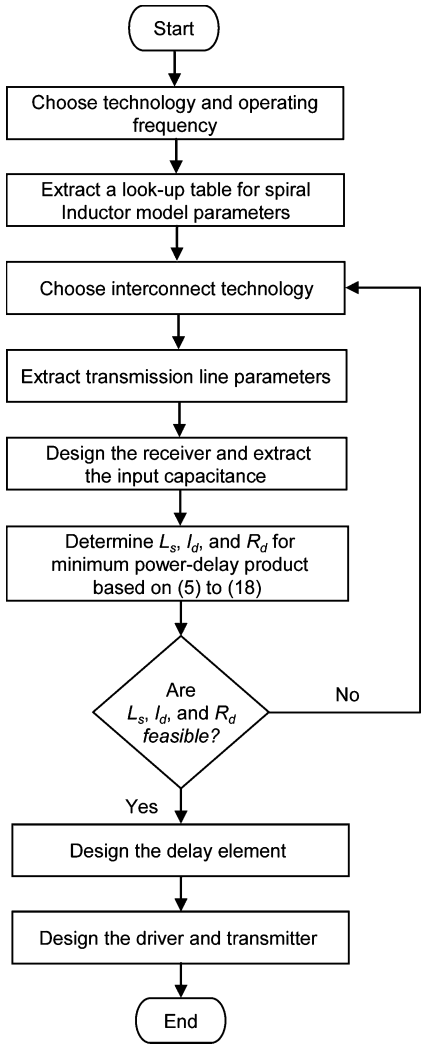

Fig. 9. Flow diagram of QRN design process.

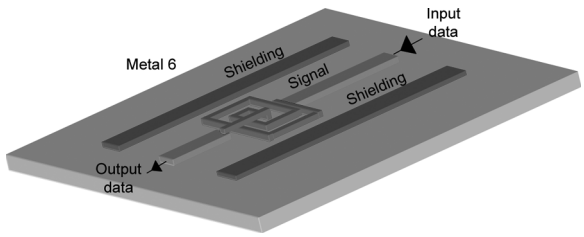

Fig. 10. Layout of a resonant transmission line network.

V. Case Study

The design guidelines and principles presented in Section IV and illustrated in Fig. 9 are demonstrated in a case study. This example is based on a TSMC 0.18-μm CMOS technology, transmitting data at a 5 Gb/s frequency. The target time period is $t_p = 200$ ps and the rise (fall) time is $t_r = 20$ ps with a supply voltage $V_{\mathrm{dd}} = 1.8$ V.

The on-chip octagonal inductor model parameters are extracted from SPIRAL.[1] The spiral inductors (varying between 1 to 10 nH) have been designed and optimized to achieve a maximum Q at 5 GHz.

The layout geometry and configuration of the quasi-resonant network are schematically illustrated in Fig. 10. To reduce crosstalk and coupling noise from neighboring interconnects, the quasi-resonant interconnect is shielded by two parallel ground lines. The shield lines reduce the parasitic coupling capacitance between the two signal lines. Another strategy to mitigate inductive crosstalk is to utilize perpendicular lines on different metal layers.

The separation between the signal and ground lines is 2 μm. The width of the signal and ground lines is 2 and 4 μm, respectively, while the thickness of each of the lines is 1 μm. In this example, the interconnect parameters (including the shield lines) are $l = 5$ mm, $R = 17$ mΩ/μm, $L = 1.66$ pH/μm, and $C = 0.072$ fF/μm.

TABLE I
TRANSISTOR WIDTH OF THE RECEIVER AND TRANSMITTER CIRCUITS, $L = 0.18\ \mu$m

Width [μm]			
Receiver		Transmitter	
M_{r1}	2.0	M_{t1}	1.0
M_{r2}	1.0	M_{t2}	1.0
M_{r3}	1.5	M_{t3}	2.5
M_{r4}	2.0	M_{t4}	1.0
M_{r5}	2.5	M_{t5}	0.5
M_{r6}	1.0	M_{t6}	2.5
M_{r7}	2.5	M_{t7}	1.0
M_{r8}	1.0	M_{t8}	0.3
M_{r9}	7.5	M_{t9}	0.2
M_{r10}	3.0		

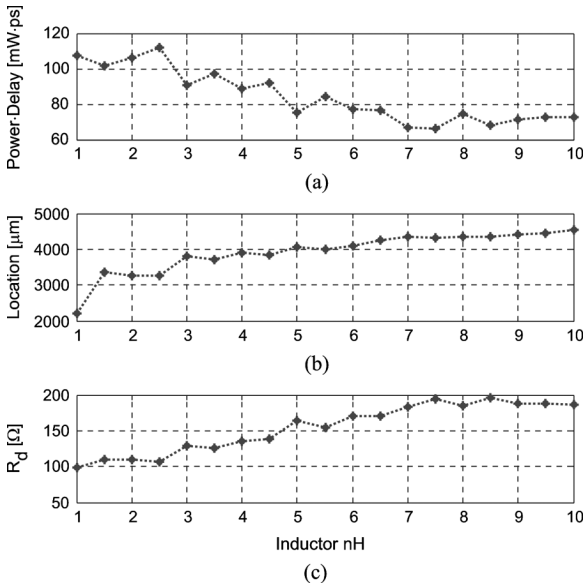

Fig. 11. Design example of a 5-mm-long interconnect operating at a 5-Gb/s transmission frequency: (a) minimum power-delay product as a function of inductance; (b) insertion location as a function of inductance; and (c) driver resistance as a function of inductance.

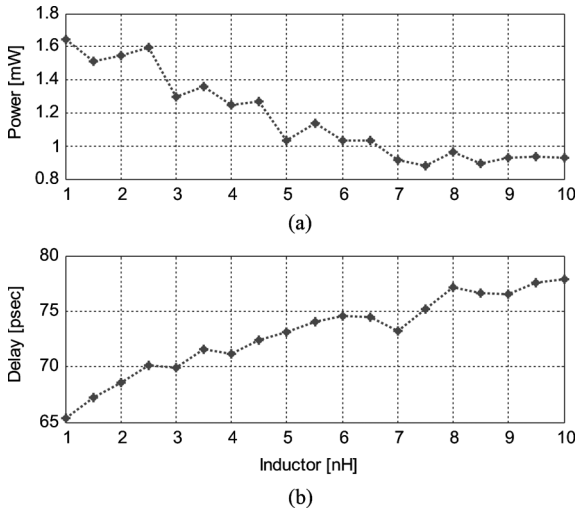

Fig. 12. Power and delay: (a) power consumption; (b) signal delay.

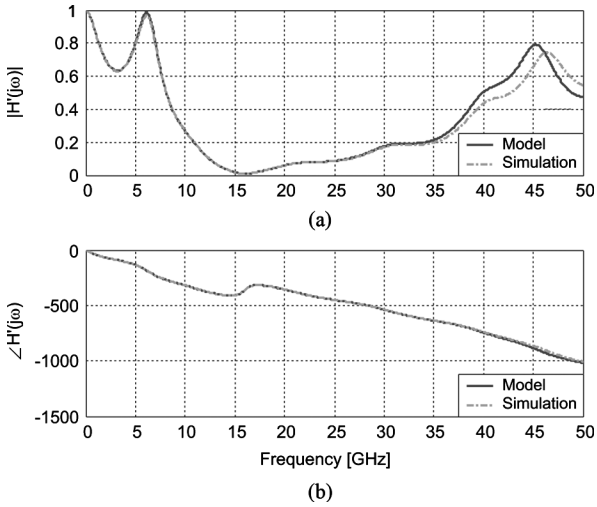

Fig. 13. Frequency response of the transfer function: (a) magnitude; (b) phase.

The receiver is based on the topology proposed in Fig. 6(b) and the transistor widths are listed in Table I. The input capacitance of the receiver circuit [i.e., the first buffer shown in Fig. 6(b)] is $C_l = 17.4$ fF.

Once the capacitive load of the interconnect is known, L_s, l_d, and R_d are determined to minimize power and delay. The minimum power-delay product as a function of the on-chip inductance, using (5) to (18), is shown in Fig. 11(a). The corresponding insertion point and driver resistance as a function of the on-chip inductance are shown in Figs. 5(b) and (c), respectively. As evident from Fig. 11, the minimum power-delay product occurs when an inductor $L_s = 7.5$ nH, inserted at $l_d = 4.3$ mm, and a driver resistance of $R_d = 195\ \Omega$ are used. For these parameters, the power consumption and signal delay of the QRN are shown in Fig. 12.

The magnitude and phase of the QRN transfer function are depicted in the frequency domain, in Fig. 13. Good agreement between simulations and the proposed analytic expressions for the magnitude and phase of the transfer function is achieved, exhibiting a maximum error of 19.5% and 2.8%, respectively. At a 5-GHz frequency, the magnitude of the transfer function is near resonance, here described as *quasi-resonance*. This behavior occurs since the addition of the parasitic capacitance of the on-chip spiral inductor reduces the resonant frequency, i.e., $1/2\pi(LC)^{1/2}$. The resonance peak, therefore, shifts to a higher frequency. Note that the magnitude of the transfer function reaches 0.8 at a 5-GHz frequency, as determined from (5).

The real and imaginary parts of the network input impedance are shown in Fig. 14. With an on-chip inductor $L_s = 7.5$ nH operating at 5 GHz, the input impedance of the network is $Z_{\text{in}} = 110 + j55$. Good agreement between simulations and the proposed analytic expressions for the magnitude and phase of the input impedance are achieved, exhibiting a maximum error of 4.3% and 37%, respectively.

The effect of the on-chip inductor on the magnitude of the transfer function is shown in Fig. 15. In this example, the magnitude of the transfer function reaches 0.8 with a 7.5-nH on-chip

TABLE II
SIMULATED AND ANALYTIC POWER CONSUMPTION AND DELAY OF THE RECEIVER, TRANSMITTER, AND QRN

	Simulation		QRN		Total		
	Receiver	Transmitter	Model	Simulation	Model	Simulation	Error %
Power [mW]	0.45	0.34	0.88	1.18	1.67	1.90	12.11
Delay [psec]	27.50	86.00	74.00	80.00	187.50	193.50	3.10

TABLE III
COMPARISON OF QRN MODEL WITH SIMULATION

Length [mm]	L_s [nH]	l_d [mm]	Analytic model			Simulation				Error	
			R_d [Ω]	Power [mW]	Delay [psec]	Driver NMOS W/L [μm/μm]	Driver PMOS W/L [μm/μm]	Power [mW]	Delay [psec]	Power %	Delay %
0.5	1.5	0	344	0.87	132	5.0 / 0.18	12.5 / 0.18	0.95	136	8.4	2.9
1	1.5	0.96	262	0.89	136	6.0 / 0.18	15.0 / 0.18	0.92	148	3.3	8.1
3	7.0	2.73	230	1.12	163	7.0 / 0.18	17.5 / 0.18	1.27	168	11.8	2.9
5	7.5	4.30	195	1.61	187	8.0 / 0.18	20.0 / 0.18	1.91	193	15.7	3.1
10	7.5	8.80	102	2.56	248	11.0 / 0.18	27.5 / 0.18	2.54	263	0.8	5.7
14	7.5	12.74	39	3.48	290	14.0 / 0.18	35.0 / 0.18	2.80	309	19.5	6.1
20	7.5	19.20	22	4.63	425	16.0 / 0.18	40.0 / 0.18	3.16	368	31.7	13.4
Average error										13.1	6.1

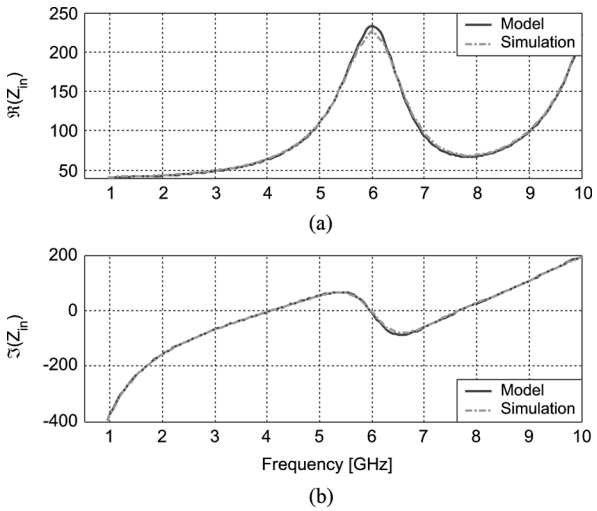

Fig. 14. QRN input impedance: (a) real part; (b) imaginary part.

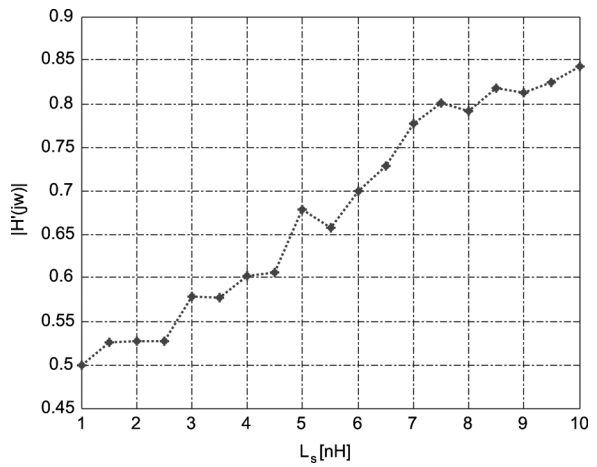

Fig. 15. Magnitude of the transfer function as a function of inductance at a 5-GHz operating frequency.

inductor. This behavior implies that a full swing voltage waveform is delivered at the far end only for this inductance.

The driver in this example is a 0.18-μm CMOS inverter with $\mathrm{P/N} = 20/8$. The transmitter is based on the proposed circuit shown in Fig. 5(c), and the transistor widths are listed in Table I. The transmitter circuit load capacitance (i.e., the input capacitance of the driver) is 52.4 pf. The simulated input and output data signals described in the time domain are shown in Fig. 16. Note that the square data waveform is distributed to the far end, achieving a full rail-to-rail voltage swing. In this example, a "1000101111" bit stream is transmitted at 5 Gb/s. The simulated and analytic power consumption and delay of the receiver, transmitter, and QRN circuits are listed in Table II.

To evaluate the noise performance of the QRN for this case study, eye diagrams of nonresonant and quasi-resonant interconnects are generated by transmitting a random bit stream. To represent a noisy environment, the power supply and ground signals are corrupted by the addition of Gaussian noise, as shown in Fig. 17(a). The injected noise signal includes low frequencies to emulate the resonances produced by the package inductance and capacitance. From Fig. 17(c), observe that a large open eye is formed, exhibiting a high signal-to-noise ratio. The high noise rejection exhibited by the QRN is attributed to the detection and transmission of a single harmonic when a high logic level is transmitted. An eye diagram of an interconnect with repeaters is shown in Fig. 17(b). The jitter of the quasi-resonant interconnect (40 ps) is two times less than the nonresonant interconnect (80 ps).

VI. SIMULATION RESULTS AND COMPARISON

To evaluate the accuracy of the model as compared to simulations, a 5 Gb/s data signal and 0.5, 1, 3, 5, 10, 14, and 20 mm length interconnects are considered, as listed in Table III. Good agreement between simulation and the model is demonstrated, exhibiting an average error of 13.1% and 6.1%, respectively, for

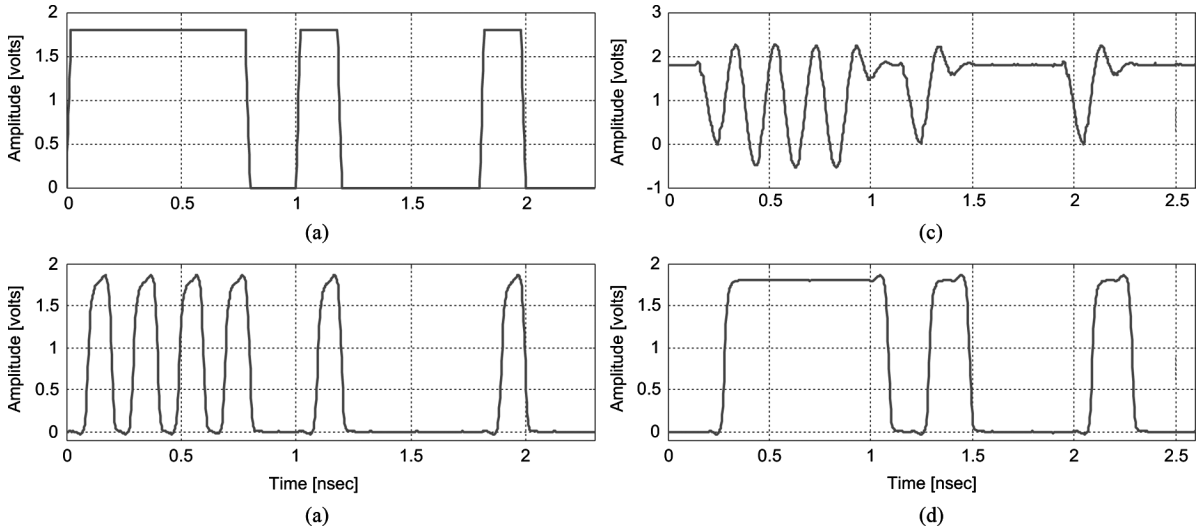

Fig. 16. Ten bit data stream example: (a) data at input of transmitter; (b) data at output of transmitter; (c) data at input of receiver; (d) data at output of receiver.

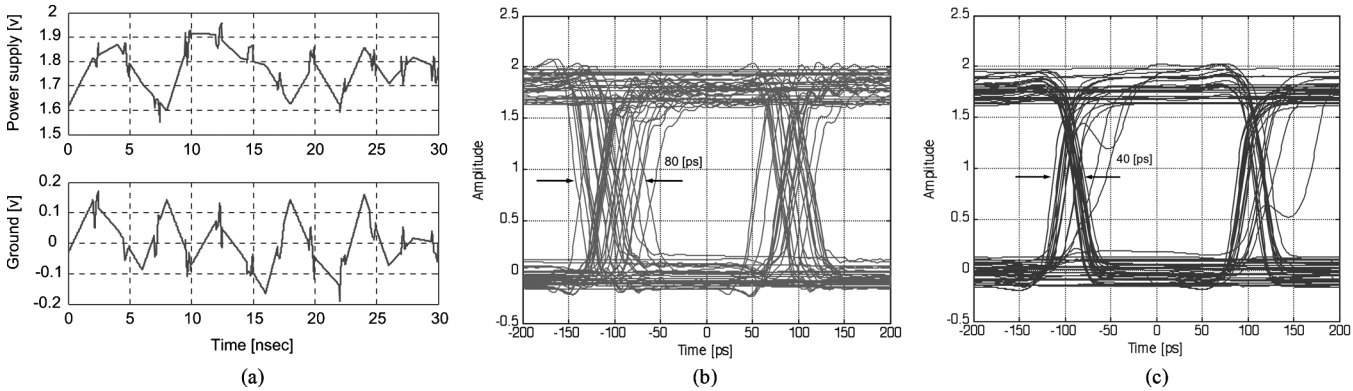

Fig. 17. Noise analysis: (a) noisy power supply and ground signals; (b) eye diagram of an interconnect with repeaters; (c) eye diagram of quasi-resonant interconnect.

TABLE IV
COMPARISON OF POWER CONSUMPTION AND DELAY

Length [mm]	This work		Repeater insertion		Improvement	
	Power [mW]	Delay [ps]	Power [mW]	Delay [ps]	Power %	Delay %
0.5	1.02	136	5.92	104	82.8	-23.5
1	0.99	148	10.79	160	90.8	7.5
3	1.34	168	16.87	255	92.1	34.1
5	1.98	193	25.20	368	92.1	47.5
10	2.61	263	51.20	1100	94.9	76.1
Average improvement					90.5	28.3

TABLE V
PERFORMANCE COMPARISON OF QUASI-RESONANT METHOD WITH DIFFERENT APPROACHES

	Technology [nm]	Speed [Gbps]	Length [mm]	Power [mW]	Delay [ps]
This work	180	5	3	1.34	168
Signal modulation [9]	180	8	3	27.12	280
Improvement				20X	40.0%
This work	180	5	20	3.23	368
Pulsed current [10]	180	1	20	16	300
Improvement				5X	-18.5%
This work	180	5	5	1.91	193
Optics (edge emitting) [11]	250	3	5	78	260
Improvement				40X	25.8%
This work	180	5	5	1.98	193
Optics (VCSEL) [11]	250	3	5	66	300
Improvement				33X	35.6%
This work	180	5	14	2.8	309
Loss compensation [20]	180	3	14	6	140
Improvement				2X	-54.7%

the power consumption and delay. The main reason for these discrepancies is due to the assumption of a linear driver model.

To evaluate the proposed methodology as compared to a traditional buffer insertion method, a 5 Gb/s data signal and 0.5, 1, 3, 5, and 10 mm length interconnects are considered, as listed in Table IV. It is a challenge to design repeaters to drive long interconnects at frequencies as high as 5 GHz in a 0.18-μm CMOS technology. Hence, signal integrity in this repeater insertion case has been compromised for the sake of this comparison. From Table IV, the average reduction in power consumption and delay is 91.1% and 37.8%, respectively. The performance improvement is due to the repeaterless nature of the quasi-resonant interconnect.

A comparison between the proposed methodology and other aggressive approaches described in the literature is listed in Table V. Interestingly, the greatest reduction in power consumption of 97.1% and delay of 35.6% occurs as compared to

TABLE VI
AREA COMPARISON OF REPEATERS AND ON-CHIP SPIRAL INDUCTORS FOR DIFFERENT TECHNOLOGIES

Length	Repeater insertion [μm^2]		Quasi-resonant [μm^2]		Area overhead	
[mm]	180 [nm]	50 [nm]	180 [nm]	50 [nm]	180 [nm]	50 [nm]
0.5	19	57	9063	1007	480X	17X
1	32	96	9063	1007	288X	10X
3	44	132	6803	756	155X	6X
5	63	189	6722	747	107X	4X
10	126	378	6722	747	53X	2X

optoelectronic links [11]. The power consumption overhead in [11] is due to the edge emitting laser modulator at the transmitting edge and the photodiode and signal level restorer at the receiving end of the optical link. This comparison suggests that novel signaling schemes incorporating electrical interconnects outperforms optoelectronic solutions. These results are obtained despite the optical link transmitting a slower signal (3 Gb/s) as compared to the resonant link (5 Gb/s).

With the exception of pulsed current [9], the resonant link transmits a higher frequency signal than the other methods. The proposed quasi-resonant interconnect methodology outperforms all of the other approaches described in the literature in power and, in most cases, in both power and latency. The primary tradeoff of the proposed methodology is the large area occupied by the on-chip inductor. This additional area is required to achieve a high Q inductor. In more advanced technologies, however, the area required for these inductors will be much lower. A comparison of the total area of repeaters and quasi-resonant methods for different technology nodes is listed in Table VI. The reduction in area overhead for a 50-nm CMOS technology is due to the requirement to insert additional repeaters to overcome the losses associated with long thin wires. Concurrently, the area of the on-chip inductor is lower due to the decrease in wire width and spacing.

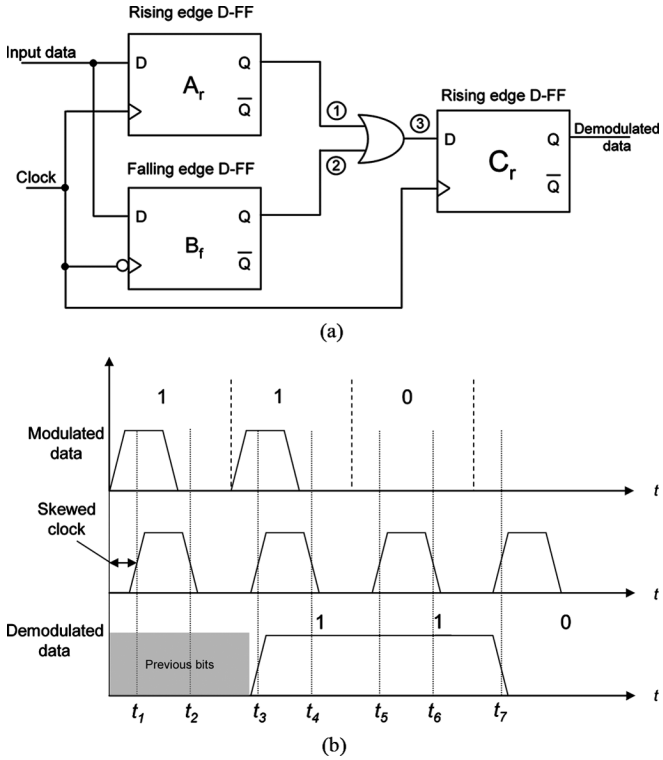

Fig. 18. Alternative receiver circuit: (a) gate implementation; (b) timing diagram.

VII. CONCLUSION

A methodology is described in this paper for designing quasi-resonant interconnect networks. An accurate model is presented based on transmission line theory and a lumped high frequency model of an on-chip spiral inductor. The accuracy of the model enables the design of low power, low latency resonant communication links. The methodology can be used to determine the specific inductance L_s, insertion point l_d, and driver resistance R_d that minimizes the power-delay product.

Good agreement between the proposed model and simulation is exhibited, achieving an average error of 13.1% and 6.1% for the power consumption and delay, respectively. Quasi-resonant interconnects are shown to outperform other technologically aggressive circuit approaches. For buffered lines, an average reduction of 90.5% and 28.3% is obtained in power consumption and delay, respectively. As compared to optical links, a reduction of 97.0% and 35.6% is observed in power consumption and delay, respectively. These results show that quasi-resonant interconnects exhibit superior performance, suitable for high performance, high complexity integrated circuits.

APPENDIX A
ALTERNATIVE RECEIVER CIRCUIT

The receiver circuit located at the far end of the interconnect (see Fig. 2) demodulates the transmitted data into the original signal. The proposed receiver circuit and timing diagram are depicted in Fig. 18.

The receiver circuit consists of three D flip-flops and an OR gate, as shown in Fig. 18(a). This circuit demodulates the received data regardless of the relative skew between the clock and the modulated signal. Note that A_r and C_r are rising edge flip-flops, and B_r is a falling edge flip-flop.

As an example of the operation of the demodulation circuit, consider the timing diagram shown in Fig. 18(b). At time t_1 (rising edge of the clock), A_r senses logic high of the input signal and transfers the signal to node 1. At this point, the output of the OR gate may not be correct. At time t_2 (falling edge of the clock), B_f senses logic low and transfers the signal to node 2. At this point, node 3 is logic high. On the next rising edge of the clock (time t_3), C_r transfers a logic high signal at node 3 to the output. At the same time, A_r senses the next modulated bit. If logic low is sensed by both A_r and B_f, logic low is transferred

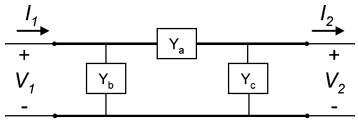

Fig. 19. Simplified admittance network for the spiral inductor model.

to the output (as demonstrated in the timing diagram depicted in Fig. 18(b) at time t_7). The demodulated signal at the output is synchronized with the clock. Note that the delay of the demodulation circuit is relative to the introduced skew. Also note that the skew can be either positive or negative.

Appendix B
ABCD Matrices of the Quasi-Resonant Network

The ABCD matrix for a transmission line as depicted in Fig. 7 is

$$M_{int1} = \begin{bmatrix} \cosh\gamma l & Z_0 \sinh\gamma l \\ \frac{1}{Z_0}\sinh\gamma l & \cosh\gamma l \end{bmatrix} \tag{A1}$$

where Z_0, γ, and l are the characteristic impedance, propagation constant, and line length, respectively. Similarly, M_{int2} is

$$M_{\text{int2}} = \begin{bmatrix} \cosh\gamma (l-l_d) & Z_0 \sinh\gamma (l-l_d) \\ \frac{1}{Z_0}\sinh\gamma (l-l_d) & \cosh\gamma (l-l_d) \end{bmatrix}. \tag{A2}$$

To derive the *ABCD* matrix M_s, the spiral inductor depicted in Fig. 3(b) is simplified into the network shown in Fig. 19.

From this network, the *ABCD* matrix is

$$M_s = \begin{bmatrix} 1+\frac{Y_c}{Y_a} & \frac{1}{Y_a} \\ Y_b + Y_c + \frac{Y_b Y_c}{Y_a} & 1+\frac{Y_1}{Y_3} \end{bmatrix} \tag{A3}$$

where

$$Y_a = \frac{1}{j\omega L_{\text{series}} + \frac{R_{\text{ac}}(R_{skin}+j\omega L_{\text{skin}})}{R_{\text{ac}}+R_{\text{skin}}+j\omega L_{\text{skin}}}} + j\omega C_p \tag{A4}$$

$$Y_b = \frac{1}{\frac{1}{(j\omega C_{\text{ox1}})} + \frac{\left(\frac{R_{\text{sub1}}}{j\omega C_{\text{sub1}}}\right)}{\left(\frac{R_{\text{sub1}}+1}{j\omega C_{\text{sub1}}}\right)}} \tag{A5}$$

$$Y_c = \frac{1}{\frac{1}{(j\omega C_{\text{ox2}})} + \frac{\left(\frac{R_{\text{sub2}}}{j\omega C_{\text{sub2}}}\right)}{\left(\frac{R_{\text{sub2}}+1}{j\omega C_{\text{sub2}}}\right)}}. \tag{A6}$$

Finally, the *ABCD* matrix of the capacitive load is

$$M_l = \begin{bmatrix} 1 & 0 \\ j\omega C_l & 1 \end{bmatrix}. \tag{A7}$$

Appendix C
Derivation of the Quasi-Resonant Network Delay Expression

The transfer function of the QRN at each angular frequency can be represented as

$$H'(j\omega) = \left|H'(\omega)\right| e^{j\beta(\omega)} \tag{B1}$$

where $\beta(\omega)$ is the phase of the transfer function. The output waveform in the time domain for a linear system, described by a transfer function such as (B1) and stimulated by a periodic square signal, can be approximated by

$$V_{\text{out}}(t) \approx \frac{V_{\text{dd}}}{2} + A_1 \sin(\omega_p t + \phi_1) + A_3 \sin(3\omega_p t + \phi_3) \tag{B2}$$

where

$$A_{m=1,3} = \frac{2t_p V_{\text{dd}}}{t_r m^2 \pi^2} \left|\sin\left(\frac{m\omega_p t_r}{2}\right)\right| \left|H'(m\omega_p)\right| \tag{B3}$$

and

$$\phi_{m=1,3} = -\frac{m\omega_p t_r}{2} + \beta(m\omega_p). \tag{B4}$$

Note that the approximated closed-form solution in (B2) is available only when considering the first three harmonics of the input signal. To determine the 50% delay, (B2) is set to $V_{\text{dd}}/2$. A third-order trigonometric expression can be obtained as

$$a_3 x^3 + a_2 x^2 + a_1 x + a_0 = 0 \tag{B5}$$

where $x = \tan(\omega_p t)$ and

$$a_0 = A_1 \sin\phi_1 + A_3 \sin\phi_3 \tag{B6}$$

$$a_1 = A_1 \cos\phi_1 + 3A_3 \cos\phi_3 \tag{B7}$$

$$a_2 = A_1 \sin\phi_1 - 3A_3 \sin\phi_3 \tag{B8}$$

$$a_3 = A_1 \cos\phi_1 - A_3 \cos\phi_3. \tag{B9}$$

A third order polynomial such as (B5) has either one or three real roots, and a closed-form solution exists. In the case of a single real root x_0, the 50% delay can be calculated from (18).

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