Corrections to "Unified Logical Effort—A Method for Delay Evaluation and Minimization in Logic Paths With *RC* Interconnect"

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In the paper [1], the formula and the caption in Fig. 3 appeared incorrectly. The correct figure is provided at the bottom of the page along with an explanation.

Manuscript received May 21, 2010. Date of publication July 01, 2010; date of current version July 23, 2010.

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Digital Object Identifier 10.1109/TVLSI.2010.2052421

The only resistive component at the right-hand side of the optimal size expression is R_{i+1}. The formula in Fig. 3 should be similar to the optimum condition (11) in the original paper [1].

The optimum condition of ULE is

$$(R_i + R_{w_i}) \cdot C_{i+1} = R_{i+1} \cdot \left(C_{i+2} + C_{w_{i+1}}\right). \tag{11}$$

The meaning of (11) is that the optimum size of gate $i+1$ is achieved when the delay component $(R_i + R_{w_i}) \cdot C_{i+1}$ due to the gate capacitance is equal to the delay component $R_{i+1} \cdot (C_{i+2} + C_{w_{i+1}})$ due to the effective resistance of the gate. Note that the other delay components $(R_i \cdot C_{w_i}, 0.5 \cdot R_{w_i} \cdot C_{w_i}, R_{w_{i+1}} \cdot (0.5 \cdot C_{w_{i+1}} + C_{i+2}))$ are independent of the size of gate $i+1$ and do not influence the optimum size.

References

[1] A. Morgenshtein, E. G. Friedman, R. Ginosar, and A. Kolodny, "Unified logical effort—A method for delay evaluation and minimization in logic paths with *RC* interconnect," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 18, no. 5, pp. 689–696, May 2010.

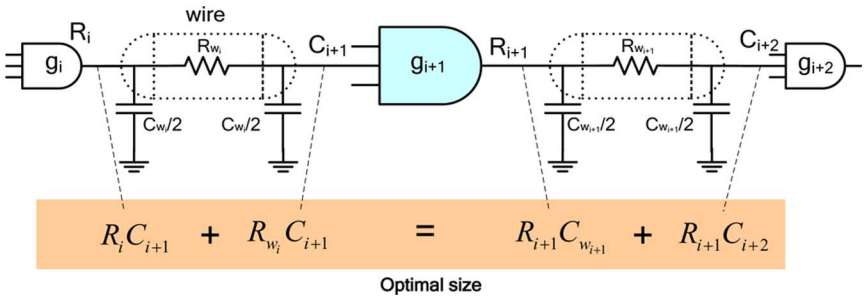

Fig. 3. Delay components in optimum ULE.