A Distributed Filter Within a Switching Converter for Application to 3-D Integrated Circuits

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***Abstract*—A design methodology for distributing a buck converter filter for application to 3-D circuits is described. The 3-D filter exploits transmission line properties, permitting the generation and distribution of power supplies to different planes. As compared to a conventional *LC* filter, the proposed filter only requires on-chip capacitors without the use of on-chip inductors. Additionally, the physical structure of the filter simultaneously enables the distribution of the current to the load while filtering the switching signal at the input. A case study in a 0.18-μm CMOS 3-D technology demonstrates the generation of a 1.2 V power supply delivering 700 mA peak current.**

***Index Terms*—3-D integrated circuits, dc-dc buck converters, distributed filters.**

I. Introduction

IN THE ERA of rapid technology scaling, the performance and reliability of integrated circuits (IC) have reached limits that are difficult to surpass. As a result, novel design methodologies for high performance, high complexity ICs are required. 3-D nanoscale technology can provide the required characteristics of future state-of-the-art integrated systems. With 3-D circuits [1], new design challenges arise. One primary requirement of 3-D integrated systems is diverse, high quality, and reliable power [2]. This fundamental issue of power generation and distribution in 3-D circuits is explored in this paper.

3-D integrated circuits are comprised of multiple planes with many circuit domains. The different planes are typically dedicated to a specific function, forming a highly heterogeneous system [1], [3], [4]. As an example, RF, analog, communications, and digital circuits are typically located on different planes, requiring several power supply voltages, as illustrated in Fig. 1. In this example, $V_{\rm dd1}$, $V_{\rm dd2}$, $V_{\rm dd3}$, and $V_{\rm dd4}$ are generated from the primary power supply $V_{\rm dd}$.

Multiple circuit domains require several power supplies to reliably operate and provide sufficient and stable current. To provide circuit domains with the appropriate power supplies, dc-dc converters are distributed across each plane [5] as it is often impractical to provide external power supplies due to the limited number of input pins. Moreover, planes located far from the faces of the 3-D cube require a large number of expensive 3-D vias to distribute the power supply across the plane.

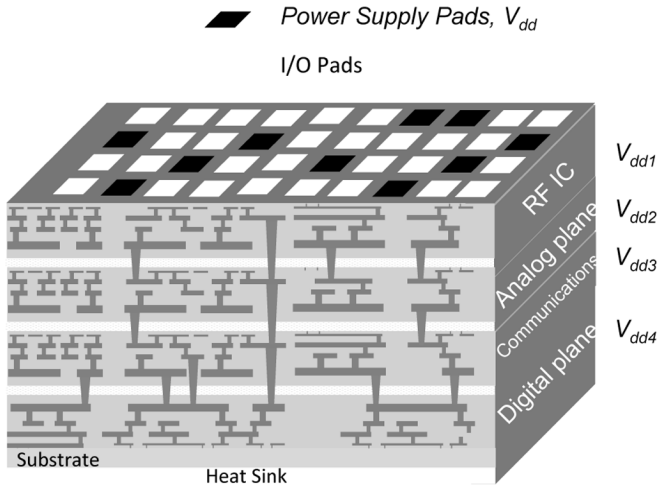

Fig. 1. 3-D circuit with multiple power supplies.

To alleviate these difficulties, dc-dc converters are distributed on-chip, generating a specific voltage required by the different circuit blocks within each plane of a 3-D system. A suitable dc-dc converter for low power applications is a buck converter [5], [6]. A buck converter generates an output supply voltage smaller than the input supply voltage [5].

The filter portion of a buck converter to generate and distribute power supplies in 3-D integrated circuits is the primary focus of this paper. The proposed filter is comprised of on-chip interconnects and capacitors, eliminating the need for an on-chip inductor [7]. For a specific dc voltage ripple, the distributed filter produces the target transfer function, passing the dc component of the input signal while attenuating the high frequency harmonics.

This paper is organized into five sections. Background on the operation of a conventional buck converter is reviewed in Section II. In Section III, a methodology for designing these circuits is described. To exemplify the proposed approach, a case study is described in Section IV, while a performance analysis of the distributed filter is presented in Section V. Some conclusions are offered in Section VI.

II. Background

A standard topology of a buck converter for high performance microprocessors is depicted in Fig. 2(a) [5]. The power MOSFETs produce an ac signal at node A by a signal controlled by a pulse width modulator (PWM) [8], [9], as shown in Fig. 2(b).

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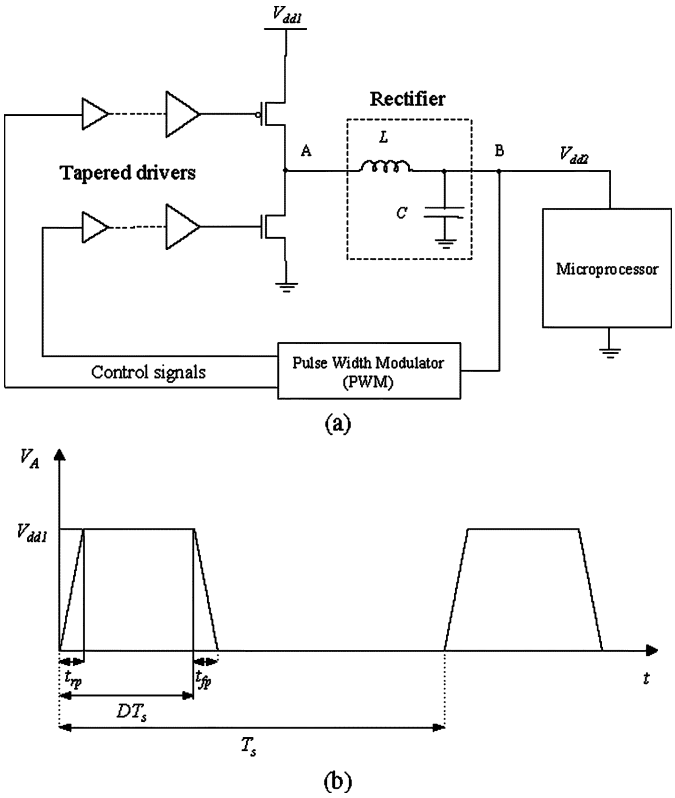

Fig. 2. Conventional dc-dc converter: (a) buck converter circuit [5] and (b) signal at the output of the power MOSFETs (node A).

The ac signal at node A is filtered by a filter composed of a second-order low pass band *LC* filter. Assuming the resonance frequency $1/2\pi\sqrt{LC}$ is less than the switching frequency of the power MOSFETs, the filter only passes the dc component of the signal and a residue composed of the high frequency harmonics. The dc component of the signal shown in Fig. 2(b) is

$$\frac{1}{T_s}\int_0^{T_s} V_A\,dt = \frac{V_{\rm dd1}(2DT_s - t_{rp} + t_{fp})}{2T_s} \tag{1}$$

where D, T_s, and $V_{\rm dd1}$ are the duty cycle, time period, and input power supply, respectively, and t_{rp} and t_{fp} are the rise and fall times, respectively, of the switching signal produced by the PWM circuit. In the case of $t_{rp} = t_{fp}$, (1) reduces to

$$V_{\rm dd2} = V_{DC|t_{rp}=t_{fp}} = DV_{\rm dd1}. \tag{2}$$

Hence, the buck converter produces an output voltage $V_{\rm dd2}$ at node B equal to $DV_{\rm dd1}$.

The power transistors are typically large in physical size and are therefore driven by tapered buffers [10]. These buffers are controlled by the PWM circuit. The feedback PWM circuit senses the output voltage supply $V_{\rm dd2}$ at node B and modifies the control signal to ensure that the appropriate duty cycle D is produced at node A. In this manner, the output voltage is maintained at the desired value while compensating for variations in the load current and input voltage. The performance and functionality of the different circuit domains under load current and dc input voltage variations are dependent upon the maximum voltage fluctuations generated by the buck converter, which is therefore regulated to provide the target voltage [5].

The performance of a buck converter can be improved by integrating these converters on-chip. In this manner, the parasitic losses associated with the interconnects among the nonintegrated components of the dc-dc converter are significantly decreased. Moreover, integrated converters benefit by advances in on-chip technologies and high operating frequencies. Monolithic fully integrated dc-dc converters can therefore achieve higher efficiency as compared to nonintegrated converters [11]–[14].

Integrating dc-dc converters on-chip in both 2-D and 3-D technologies, however, imposes challenges as the on-chip integration of large inductive and capacitive elements is problematic. A significant issue is the poor parasitic impedance characteristics exhibited by the on-chip inductors [15], [16], which degrades the performance of the on-chip converter. To improve the quality factor of a 2 nH inductor and reduce the ripple current within the inductors, magnetic coupling between two on-chip inductors has been used in a dc-dc converter [17]. Although the size and magnitude of the on-chip inductors and capacitors required to implement a buck converter are reduced with increasing switching frequency, the on-chip passive devices comprising the filter are large and cannot be practically integrated in the megahertz frequency regime [18]–[20].

A 3-D technology provides several advantages as compared to a 2-D technology. When the on-chip capacitors used by a distributed filter are implemented with active devices, less metallization resources are required to connect these capacitors to different sections of the filter as compared to a 2-D technology. Since in 3-D circuits each plane has a dedicated active device layer, routing congestion is reduced due to the smaller distance between the interconnect and the corresponding capacitor. Also, in a 2-D technology, the input power supply to the power MOSFETs (which are located within the substrate) is connected by the lowest metal layers, therefore, additional routing resources are required.

In a 3-D technology, the plane closest to the input power supply accommodates the power MOSFETs, saving metallization resources. The capacitance and inductance of the through silicon vias are exploited, reducing the required length of the interconnects and the size of the capacitors. An inherent benefit of utilizing the proposed filter in 3-D systems is that the generation and distribution of the power supply occur simultaneously, while in a 2-D technology, the filter is only used to generate the power supply.

To obtain insight into the operation of a distributed filter as compared to a lumped *LC* filter, consider the transfer function of two types of filters, as depicted in Fig. 3. A second-order low pass *LC* filter is used in a typical conventional dc-dc converter. When the effective output resistance R_d of the power MOSFETs as well as the effective series resistance of the inductor are included, two poles at different frequencies are formed, resulting in a roll-off slope of -20 dB/decade in the megahertz and -40 dB/decade in the gigahertz frequency range. The frequency behavior of a distributed filter in the megahertz frequency range is therefore similar to a lumped *LC* filter, as can be observed in Fig. 3. When R_d and the interconnect resistance are included in the analysis, a pole in the megahertz frequency is formed, resulting in a roll-off slope of -20 dB/decade. Note that in this

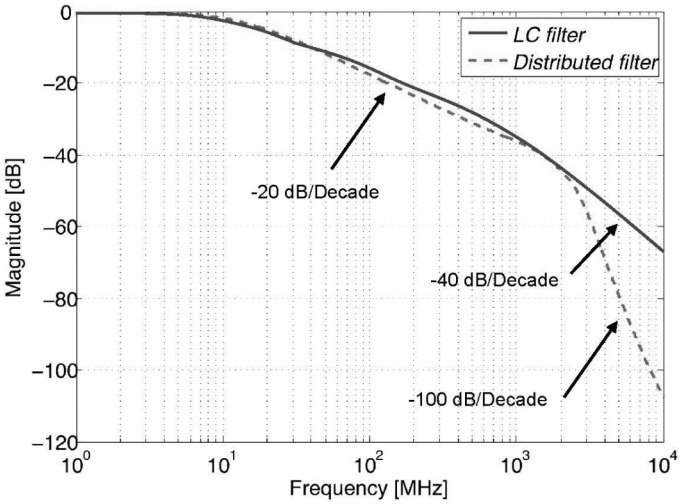

Fig. 3. Transfer functions of *LC* and distributed filters.

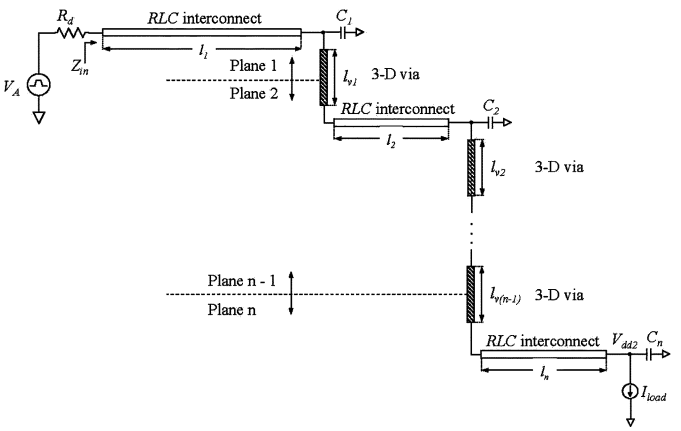

Fig. 4. Distributed filter.

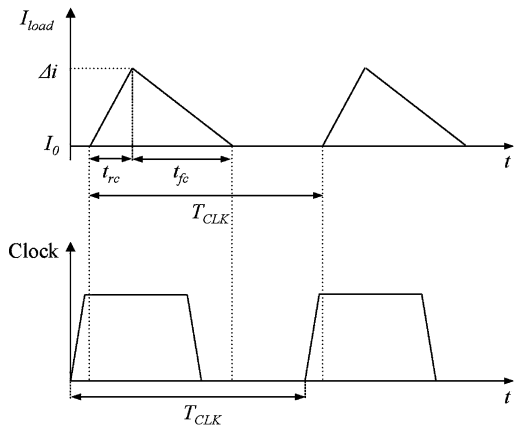

Fig. 5. Current load profile.

example, a sharp −100 dB/decade roll-off slope is formed in the gigahertz frequency range, suppressing the high frequency harmonics of the ac signal produced by the power MOSFETs. The distributed nature of the proposed filter forms multiple poles at approximately the same high frequency, resulting in a large negative slope.

III. Design Methodology

A design methodology for a distributed buck converter is described in this section. Design guidelines are provided based on the expressions developed here. The physical structure of the distributed filter as well as the current load characteristics are described in Section III-A. In Section III-B, the transfer function of the filter is used to determine the condition that satisfies a target power supply ripple while the efficiency and area of the 3-D filter are determined in Section III-C. Finally, design guidelines are described in Section III-D.

A. Physical Structure and Current Load Properties of a 3-D Filter

The proposed distributed filter is depicted in Fig. 4. The filter is driven by power MOSFETs [see Fig. 2(a)] which are modeled as a voltage source V_A followed by an effective resistance R_d. The voltage source V_A is assumed to be periodic, as illustrated in Fig. 2(b).

The filter is composed of transmission lines terminated with lumped capacitances. The inter-plane structure is connected by 3-D vias. At the target plane n, the load is represented by a periodic current load and a reference clock signal, as shown in Fig. 5. Note that the current load characterizes the approximate current profile of a specific circuit module on a plane. $I_{\rm load}$ remains at I_0 during clock low, providing dc current flow by the power supply. As with a conventional buck converter, a feedback PWM circuit senses the output node of the filter and adjusts the duty cycle of the signal driving the power MOSFETs [see Fig. 2(a)].

In 3-D circuits, the ability to deliver current is primarily limited by the 3-D vias. The maximum current that can be delivered through a single 3-D via therefore determines the current magnitude

$$I_0 + \Delta i = J_{\rm via,max} \cdot A_{\rm via} \cdot V \tag{3}$$

where $J_{\rm via,max}$, $A_{\rm via}$, and V are, respectively, the maximum current density, cross-sectional area, and number of 3-D vias on the same plane. Consequently, the maximum cross-sectional area of the interconnects (see Fig. 4) distributing the current within the different planes is

$$A_{\rm int} = \frac{I_0 + \Delta i}{J_{\rm int,max}} = \left(\frac{J_{\rm via,max}}{J_{\rm int,max}}\right) \cdot A_{\rm via} \cdot V \tag{4}$$

where $J_{\rm int,max}$ is the maximum current density of the interconnect.

In practical circuits, however, a significant amount of current is sunk by the load. To satisfy this requirement, multiple structures N, as depicted in Fig. 4, are connected in parallel, delivering $N(I_0 + \Delta i)$ amperes. In this case, the number of 3-D vias within the filter on each plane is equal to the number of parallel connected structures, $V = N$. The effective resistance and inductance per unit length of the interconnects and 3-D vias, as well as the output resistance of the driver (see Fig. 4), are N times smaller. The capacitance per unit length of the interconnects and 3-D vias, as well as the on-chip lumped capacitors, are N times larger.

B. Transfer Function of a 3-D Filter

To characterize the impedance of the filter (between R_d and I_{load}), the overall transfer function is determined based on the *ABCD* matrices. Hence, the overall *ABCD* matrix of a filter spanning n planes is

$$\begin{bmatrix} \tilde{A} & \tilde{B} \\ \tilde{C} & \tilde{D} \end{bmatrix} = \begin{bmatrix} 1 & R_d \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} A' & B' \\ C' & D' \end{bmatrix}. \tag{5}$$

The right matrix in the right-hand side of (5) is

$$\begin{bmatrix} A' & B' \\ C' & D' \end{bmatrix} = \prod_{i=1}^{n} \left(\begin{bmatrix} \cosh \gamma l_i & Z_0 \sinh \gamma l_i \\ \frac{\sinh \gamma l_i}{Z_0} & \cosh \gamma l_i \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_i & 1 \end{bmatrix} \cdot \begin{bmatrix} \cosh \gamma_v l_{vi} & Z_{v0} \sinh \gamma_v l_{vi} \\ \frac{\sinh \gamma_v l_{vi}}{Z_{v0}} & \cosh \gamma_v l_{vi} \end{bmatrix} \right) \tag{6}$$

where Z_0 and γ are the characteristic impedance and propagation constant of the *RLC* interconnects, respectively, l_i and C_i are the interconnect length and capacitance on the ith plane, respectively, Z_{v0} and γ_v are the characteristic impedance and propagation constant of the 3-D vias, respectively, and l_{vi} is the length of the 3-D via on the ith plane. The transfer function of the filter is

$$H_{\text{rect}}(j\omega) = \frac{1}{\tilde{A}} \tag{7}$$

where $\tilde{A}$ and $\tilde{B}$ are obtained from (5), and ω_{CLK} and ω_s are the radian frequency of the clock and switching signals, respectively.

Since a practical filter within a buck converter does not provide ideal low pass characteristics, the signal at node B, shown in Fig. 2(a), carries a small amount of high frequency harmonics generated by the switching power MOSFETs. Hence, the voltage at node B is

$$V_{\text{dd2}}(t) = V_{DC} + V_{\text{ripple}}(t) \tag{8}$$

where V_{DC} is the dc component of the output voltage described by (1) and $V_{\text{ripple}}(t)$ is the voltage ripple transferred by the nonideal characteristics of the filter. When only the fundamental harmonic is passed, $V_{\text{ripple}}(t)$ exhibits a sinusoidal behavior

$$V_{\text{ripple}}(t) = V_r \sin(\omega_s t). \tag{9}$$

To satisfy a target ripple voltage V_r (peak-to-peak), the magnitude of the filter transfer function at the switching frequency f_s has to be below a specific value. To satisfy this objective, consider the output signal in the frequency domain

$$|V_{\text{dd2}}(s)| = |H_{\text{rect}}(s)| \cdot |V_A(s)|. \tag{10}$$

The periodic input signal V_A can be represented by a Fourier series

$$v_A(t) = \sum_{k=-\infty}^{\infty} a_k e^{jk\omega_s t} \tag{11}$$

where a_k is the kth harmonic of the signal. In the case of the signal illustrated in Fig. 2(b) and assuming $t_{rp} = t_{fp} = t_r$, the fundamental harmonic (positive and negative) is

$$a_{\pm 1} = \left(\frac{V_{dd1} T_s}{4 t_r \pi^2} \right) \cdot \left(e^{\mp j\omega_s t_r} \left(1 - e^{\mp j2\pi D}\right) + e^{\mp j2\pi D} - 1 \right). \tag{12}$$

Equation (10) implies that the required amplitude of the transfer function for a specific ripple voltage V_r is

$$|H_{\text{rect}}(j\omega_s)| \leq \frac{\frac{V_r}{2}}{2|a_1|} = \frac{V_r}{4|a_1|}. \tag{13}$$

Once the current profile of a circuit is determined, the interconnect length l_1 to l_n, shown in Fig. 4, and the required ripple voltage V_r are chosen. Based on (7), the magnitude of the transfer function at ω_s is plotted as a function of the capacitances C_1 to C_n. The interconnect length and capacitance are chosen to satisfy (13). Since these design expressions are complex and unsuitable for manual calculations, numerical techniques are used.

An important issue is the duty cycle of the signal driving the power MOSFETs (see Fig. 4) that produces the correct power supply voltage. Note that in this case, the duty cycle determined from (2) does not provide the proper dc voltage level. This behavior occurs since the signal at the input of a distributed filter is degraded by the resistance R_d and the input impedance of the filter Z_{in}, forming a voltage divider. To obtain the duty cycle required for a specific dc voltage, consider the input impedance of the filter at DC

$$Z_{\text{in}}(0) = \frac{V_{DC} A'(0) + I_{DC} B'(0)}{V_{DC} C'(0) + I_{DC} D'(0)} \tag{14}$$

where A', B', C', and D' are defined in (6), and I_{DC} is the dc component of the current load

$$I_{DC} = I_0 + \frac{\Delta i}{2T_{\text{CLK}}} \cdot (t_{rc} + t_{fc}). \tag{15}$$

The dc component of the signal at the input of the filter (including R_d in Fig. 4) is

$$DV_{\text{dd1}} = D_{\text{PWM}} V_{\text{dd1}} \left| \frac{Z_{\text{in}}(0)}{Z_{\text{in}}(0) + R_d} \right| \tag{16}$$

the dc voltage transferred by the filter to the target plane. In (16), D_{PWM} is the duty cycle provided by the PWM feedback circuit [see Fig. 2(a)]. Consequently, to achieve a specific dc voltage at the output of the filter, the duty cycle in (2) is

$$D_{\text{PWM}} = D \cdot \left| 1 + \frac{R_d}{Z_{\text{in}}(0)} \right|. \tag{17}$$

Observe from (17) that D_{PWM} is always larger than the original duty cycle D obtained from (2), limiting the magnitude of the generated power supply. When the interconnects within the distributed filter are resistive, D_{PWM} approaches D (no reflections occur at the input). It is typically preferable to design the filter to ensure that D_{PWM} is closer to D to provide a large tuning range for the PWM circuit.

C. Efficiency and Area of a 3-D Filter

An important property of a buck converter is the power efficiency. The efficiency of a distributed filter within a buck converter is

$$\eta_{\text{rect}} = \frac{P_{\text{load}}}{P_{\text{load}} + P_{\text{rect}}} \times 100\% \tag{18}$$

where P_{load} is the average power delivered to the load and P_{rect} is the average power consumed by the filter. The power expressions P_{load} and P_{rect} are, respectively,

$$P_{\text{load}} = V_{\text{dd2}} I_{DC} \tag{19}$$

$$P_{\text{rect}} = V_{A,\text{rms}}^2 \left| \frac{Z_{\text{in}}(j\omega_s)}{Z_{\text{in}}(j\omega_s) + R_d} \right|^2 \cdot \Re\left\{ \frac{1}{Z_{\text{in}}(j\omega_s)} \right\} \tag{20}$$

where $V_{A,\text{rms}}$ is the root-mean-square value of the driving signal with a duty cycle D_{PWM}, and $Z_{\text{in}}(j\omega_s)$ are, respectively

$$V_{A,\text{rms}} = \sqrt{\frac{1}{T_s} \int_{t_0}^{t_0+T_s} |v_A(t)|^2 \, dt} \tag{21}$$

$$Z_{\text{in}}(j\omega_s) = \frac{V_{DC} A'(j\omega_s) + I_{DC} B'(j\omega_s)}{V_{DC} C'(j\omega_s) + I_{DC} D'(j\omega_s)}. \tag{22}$$

The area occupied by a 3-D filter is

$$A_{3-D,\text{rect}} = \left(\sum_{i=1}^{n} (W_{metal,i} \cdot l_i + A_{C_i}) + \sum_{i=1}^{n-1} A_{\text{via},i} \right) \cdot N + S_i \cdot l_i \cdot n \cdot (N-1) \tag{23}$$

where A_{C_i} and $A_{\text{via},i}$ are the area occupied by the on-chip capacitors and 3-D vias on the ith plane, respectively. $W_{\text{metal},i}$ and S_i are the width and spacing of the interconnects on the ith plane, respectively. As mentioned in Section III-A, n and N are, respectively, the number of planes spanned by the filter and the number of parallel connected filter structures. The generation and distribution of additional power supplies, as illustrated in Fig. 1, requires the use of additional dc-dc converters and distributed filters.

D. Design Guidelines

In order to provide a comprehensive perspective of the design space, several design parameters that affect the performance of the distributed filter are investigated. To determine the required magnitude of the transfer function of the filter for different output voltage ripples and dc voltages, consider Fig. 6. The output dc voltage ranges between 0.8 and 3 V (assuming a 3.3 V input dc voltage), while the required voltage ripple ranges between 1% and 10%. As expected, the magnitude of the transfer function increases for higher voltage ripple, since a larger amplitude of the dominant harmonic of the input signal is permitted to pass. Furthermore, as the output dc voltage becomes larger, an increase in the transfer function is evident in (10). Consequently, a lower capacitance and fewer resistive interconnects are required. Once the required output dc voltage is chosen for a specific voltage ripple, permitting the target magnitude of the transfer function to be determined, the design space of the distributed filter is specified.

In this example, all of the interconnect lengths are $l = 1$ mm with a voltage ripple $V_r = 5\%$, input dc voltage $V_{\text{dd1}} = 3.3$ V,

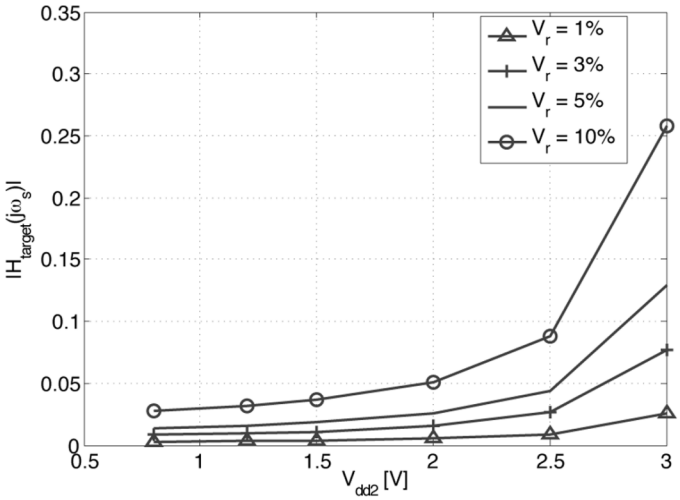

Fig. 6. Required magnitude of the transfer function.

and a switching frequency $f_s = 100$ MHz. Consider the design space of the filter, as shown in Fig. 7. The modified duty cycle D_{PWM}, ratio between the duty cycle D [see (2)] and D_{PWM}, capacitance, and filter efficiency are depicted as a function of the output dc voltage and series resistance R_d (see Fig. 4). The modified duty cycle D_{PWM} is shown in Fig. 7(a). Observations of Fig. 7(a) reveal that under the specified operating conditions, this filter cannot convert 3.3 to 3 V since for all values of R_d, D_{PWM} is greater than one. The feasible operation of the distributed filter is therefore limited to about 2.5 V.

To narrow the design space, recall that D_{PWM} is always greater than D (see Section III-B). To permit a larger operational range of the feedback PWM circuit, D_{PWM} should be chosen close to D. A new design metric is therefore defined which is the ratio of D to D_{PWM}, as shown in Fig. 7(b). This ratio should be as close to one as possible. As shown in Fig. 7(b), the ratio D/D_{PWM} decreases as R_d increases. The lowest permissible ratio D/D_{PWM} is chosen to be 0.5 to accommodate a tradeoff between the ratio D/D_{PWM} and the filter efficiency.

As mentioned in the beginning of this subsection, less capacitance is required for lower conversion ratios, as shown in Fig. 7(c). As expected, with a larger series resistance of the power MOSFETs R_d, the required capacitance can be decreased to satisfy the target magnitude of the transfer function. Finally, the filter efficiency η_{rect} is shown in Fig. 7(d). The general trend for all output DC voltages is that the filter efficiency increases with higher R_d, as evident from (18) and (20). From Figs. 7(b)–(d), the permissible range for R_d is

$$R_d(\min(\eta_{\text{rect}})) < R_d < R_d\left(\frac{D_{\text{PWM}}}{D} = \frac{1}{2}\right) \tag{24}$$

$$R_d(\max(C)) < R_d < R_d\left(\frac{D_{\text{PWM}}}{D} = \frac{1}{2}\right). \tag{25}$$

IV. Case Study

To demonstrate the design methodology described in Section III, an example DC-DC converter based on the MIT Lincoln Lab (MITLL) 180 nm 3-D integration process [21],

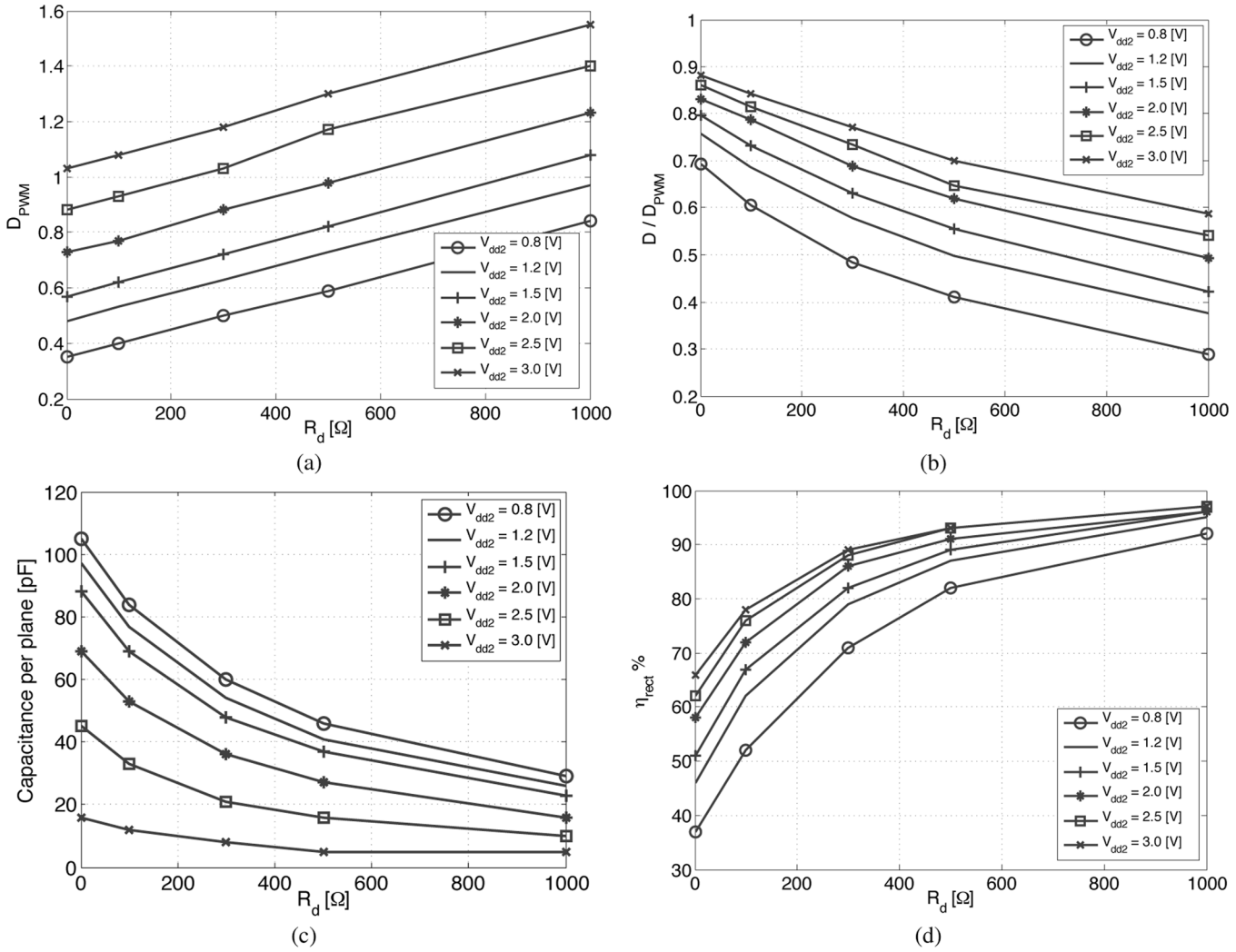

Fig. 7. Design space of a distributed filter: (a) modified duty cycle as a function of R_d; (b) duty cycle ratio as a function of R_d; (c) capacitance as a function of R_d; (d) filter efficiency as a function of R_d.

[22] is described in this section. Since the ability to deliver current is primarily limited by the 3-D via, characterization of the maximum current that can flow through a single via is described in Section IV-A. A distributed filter based on a 3-D technology is described in Section IV-B and compared to an implementation in a 2-D technology in Section IV-C. In order to quantify the advantages of the proposed distributed filter as compared to a conventional buck converter filter, a traditional filter is described in Section IV-D for the same performance requirements as a distributed filter. SPICE simulations are performed based on the 3-D MITLL technology.

A. Current Load Characterization

The MITLL technology is a 0.18 μm low power, fully depleted silicon-on-insulator (FDSOI) CMOS process where three independent wafers are physically bonded to form a 3-D integrated structure. Each plane has three aluminum metallization layers. In this technology, the maximum current density is [22]

$$J_{Al,3\text{-}D} = \frac{3 \text{ mA}}{\mu\text{m}^2}. \tag{26}$$

Since the cross-sectional area of a 3-D via in this technology is 1.5×1.5 μm^2, the maximum current that can flow through a single 3-D via, based on (3), is

$$I_0 + \Delta i \approx 7 \text{ mA}. \tag{27}$$

In this case study, the current load waveform, depicted in Fig. 5, has the following characteristics: $1/T_{\text{CLK}} = 3$ GHz, and t_{rc} and t_{fc} are $0.3T_{\text{CLK}}/2$ and $0.7T_{\text{CLK}}/2$, respectively.

B. Distributed 3-D Filter

To overcome the difficulty described in Subsection IV-D, a distributed filter circuit has been developed that generates and distributes the power supply to a target plane within a 3-D structure. This filter is described in this section. The resistance, inductance, and capacitance per unit length of the interconnects (Metal 3) and 3-D vias are extracted based on the predictive technology model (PTM) [23]–[25], as listed in Table I. The width of the interconnects is determined by the maximum current density of the MITLL 3-D technology. Assuming that both the interconnect and 3-D vias support the same current density

TABLE I
RLC INTERCONNECT (ALUMINUM) AND 3-D VIA IMPEDANCES

	R [$m\Omega/\mu$m]	L [pH/μm]	C [fF/μm]
Interconnects	14.5	1.3	0.5
3-D via [24]	20.40	0.55	0.37

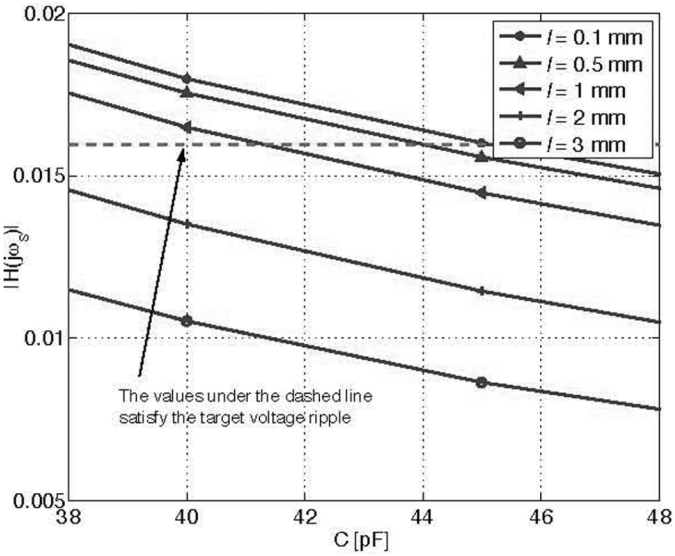

Fig. 8. Magnitude of the transfer function at ω_s for different line lengths and capacitances.

of 3 mA/μm^2, the maximum cross-sectional area of the interconnect determined from (4) is 1.5×1.5 μm^2. The thickness of the interconnect for this technology is 630 nm, resulting in an approximately 4 μm wide line. Note that each 3-D via is 7.34 μm long, connecting three planes, as illustrated in Fig. 4.

For the same performance requirements as a conventional filter, the magnitude of the transfer function at ω_s for different capacitances and interconnect lengths, assuming $l = l_1 = l_2 = l_3$ and $C = C_1 = C_2 = C_3$, is depicted in Fig. 8. An output resistance of the power MOSFETs $R_d = 7.36\ \Omega$ is assumed in this case study.

As the interconnect line length increases, less capacitance is required, as evident in Fig. 8. To satisfy the required voltage ripple, the target interconnect length in this example is $l = 1$ mm with a capacitance $C = 42$ pF. The dc voltage at the output of the filter is shown in Fig. 9. The simulated ripple of the output dc voltage is 52 mV (4.3% of the output dc voltage), satisfying the design objective of a maximum 5% voltage ripple. In this example, the required duty cycle of the signal driving the power MOSFETs is $D_{\rm PWM} = 0.73$, and the efficiency of the filter is about 88%.

If additional current is required, the distributed filter can be extended by connecting multiple structures in parallel. For example, to enlarge this structure to produce 700 mA, 100 parallel structures are required. In this case, the effective resistance and inductance per unit length, listed in Table I, and R_d are N times smaller, while the capacitance per unit length is N times larger. The multiple parallel filters produce the same transfer function magnitude, as shown in Fig. 8. The same interconnect

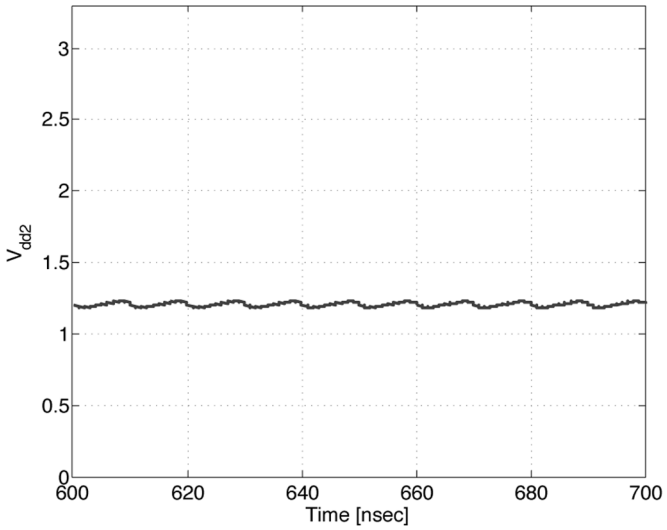

Fig. 9. DC voltage at the output of a distributed filter.

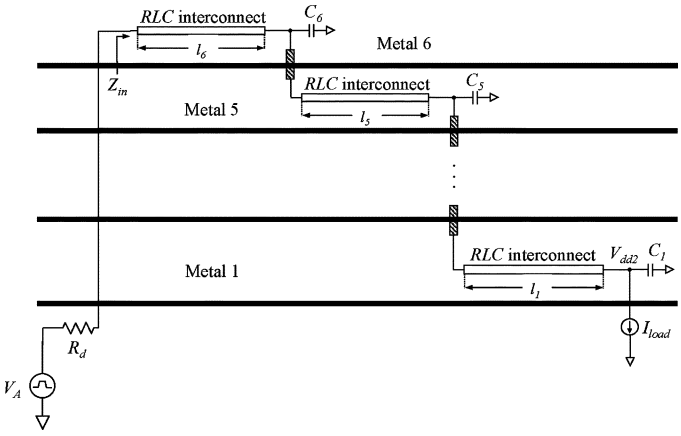

Fig. 10. Distributed filter in a 2-D technology.

lengths and capacitances are therefore chosen, producing a 1.2 volt power supply with 700 mA maximum current, resulting in a total of 4.2 nF/plane. The interconnect network and the capacitors per plane occupy, in this example, about 0.42 mm^2.

C. Distributed Filter in a 2-D Technology

As mentioned in Section II, the distributed filter can also be implemented in a 2-D technology, as shown in Fig. 10. In a 2-D technology, the filter spans all metal layers down to the device layer where conventional vias are used to connect the different metal layers.

To provide an effective comparison to the 3-D case, a 180 nm 2-D TSMC technology with six copper metal layers is used. Additionally, the width of all of the metal interconnects and the output resistance of the driver are assumed to be 4 μm and $R_d = 7.36\ \Omega$, respectively, as in the 3-D case. The *RLC* parameters for this technology are listed in Table II.

Following the same design methodology and performance requirements as used for the 3-D case, the magnitude of the transfer function at ω_s for different capacitances and interconnect lengths, assuming $l = l_1 = l_2 = l_3 = l_4 = l_5 = l_6$ and $C = C_1 = C_2 = C_3 = C_4 = C_5 = C_6$, is depicted in

TABLE II
RLC INTERCONNECT (COPPER) IMPEDANCES IN A 2-D TECHNOLOGY

	R [$m\Omega/\mu$m]	L [pH/μm]	C [fF/μm]
M_6	5.5	1.3	1.0
M_5, M_4, M_3, M_2, M_1	10.40	1.30	0.89

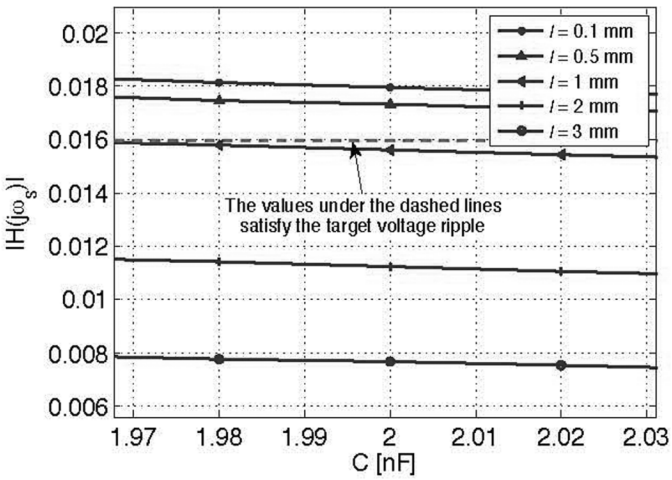

Fig. 11. Magnitude of the transfer function at ω_s for different line lengths and capacitances in a 2-D technology.

TABLE III
PERFORMANCE COMPARISON OF THE DISTRIBUTED FILTER IMPLEMENTED IN A 2-D AND 3-D TECHNOLOGY

	2-D 180 nm	3-D 180 nm
Capacitance density [fF/μm^2]	1	10
Total capacitance [nF]	12	4.2 (per plane)
filter efficiency [%]	88	88
Area [mm^2]	12.25	0.42

Fig. 11. To ensure a proper comparison with the 3-D case, the interconnect length in this example is also $l = 1$ mm, resulting in a capacitance $C = 2$ nF (see Fig. 11). The total on-chip capacitance in the 2-D case is therefore $2 \times 6 = 12$ nF. The required duty cycle of the signal driving the power MOSFETs is $D_{\rm PWM} = 0.73$, and the efficiency of the filter is about 88%. The area occupied by this filter is about 12.25 mm^2.

A comparison of the filter implemented in a 2-D and 3-D technology is provided in Table III. Note that the 3-D implementation exhibits better characteristics due to several reasons. The on-chip capacitance density is ten times larger in a 3-D technology, translating into a larger area occupied by the filter in a 2-D technology. Additionally, in the 3-D technology, the capacitance is distributed among the three planes. Furthermore, the capacitance required in the 2-D technology is 2.85 larger than the capacitance in the 3-D case.

The requirement for on-chip capacitance in the 2-D technology increases due to the following rationale. The cutoff frequency of the distributed low pass filter is proportional to $1/2\pi R_{\rm int} C_{\rm plane}$, where $R_{\rm int}$ is the total resistance of the filter interconnects and $C_{\rm plane}$ is the total on-chip capacitance connected to the interconnects on different planes, $C_{\rm plane} = \sum_{i=1}^{n} C_i$ (see Fig. 4). To maintain the same cutoff frequency as in the 3-D case and since $R_{\rm int}$ is lower in the 2-D case, the requirement for $C_{\rm plane}$ increases (in this example, by 2.85). The resistance $R_{\rm int}$ in the 2-D case is lower as compared to the 3-D technology since in the 2-D technology, copper interconnects are used while aluminum interconnects are used in the 3-D technology.

Finally, the efficiency of the filter in both cases is approximately the same (88%). Summarizing, the distributed filter requires significantly less total area when implemented within a 3-D technology as compared to a 2-D technology (in this example, 30 times less, as inferred from Table III).

D. Conventional Filter

A conventional buck converter filter is composed of a second order low pass *LC* filter, as shown in Fig. 2(a). Assuming the inductor and capacitor exhibit ideal characteristics, the transfer function of the *LC* filter is

$$H_{{\rm rect},LC}(j\omega) = \frac{1}{1 - \omega^2 LC + j\omega C R_d} \tag{28}$$

where R_d, L, and C are the effective output resistance of the power MOSFETs and the inductor and capacitor of the conventional filter, respectively.

In this example, a practical 2 nH on-chip inductor is used, based on the characterization in [17]. This inductor has been designed in a 130-nm CMOS technology, conducting 130 mA maximum current, with 75 μm line width and 600 μm diameter. In order to conduct 700 mA, five 2 nH inductors are connected in parallel, resulting in 0.4 pH total inductance. The dc-dc conversion is from 3.3 to 1.2 V ($D = 0.36$) at a switching frequency $f_s = 100$ MHz. The effective output resistance of the power MOSFETs in a 0.18-μm CMOS technology delivering 700 mA is $R_d = 7.36\,\Omega$. To achieve 5% ($V_r = 0.05 V_{\rm dd2}$ peak-to-peak) ripple voltage, the magnitude of the transfer function at 100 MHz according to (13) is 0.016. To satisfy these requirements, the corner frequency of an *LC* low pass filter, i.e., the resonant frequency, should be about one decade less than f_s.

This condition results in $C = 20$ nF and five $L = 0.4$ pH inductors. Note that for these performance requirements, significant area is required. The inductors and capacitor occupy about 4 mm^2 as compared to 0.42 mm^2 per plane occupied by the distributed filter.

V. PERFORMANCE ANALYSIS

To obtain deeper insight into the performance characteristics of the proposed filter, an analysis over a wide range of design parameters is presented in this section. In all cases, the filter is designed to satisfy less than 5% voltage ripple with an input 3.3 dc voltage. In the simulation of a 3-D filter, the parameters and structure presented in the case study discussed in Section IV are assumed.

To place these results in the context of a conventional filter, the inductor and capacitor values as a function of switching frequency for different current loads are illustrated in Fig. 12. As

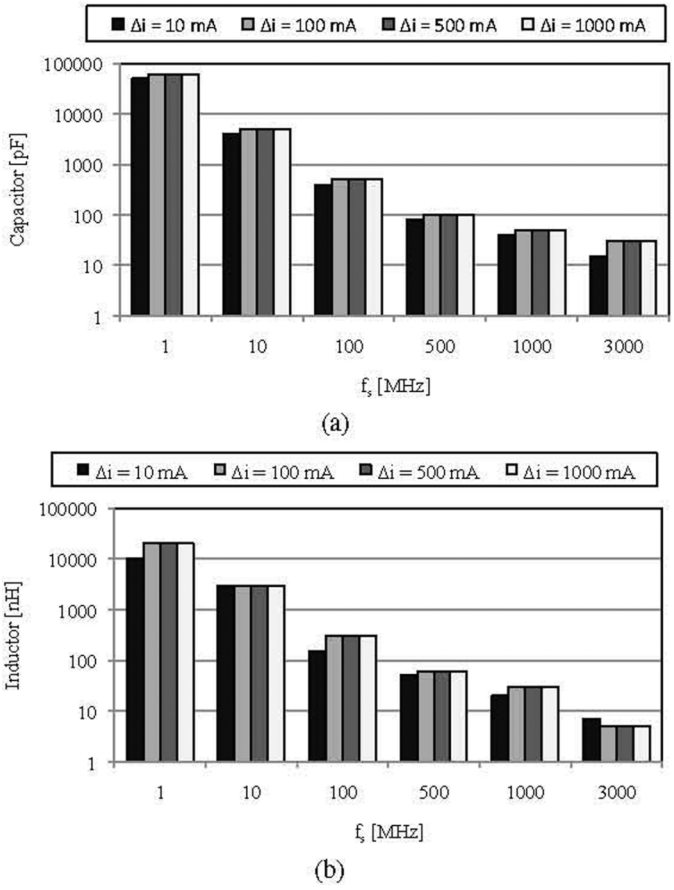

Fig. 12. Conventional *LC* filter: (a) capacitance and (b) inductance.

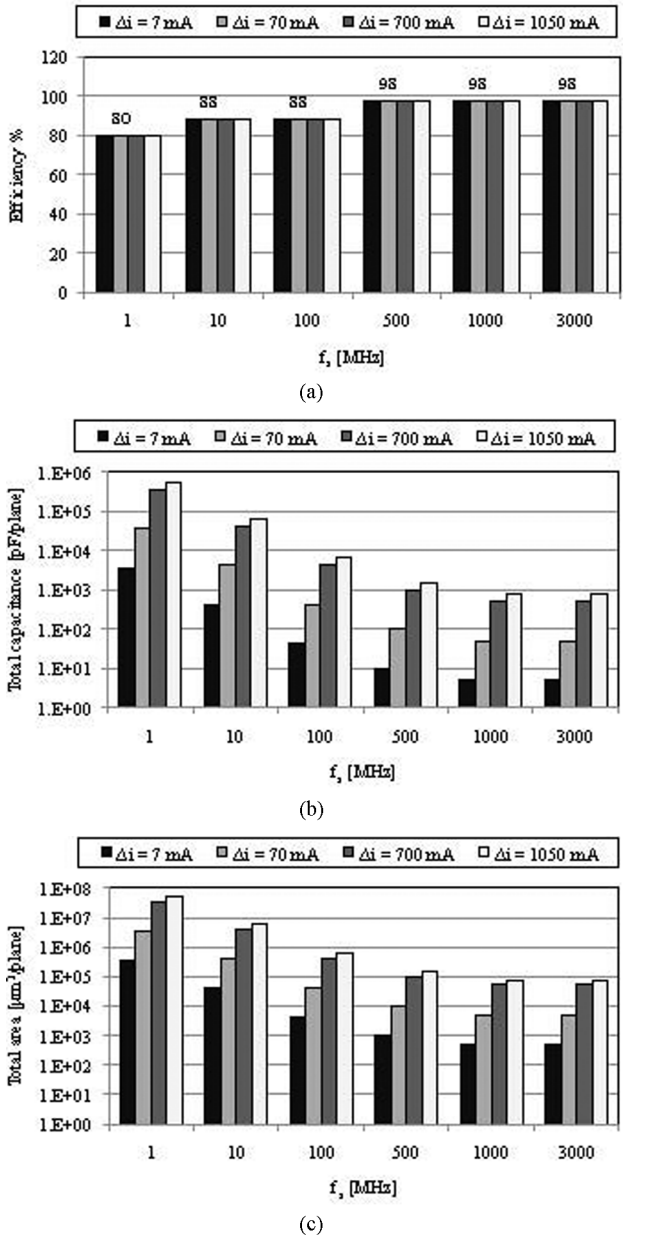

Fig. 13. 3-D distributed filter: (a) efficiency, (b) total capacitance per plane, and (c) total area per plane.

expected, the magnitude of the lumped inductor and capacitor decreases as the switching frequency increases. However, in the megahertz frequency region, the magnitude of the capacitor is between 100 pF and 100 nF, while the magnitude of the inductor is between 60 nH and 10 μH. In current technologies, these large inductors cannot be implemented on-chip. When the switching frequency is increased to gigahertz frequencies, the magnitude of the on-chip inductor becomes realizable on-chip. Note that in this case, the current load is assumed to only affect the output resistance of the power MOSFETs. Therefore, at higher current loads (above 100 mA), insignificant changes in the magnitude of the capacitance and inductance can be observed in Fig. 12.

The efficiency, total capacitance, and area per plane of the distributed filter as a function of switching frequency for different current loads are shown in Fig. 13. At a 1 MHz switching frequency, the efficiency of the filter reaches 80%. At higher frequencies, the efficiency is significantly greater, reaching 98% at 500 MHz, 1 GHz, and 3 GHz. Since only the filter efficiency is considered, excluding the power MOSFETs, the efficiency at the higher frequencies is dependent on the input impedance of the distributed filter which does not change significantly at higher frequencies. The input impedance remains approximately the same at higher frequencies since the capacitors C_1 to C_n of the distributed filter contribute less to the input impedance. As expected, the total capacitance and area occupied by the distributed filter decreases as the frequency increases. This behavior occurs since less capacitance and shorter interconnects are required at higher frequencies to satisfy the target voltage ripple.

As shown in Fig. 12(b), the magnitude of the required inductor within an *LC* filter varies between 50 and 10 000 nH for switching frequencies up to 1 GHz. The large range of inductance is attributed to the wide range of switching frequencies, i.e., 1 MHz to 1 GHz. At 3 GHz, the required inductor is less than 10 nH. This characteristic implies that at switching frequencies used in current technologies, i.e., up to several megahertz [26], a conventional *LC* filter cannot be implemented on-chip.

To evaluate the capability of providing a wide voltage conversion range, as required in 3-D circuits, the proposed methodology is compared to three on-chip converters [17], [27], [28], as shown in Fig. 14. The proposed converter in this example

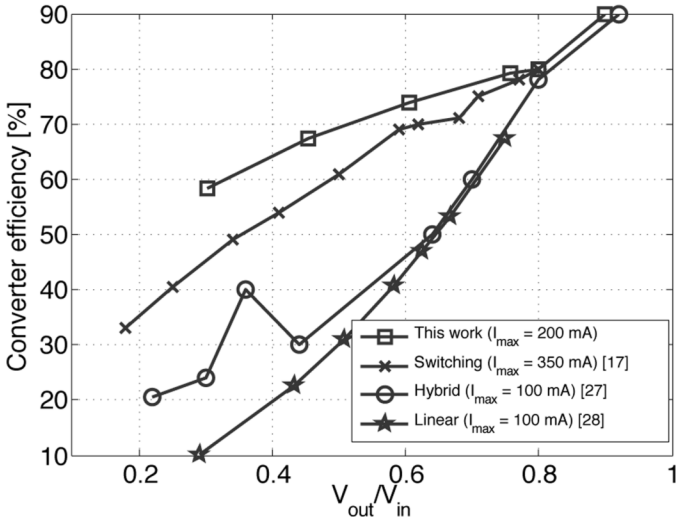

Fig. 14. Comparison of power efficiency.

distributes 200 mA maximum current. As evident from Fig. 14, the power efficiency of the proposed converter is greater than the other converters. A primary reason for the superior power efficiency is that the proposed converter eliminates the need for an on-chip inductor and any associated losses.

VI. Conclusion

Integrating dc-dc converters on-chip can significantly enhance the performance and reliability of integrated circuits. Conventional filters, however, are difficult to integrate due to the large magnitude of the on-chip inductors and capacitors. A distributed buck converter filter for application to three-dimensional circuits is proposed in this paper. By exploiting the low pass bandwidth properties of transmission lines, simultaneously generating and distributing power supplies to different planes is possible. An example converter based on the MITLL 3-D CMOS technology is described, demonstrating a dc-dc converter that can generate a 1.2 V power supply while delivering 700 mA.

A performance analysis considering the filter efficiency, total capacitance, and physical area is performed for a wide range of switching frequencies and current loads. A conventional on-chip *LC* filter in the megahertz frequency range is not practical due to the large inductors. Alternatively, an on-chip distributed filter can be implemented in the megahertz frequency range, achieving high efficiency, suitable for 3-D integration.

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