Linear and Switch-Mode Conversion in 3-D Circuits

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***Abstract*—A methodology for DC–DC conversion in three-dimensional (3-D) circuits is described in this paper. The proposed approach exploits both linear and switching buck converters with different conversion ranges, thereby increasing power efficiency. By replacing the traditional *LC* filter within a switching converter with a distributed filter, a significant increase in efficiency is demonstrated. Additionally, the physical structure of the filter simultaneously enables the distribution of high current to the load while filtering the switching signal at the input. Design guidelines and expressions are developed, achieving good agreement with simulations based on the MIT Lincoln Laboratories CMOS/SOI 180-nm 3-D technology. The proposed converter distributes 2.5 A maximum current, achieving conversion from 3.3 V to 2.5 V and 1 V with, respectively, 74% and 44% power efficiency.**

***Index Terms*—3-D integrated circuits, DC–DC buck converters, power efficiency.**

I. Introduction

TO COMPENSATE for the significant increase in power dissipation, multiple power supplies have been incorporated into large scale circuits. Multivoltage circuits exploit delay differences among the different signal paths by selectively lowering the supply voltage of these gates along the noncritical delay paths while maintaining a higher supply voltage on the critical delay paths to satisfy a target clock frequency [1], [2].

To reduce power dissipation and latency in high complexity circuits, an emerging three-dimensional (3-D) integrated circuit technology is under development [3]. In a 3-D technology, individual planes of 2-D integrated circuits are combined into 3-D cubes, increasing density and functionality. The distance between different circuit domains in a 2-D technology is significantly reduced once a plane is partitioned and stacked into a 3-D structure [3].

3-D integration offers novel architectural opportunities for microprocessors, as exemplified in Fig. 1. A multiplane structure enables the efficient partitioning of different portions of high performance, high complexity systems, such as memory, RF, and digital circuits. Additionally, heterogeneous technologies can be integrated onto different planes within the same system, thereby improving performance.

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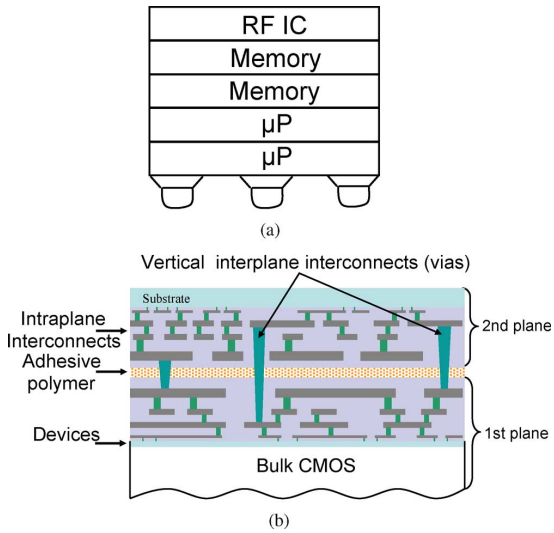

Fig. 1. 3-D circuit: (a) Multi-core processor combined from stacked planes. (b) Cross-section of a 3-D circuit.

Multiple on-chip power supplies in 2-D circuits are important due to the integration of low power, high speed digital circuits with analog/RF circuits on the same die. System heterogeneity offered by 3-D circuits has exacerbated the requirement for multiple, wide range, and well controlled power supplies. Each plane supports a variety of functions and applications, such as MEMs, RF, analog, memory, and high speed digital circuits. A system of distributed on-chip power supplies is therefore required. To support a multiple voltage domain system, efficient on-chip DC–DC converters are required.

The on-chip integration of DC–DC converters is highly efficient from an I/O perspective, particularly in 3-D circuits [4]. By integrating the entire buck converter on-chip, the number of I/O pins is reduced, decreasing the cost and physical size of the package. The large voltage swings produced by the parasitic impedances of the package are also eliminated [5]. Supply voltages produced locally on-chip can be dynamically controlled to compensate for on-chip temperature, process, and load variations. Furthermore, in a typical off-chip DC–DC converter, power is dissipated by the parasitic impedances of the interconnect among the nonintegrated devices. Multiple on-chip DC–DC converters can be distributed within the 3-D circuit to achieve target power requirements.

A methodology for designing on-chip DC–DC converters for application to 3-D circuits is described in this paper. The proposed scheme is a combination of linear and switching converters, forming a high efficiency conversion system. The methodology exploits the benefits of both types of DC–DC converters, depending upon the required power supply.

This paper is organized into five sections. A review of common types of buck converters as well as recent work

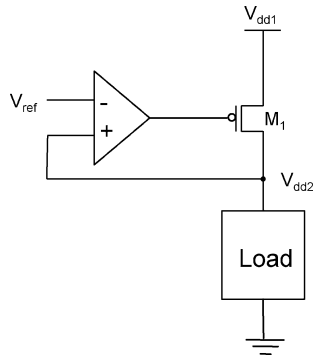

Fig. 2. Linear converter.

on on-chip converter circuits are described in Section II. In Section III, a methodology for designing a novel linear and switching converter for 3-D circuits is described, followed by the design of a linear converter and a switching converter in 3-D technology in Section IV and Section V, respectively. Two case studies are described in Section VI. In Section VII, a performance comparison between the proposed circuit and other on-chip DC–DC converters is presented. Finally, the paper is concluded in Section VIII.

II. Background

Converting AC or DC power supplies into lower or higher DC power supplies has been a topic of interest since the invention of modern electrical networks [6]. For integrated circuit applications, converting a high DC power supply into a lower DC power supply (called buck conversion) is of primary interest. Three common types of DC–DC converters are linear, switched-capacitor, and switching converters [7].

A. Linear Converters

A linear converter, also called a low dropout regulator (LDO), is effectively a controllable voltage divider, as shown in Fig. 2. The output voltage $V_{\rm dd2}$ is determined by $V_{\rm dd1}$ and the ratio of the impedance of the power MOSFET $\rm M_1$ and the load. An amplifier in a feedback loop senses the output DC voltage $V_{\rm dd2}$ and appropriately adjusts the gate voltage of transistor $\rm M_1$ to provide the required current to the load. Note that transistor $\rm M_1$ is typically very wide to conduct a large amount of current.

The design simplicity of a linear converter is attractive; however, at lower conversion ratios, the power efficiency exhibited by this type of converter is relatively low since the maximum power efficiency $\eta_{\rm linear,max}$ is determined by the ratio between the output and input DC voltages

$$\eta_{\rm linear,max} = \frac{V_{\rm out}}{V_{\rm in}} = \frac{V_{\rm dd2}}{V_{\rm dd1}}. \quad (1)$$

Due to the maximum power efficiency imposed by (1), the current efficiency is of interest in linear converters

$$\eta_{\rm linear} = \eta_{\rm linear,max} \cdot \eta_{\rm current} \quad (2)$$

where

$$\eta_{\rm current} = \frac{I_{\rm out}}{I_{\rm in}}. \quad (3)$$

For high conversion ratios, however, an LDO is an attractive approach. In [8], conversion from 1.2 V to 0.9 V with 94% current efficiency is demonstrated, resulting in 71% power efficiency while delivering 100 mA maximum current. In this circuit, the LDO achieves a small dropout voltage and fast load regulation due to a single-stage feedback loop, rapidly adjusting the PMOS power transistor (Fig. 2). Alternatively, an LDO with an impedance-attenuated buffer is described in [9]. Dynamically-biased shunt feedback is used, achieving stability of the LDO over a wide range of current loads. In this circuit, the input voltage ranges from 2 V to 5.5 volts, while the minimum output DC voltage is 1.8 V. With 99.8% current efficiency, the highest and lowest power efficiencies are 89% and 32%, respectively, delivering 200 mA maximum current.

B. Switched-Capacitor Converters

The operation of a switched-capacitor converter is based on periodically charging/discharging the charge pump capacitors through resistive switches. These switches contribute to the power losses of the converter. Additionally, a switched-capacitor converter exhibits poor output voltage regulation. To maintain a stable output voltage, high power feedback control circuitry is used which decreases the power efficiency. A switched-capacitor convertor can typically provide moderate levels of efficiency for small conversion ratios, while providing low current loads. The output resistance limits the peak power efficiency of a capacitive converter; the efficiency of a switched-capacitor converter therefore increases as the current load decreases [10]. A controllable DC–DC converter that combines a switched-capacitor voltage divider and a linear regulator is described in [11]. The circuit converts 2.5 V to as low as 0.65 V. A hybrid switched-capacitor and linear converter achieves higher power efficiency than a traditional linear converter. In this circuit, the switched capacitor converter generates a $V_{\rm dd}/2$ power supply with relatively high efficiency. Depending upon the required DC output voltage, a high voltage (with $V_{\rm dd}$ input power supply) or low voltage (with $V_{\rm dd}/2$ input power supply) linear converter is chosen using programmable control circuitry. The highest and lowest power efficiencies achieved by the proposed circuit when converting from 2.5 volts to 2.35 V and 0.6 V are 93% and 25%, respectively, delivering 100 mA maximum current.

C. Switching Converters

A switching converter is the most common converter due to the high efficiency of this type of converter. A standard topology of a buck converter is depicted in Fig. 3 [1], [12]. The working principle of this converter is based on an AC signal produced by the power MOSFETs. Depending upon the duty cycle and the input power supply, a specific DC component of the signal is passed to the output by a second order low pass *LC* filter. Due to the nonideality of the filter, residual high harmonics are also passed. The fundamental difficulty in integrating a switching converter on-chip is the significant area occupied by the *LC* filter.

III. Evaluation of Switching Converter Efficiency

The proposed design methodology is for generating and distributing numerous power supplies from a single input power

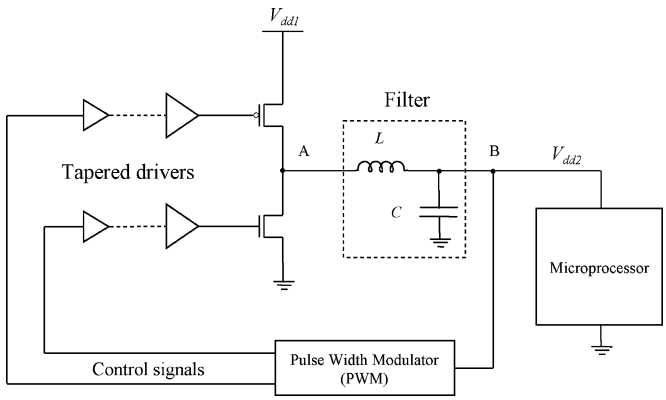

Fig. 3. Conventional switching DC–DC buck converter.

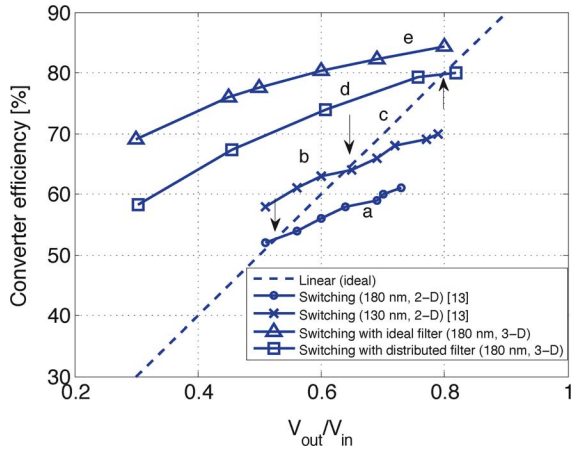

Fig. 4. Efficiency as a function of conversion ratio in different technologies.

supply within a 3-D cube. By utilizing a combination of linear and switching buck converters, high efficiency is achieved over a wide range of conversion ratios. A distributed filter within the switching buck converter is used to further improve power efficiency. In this section, the efficiency of several 2-D and 3-D converters is evaluated.

Since energy losses during power conversion is a significant concern, the primary focus of the proposed methodology is on increasing converter efficiency over a wide range of conversion ratios. Based on [13], the efficiency of a switching converter in a 180-nm (curve a) and 130-nm (curve b) 2-D technology as well as an ideal linear converter (curve c) and a switching converter with a distributed filter (curve d) based on the MIT Lincoln Laboratory 180-nm 3-D technology [14] is depicted in Fig. 4. The efficiency of the switching converter excluding any filter losses is also shown as a reference (curve e). In the 180-nm CMOS 2-D technology (curve a), the efficiency of an ideal linear converter (curve c) surpasses the efficiency of a conventional switching converter above a 0.5 conversion ratio. In the 130-nm technology (curve b), however, the efficiency of an ideal linear converter is higher than a conventional switching converter above a 0.65 conversion ratio. The low efficiency of a switching converter can be attributed to the dynamic power losses of the power MOSFETs (and the drivers) and the inductor losses within the *LC* filter. With advances in technology, however, switching converters tend to achieve higher efficiencies than a linear converter over a wider range of conversion ratios due to the decreased parasitic capacitance of the power MOSFETs and improvements in on-chip inductor technologies.

As a reference, consider the efficiency of an optimal switching converter excluding filter losses (curve e). As evident from curve e, the associated filter losses significantly reduce the converter power efficiency. The efficiency of a switching converter employing the distributed 3-D filter [15], [16] is also shown in Fig. 4 (curve d). The distributed filter increases the efficiency of a switching filter as compared to an ideal linear and a conventional switching converter in both a 180-nm and 130-nm technology. Note that at a 0.8 conversion ratio, the power efficiency of the linear converter surpasses the efficiency of the switching converter (curves c and d).

Switching 3-D converters exhibit higher efficiency as compared to other on-chip DC–DC converters due to the lower resistance of the distributed filter as compared to the on-chip inductor. On-chip inductors exhibit a high series resistance due to narrow metal lines, capacitive coupling with the substrate and other metal lines, and eddy currents [17]. An on-chip inductor typically exhibits a series parasitic resistance of 0.5 to 2Ω [18]. Additionally, the current flow through a spiral on-chip inductor is limited by the width of the metal lines comprising the inductor and the number of turns, which ultimately determine the inductance. Alternatively, by adding additional parallel interconnects, the distributed filter can provide a significantly larger amount of current to the load with a lower parasitic resistance. For example, the distributed 3-D converter efficiency presented in Fig. 5 is obtained with 40 parallel 0.5 mm long interconnects with a parasitic resistance of 14.5 $\text{m}\Omega/\mu\text{m}$. The total resistance (excluding the 3-D vias) of the distributed filter spanning three planes is therefore $3(14.5 \times 500)/40 = 0.54\,\Omega$. To further decrease this resistance, additional parallel interconnects can be added (with an additional area penalty). The distributed filter typically exhibits a lower resistance than the parasitic resistance of a spiral on-chip inductor.

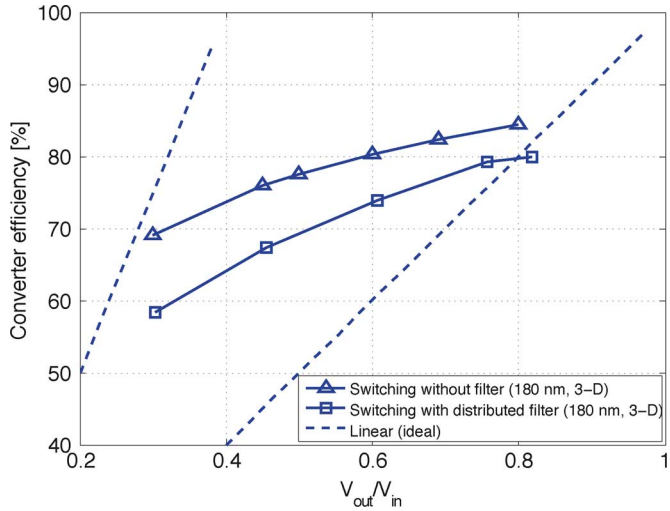

Fig. 5. Efficiency of linear and switching converters with dual-Vdd input voltage (the two dashed lines represent the two input voltages).

From the above discussion, the following conclusions can be drawn. A switching converter with a distributed filter is superior in power efficiency as compared to on-chip linear and

conventional switching converters. A detailed analysis of the power losses within the distributed 3-D switching converter is described in Section V-B. Due to the losses of a switching converter with a distributed filter operating at higher switching ratios (in this example, 0.8), a linear filter is more efficient for these conversion ratios. To obtain the highest efficiency over a wide range of conversion ratios, a methodology that uses a linear or a switching converter is proposed. As evident from Fig. 4, a switching converter with a distributed filter should be used up to a critical conversion ratio (in this example, the ratio is 0.8). Above this critical ratio, a linear filter provides the highest efficiency.

Alternatively, a dual-$V_{\rm dd}$ system can further improve efficiency. In this approach, two external power supplies $V_{\rm dd1H}$ and $V_{\rm dd1L}$ are provided where $V_{\rm dd1H}$ is higher than $V_{\rm dd1L}$. As observed in Fig. 4, the highest efficiency is obtained at higher conversion ratios. By separating the conversion range into three sections, overall performance is improved, as shown in Fig. 5. In this example, $V_{\rm dd1L}/V_{\rm dd1H}$ equals 0.4. The highest power efficiency depends upon the required conversion ratio. For conversion ratios between 0.2 to 0.4 and 0.8 to 1, a linear 3-D converter is preferable, while for conversion ratios between 0.4 to 0.8, a switching converter with a distributed filter provides the highest power efficiency. Over the entire conversion range (0.3 to 1), the power efficiency ranges from 65% to about 95% (at a 0.4 conversion ratio).

Based on the observations drawn from the aforementioned discussion, a novel linear converter is proposed in Section IV. In Section V, a switching converter with a distributed filter is described.

IV. A Linear Converter in 3-D Technology

A 3-D based linear converter is illustrated in Fig. 6. The current is distributed within the interconnect network. The RLC transmission lines are connected by 3-D vias, forming a network that spans from the first plane to a target plane. To adhere to electromigration and current density rules, several interconnect networks, illustrated in Fig. 6, are connected in parallel, providing the required current load. On the first plane, current mirror transistors ($\rm M_7$ and $\rm M_8$) conduct the primary portion of the current load. The current mirror produces a high output impedance at the input to the interconnect on the first plane. The same amount of current will flow within the interconnect network regardless of the voltage ripple. The remaining portion of the current flows through the PMOS transistor $\rm M_9$ which accommodates the input voltage, manufacturing process, and DC current load variations.

An amplifier connected in a negative feedback loop controls the gate voltage of transistor $\rm M_9$. By comparing the voltage at the output of the network to a reference voltage $(V_{\rm dd2})$, the amplifier adjusts the gate voltage of transistor $\rm M_9$ to maintain a stable output power supply. Note that the voltages used to bias this amplifier are also provided by the current mirror bias circuit. The decoupling capacitor at the output $C_{\rm dec}$ reduces the voltage ripple produced by the transient current load.

The size of transistors $\rm M_7, M_8$, and $\rm M_9$ within the 3-D linear converter depends upon the required DC current load as well as the transient behavior of the current load. Different switching events occur at different times for relatively long periods of

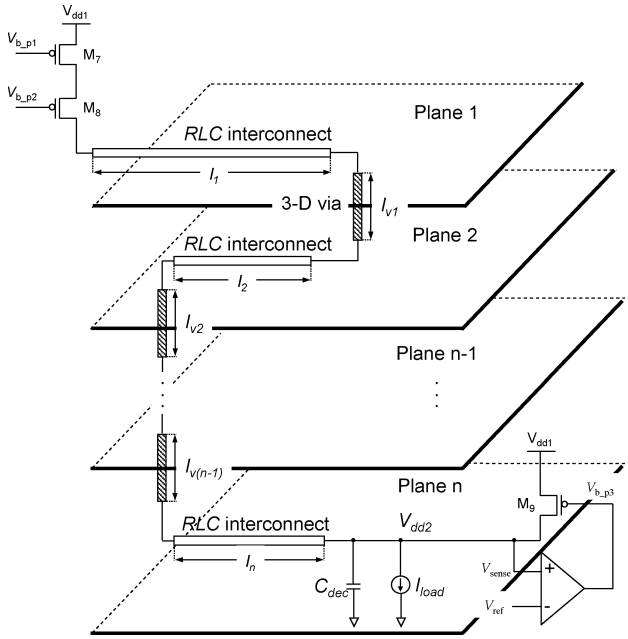

Fig. 6. Linear converter within a 3-D circuit.

times, producing DC current load fluctuations. To ensure proper function of the 3-D linear converter, transistor $\rm M_9$ is placed within a closed feedback loop, providing additional current to the load.

Assuming the maximum DC current load fluctuation is $\pm\Delta I_{\rm DC}$, transistor $\rm M_9$ is designed to provide $2\Delta I_{\rm DC}$ under nominal operation conditions (no current fluctuation). Hence, $\rm M_7$ and $\rm M_8$ provide the remaining portion of the DC current load, $I_{\rm DC} - 2\Delta I_{\rm DC}$. In this manner, by adjusting the gate voltage of $\rm M_9$ (Fig. 6), the load current is accordingly increased or decreased. For example, if an additional $+\Delta I_{\rm DC}$ current is required, increasing the gate voltage of $\rm M_9$ provides a current of $2\Delta I_{\rm DC} + \Delta I_{\rm DC}$ through $\rm M_9$. The total DC current flowing to the load is therefore $I_{\rm DC} - 2\Delta I_{\rm DC} + 3\Delta I_{\rm DC} = I_{\rm DC} + \Delta I_{\rm DC}$. Alternatively, if a smaller current is required by an amount $-\Delta I_{\rm DC}$, decreasing the gate voltage of M9 provides a current of $2\Delta I_{\rm DC} - \Delta I_{\rm DC}$ through $\rm M_9$. The total DC current flowing to the load in this scenario is therefore $I_{\rm DC} - 2\Delta I_{\rm DC} + \Delta I_{\rm DC} = I_{\rm DC} - \Delta I_{\rm DC}$.

As described in Section II-A, the maximum power efficiency of a linear converter is determined by the ratio of the output voltage to the input voltage. Current efficiency is therefore a useful metric for linear converters. In this linear converter circuit (Fig. 6), three currents have a direct DC path to ground which reduce the current efficiency. The total lost current is

$$I_{\rm linear,lost} = 2I_{\rm bias} + m \cdot I_{\rm bias} = (2+m)I_{\rm bias} \qquad (4)$$

where m is the ratio of the width of transistor $\rm M_{16}(M_{17})$ and $\rm M_5(M_6)$. Thus, assuming $m = 1$, the power efficiency of a linear converter is

$$\eta_{\rm linear,3-D} = \left(\frac{V_{\rm dd2}}{V_{\rm dd1}}\right) \cdot \left(\frac{I_{\rm DC}}{I_{\rm DC} + 3I_{\rm bias}}\right) \qquad (5)$$

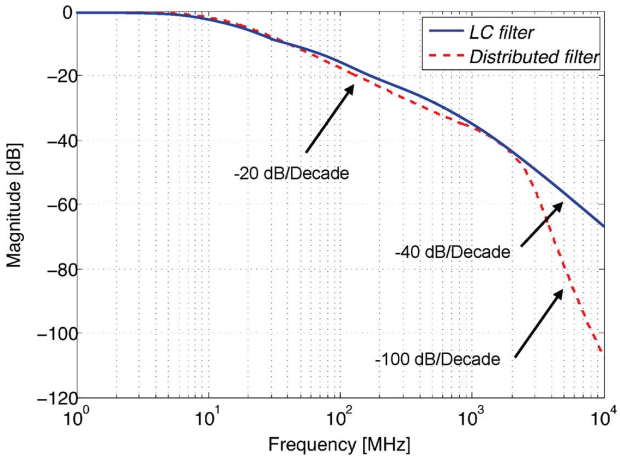

Fig. 7. Magnitude of transfer function of an *LC* filter and a distributed filter.

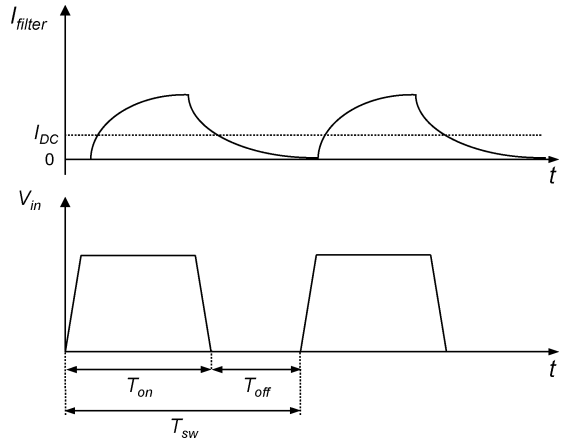

Fig. 8. Typical transient current waveform of the distributed filter.

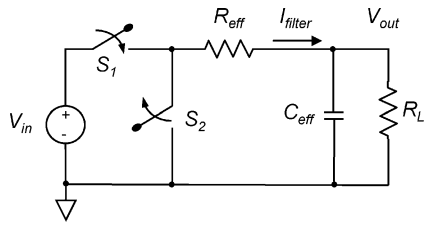

Fig. 9. Lumped model of the distributed switching DC–DC converter.

where $I_{\rm DC}$ is the DC current load

$$I_{\rm DC} = I_0 + \frac{\Delta i}{2T_{\rm CLK}}(t_{rc} + t_{fc}). \tag{6}$$

In (6), $T_{\rm CLK}$ is the time period of the current load, which corresponds to the clock signal frequency.

V. A Switching Converter in 3-D Technology

In this section, a switching converter with a distributed filter is described. In Section V-A, the operating principle and methodology for designing a distributed filter are presented. An analysis of the power efficiency of the combined 3-D switching converter with a distributed filter is described in Section V-B.

A. Distributed Filter

In this subsection, a novel distributed filter within a switching converter for 3-D circuits is introduced. In Section V-A1, the principle behind the operation of a distributed filter is presented. The physical structure and typical current load characteristics are described in Section V-A2, while in Section V-A3 the transfer function of the distributed filter is developed.

1) Principle of a Distributed Filter: The proposed filter exploits the impedance characteristics of long transmission lines. This type of interconnect behaves as a low pass filter which can be utilized within a buck converter. In this manner, the high frequency harmonics of the AC signal are filtered, producing a DC signal at the output. The distributed low pass filter spans multiple planes of a 3-D circuit, providing the required power supply to a specific circuit domain.

To obtain insight into the operation of a distributed filter as compared to a lumped *LC* filter, consider the transfer function of two types of filters, as depicted in Fig. 7. A second order low pass *LC* filter is used in a typical conventional DC–DC converter. When the effective output resistance R_d of the power MOSFETs and the effective series resistance of the inductor are included, two poles at different frequencies are formed, resulting in a roll-off slope of -20 dB/decade in the megahertz and -40 dB/decade in the gigahertz frequency range. The frequency behavior of a distributed filter in the megahertz frequency range is therefore similar to a lumped *LC* filter, as can be observed in Fig. 7. When R_d and the interconnect resistance are included in the analysis, a pole in the megahertz frequency is formed, resulting in a roll-off slope of -20 dB/decade. Note that in this example, a sharp -100 dB/decade roll-off slope is formed in the gigahertz frequency range, suppressing the high frequency harmonics of the AC signal produced by the power MOSFETs. The distributed nature of the proposed filter forms multiple poles at approximately the same high frequency, resulting in a large negative slope.

As compared to a lumped *LC* filter, the transient current flowing within a distributed filter exhibits exponential waveform characteristics, as depicted in Fig. 8. To demonstrate this behavior, consider a simplified model of the distributed switched DC–DC converter, as shown in Fig. 9. The switches $\rm S_1$ and $\rm S_2$ represent the power MOSFETs. The resistance $R_{\rm eff}$ and capacitance $C_{\rm eff}$ are, respectively, the effective resistance and capacitance of the distributed filter, while R_L is the load.

Since the input voltage is a periodic waveform (with a period $T_{\rm sw}$), the output voltage of the network shown in Fig. 9 is described by an infinite series

$$V_{\rm out}(t) = \sum_{k=-\infty}^{\infty} \frac{a_k \cdot e^{j2\pi k f_{\rm sw} t}}{1 + \frac{R_{\rm eff}}{R_L}(1 + j2\pi k f_{\rm sw} R_L C_{\rm eff})} \tag{7}$$

where

$$a_k = \begin{cases} \dfrac{V_{\rm dd1} T_{\rm on}}{T_{\rm sw}}, & k = 0 \quad (8) \\ \dfrac{V_{\rm dd1}}{\pi k} \sin(\pi k f_{\rm sw} T_{\rm on}), & k \neq 0 \quad (9) \end{cases}$$

and $f_{\rm sw} = 1/T_{\rm sw}$.

During the time interval $nT_{\rm sw} \leq t < (n + D)T_{\rm sw}$ (n is an integer number and D is the duty cycle), corresponding to the

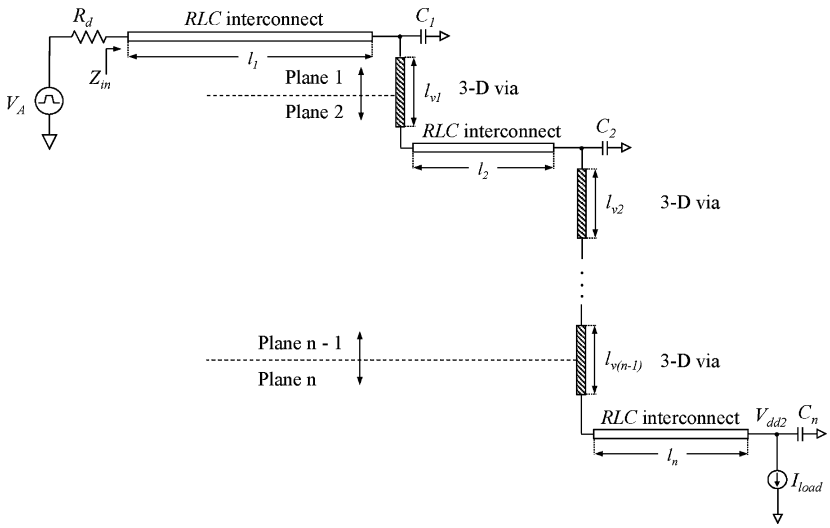

Fig. 10. Distributed filter.

state when S_1 is closed and S_2 is open, the current flowing within the distributed filter is

$$I_{\text{filter}}^{T_{\text{on}}}(t) = \frac{V_{\text{dd1}} - V_{\text{out}}(t)}{R_{\text{eff}}} \tag{10}$$

where $V_{\text{out}}(t)$ is described in (7). Consequently, during the complementary time interval $(n+D)T_{\text{sw}} \leq t < (n+1)T_{\text{sw}}$, corresponding to the state when S_1 is open and S_2 is closed, the current flowing within the distributed filter is

$$I_{\text{filter}}^{T_{\text{off}}}(t) = \frac{V_{\text{out}}(t)}{R_{\text{eff}}}. \tag{11}$$

The DC component of I_{filter} (Fig. 8) is

$$I_{\text{DC}} = \frac{V_{\text{dd2}}}{R_L}. \tag{12}$$

As expected from an ideal RC circuit and supported by (10) and (11), the output capacitance C_{eff} charges during T_{on} and discharges during T_{off}.

2) Physical Structure and Current Load Properties of a 3-D Filter: The proposed distributed filter is depicted in Fig. 10. The filter is driven by power MOSFETs (Fig. 3) which are modeled as a voltage source V_A followed by an effective resistance R_d. The voltage source V_A is assumed to be periodic, as described in Section I-C.

The filter is composed of transmission lines terminated with lumped capacitances. The inter-plane structure is connected by 3-D vias. At the target plane n, the load is represented by a periodic current load and a reference clock signal. Note that the current load characterizes the approximate current profile of a specific circuit module on a plane. I_{load} remains at I_0 during clock low, providing DC current flow by the power supply. As with a conventional buck converter, a feedback PWM circuit senses the output node of the filter and adjusts the duty cycle of the signal driving the power MOSFETs (Fig. 3).

In 3-D circuits, the ability to deliver current is primarily limited by the 3-D vias. The maximum current that can be delivered through a single 3-D via therefore determines the current magnitude

$$I_0 + \Delta i = J_{\text{via,max}} \cdot A_{\text{via}} \cdot N_{\text{via}} \tag{13}$$

where $J_{\text{via,max}}$, A_{via}, and N_{via} are the maximum current density, cross-sectional area, and number of 3-D vias on the same plane, respectively. Consequently, the maximum cross-sectional area of the interconnects (Fig. 10) distributing current within the different planes is

$$A_{\text{int}} = \frac{I_0 + \Delta i}{J_{\text{int,max}}} = \left(\frac{J_{\text{via,max}}}{J_{\text{int,max}}}\right) \cdot A_{\text{via}} \cdot N_{\text{via}} \tag{14}$$

where $J_{\text{int,max}}$ is the maximum current density of the interconnect.

In practical circuits, however, a significant amount of current is sunk by the load. To satisfy this requirement, multiple structures N, as depicted in Fig. 10, are connected in parallel, delivering $N(I_0 + \Delta i)$ amperes. In this case, the number of 3-D vias within the filter on each plane is equal to the number of parallel connected structures $N_{\text{via}} = N$. The effective resistance and inductance per unit length of the interconnects and 3-D vias, as well as the output resistance of the driver (Fig. 10), are N times smaller. The capacitance per unit length of the interconnects and 3-D vias, as well as the on-chip lumped capacitors, are N times larger.

3) Transfer Function of a 3-D Filter: To characterize the impedance of the filter (between R_d and I_{load}), the overall transfer function is based on the $ABCD$ matrices. Hence, the overall $ABCD$ matrix of a filter spanning n planes is

$$\begin{bmatrix} \tilde{A} & \tilde{B} \\ \tilde{C} & \tilde{D} \end{bmatrix} = \begin{bmatrix} 1 & R_d \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} A' & B' \\ C' & D' \end{bmatrix}. \tag{15}$$

The right matrix in the right-hand side of (15) is

$$\begin{bmatrix} A' & B' \\ C' & D' \end{bmatrix} = \prod_{i=1}^{n} \left(\begin{bmatrix} \cosh \gamma l_i & Z_0 \sinh \gamma l_i \\ \sinh \gamma l_i / Z_0 & \cosh \gamma l_i \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_i & 1 \end{bmatrix} \cdot \begin{bmatrix} \cosh \gamma_v l_{vi} & Z_{v0} \sinh \gamma_v l_{vi} \\ \sinh \gamma_v l_{vi} / Z_{v0} & \cosh \gamma_v l_{vi} \end{bmatrix} \right) \tag{16}$$

where Z_0 and γ are the characteristic impedance and propagation constant of the RLC interconnects, respectively, l_i and C_i are the interconnect length and capacitance on the ith plane, respectively, Z_{v0} and γ_v are the characteristic impedance and

propagation constant of the 3-D vias, respectively, and l_{vi} is the length of the 3-D via on the ith plane. The transfer function of the filter is

$$H_{\text{filt}}(j\omega) = \frac{1}{\tilde{A}} \tag{17}$$

where $\tilde{A}$ is obtained from (15).

Since a practical filter within a buck converter does not provide ideal low pass characteristics, the signal at node B, shown in Fig. 3, carries a small amount of high frequency harmonics generated by the switching power MOSFETs. Hence, the voltage at node B is

$$V_{\text{dd2}}(t) = V_{\text{DC}} + V_{\text{ripple}}(t) \tag{18}$$

where V_{DC} is the DC component of the output voltage and $V_{\text{ripple}}(t)$ is the voltage ripple transferred by the nonideal characteristics of the filter. When only the fundamental harmonic is passed, $V_{\text{ripple}}(t)$ exhibits a sinusoidal behavior

$$V_{\text{ripple}}(t) = V_r \sin(\omega_s t). \tag{19}$$

To satisfy a target ripple voltage V_r (peak-to-peak), the filter transfer function at the switching frequency f_s has to achieve a specific magnitude. To satisfy this objective, consider the output signal in the frequency domain

$$|V_{\text{dd2}}(s)| = |H_{\text{filt}}(s)| \cdot |V_A(s)|. \tag{20}$$

The periodic input signal V_A can be represented by a Fourier series

$$v_A(t) = \sum_{k=-\infty}^{\infty} a_k e^{jk\omega_s t} \tag{21}$$

where a_k is the kth harmonic of the signal. In the case of the signal illustrated in Fig. 12 and assuming $t_{rp} = t_{fp} = t_r$, the fundamental harmonic (positive and negative) is

$$a_{\pm 1} = \left(\frac{V_{\text{dd1}} T_s}{4 t_r \pi^2}\right) \cdot (e^{\mp j\omega_s t_r}(1 - e^{\mp j2\pi D}) + e^{\mp j2\pi D} - 1). \tag{22}$$

Equation (20) implies that the required amplitude of the transfer function for a specific ripple voltage V_r is

$$|H_{\text{filt}}(j\omega_s)| \leq \frac{V_r/2}{2|a_1|} = \frac{V_r}{4|a_1|}. \tag{23}$$

Once the current profile of a circuit is determined, the interconnect length l_1 to l_n, shown in Fig. 10, and the required ripple voltage V_r are chosen. Based on (17), the magnitude of the transfer function at ω_s is plotted as a function of the capacitances C_1 to C_n. The interconnect length and capacitances are chosen to satisfy (23).

An important issue is the duty cycle of the signal driving the power MOSFETs (Fig. 10) that produces the correct power supply voltage. Note that in this case, the duty cycle determined by $V_{\text{dd2}}/V_{\text{dd1}}$ does not provide the proper DC voltage level. This behavior occurs since the signal at the input of a distributed filter is degraded by the resistance R_d and the input impedance of the filter Z_{in}, forming a voltage divider. To produce the duty cycle required for a specific DC voltage, consider the input impedance of the filter at DC

$$Z_{\text{in}}(0) = \frac{V_{\text{DC}} A'(0) + I_{\text{DC}} B'(0)}{V_{\text{DC}} C'(0) + I_{\text{DC}} D'(0)} \tag{24}$$

where A', B', C', and D' are defined in (16), and I_{DC} is the DC component of the current load (6). The DC component of the signal at the input of the filter (including R_d in Fig. 10) is

$$\text{DV}_{\text{dd1}} = D_{\text{PWM}} V_{\text{dd1}} \left| \frac{Z_{\text{in}}(0)}{Z_{\text{in}}(0) + R_d} \right| \tag{25}$$

the DC voltage transferred by the filter to the target plane. In (25), D_{PWM} is the duty cycle provided by the PWM feedback circuit (Fig. 3). Consequently, to achieve a specific DC voltage at the output of the filter, the duty cycle is

$$D_{\text{PWM}} = D \cdot \left| 1 + \frac{R_d}{Z_{\text{in}}(0)} \right|. \tag{26}$$

Observe from (26) that D_{PWM} is always larger than $D = V_{\text{dd2}}/V_{\text{dd1}}$, limiting the magnitude of the generated power supply. When the interconnects within the distributed filter are resistive, D_{PWM} approaches D (no reflections occur at the input). It is typically preferable to design the filter to ensure that D_{PWM} is closer to D to provide a large tuning range for the PWM circuit.

B. Power Losses of Switching Converter With Distributed Filter

A switching converter with a distributed filter is illustrated in Fig. 11. The distributed filter passes the DC and residual higher order harmonic components of the signal at the output of the power MOSFETs (PM_1 and PM_2). The AC signal produced by PM_1 and PM_2 is shown in Fig. 12. The filter is comprised of an interconnect network that spans multiple planes. Capacitors C_1 to C_n are connected to each interconnect while the 3-D vias connect the interconnects throughout the planes, forming a distributed filter structure.

The input power dissipated by the distributed filter (Fig. 11) is

$$P_{\text{filt}} = V_{A,\text{rms}}^2 \left| \frac{Z_{\text{in}}(\omega_s)}{Z_{\text{in}}(\omega_s) + R_{\text{MOS,eff}}} \right|^2 \Re\left\{ \frac{1}{Z_{\text{in}}(\omega_s)} \right\} \tag{27}$$

where $V_{A,\text{rms}}$ is the rms voltage of the input signal, $R_{\text{MOS,eff}}$ is the effective output resistance of the power MOSFETs PM_1 and PM_2, and Z_{in} is the input impedance of the filter network at ω_s (24). The output power at the load of the filter is

$$P_{\text{out,filt}} = V_{\text{dd2}} I_{\text{DC}}. \tag{28}$$

The power MOSFETs are driven by buffers controlled by a pulse width modulation (PWM) circuit. The PWM circuit senses the output voltage V_{dd2} and generates the required duty cycle to maintain a stable output voltage. The design of the power MOSFETs and drivers for maximum power efficiency is adopted from [1].

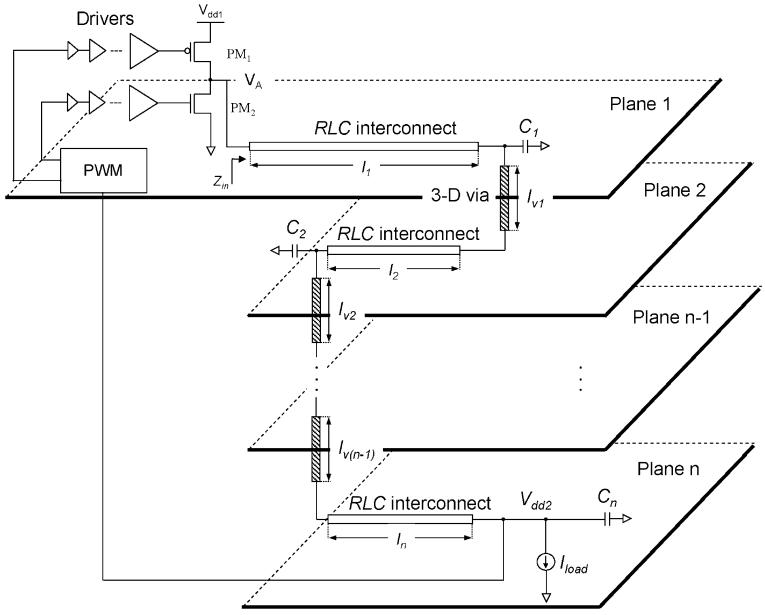

Fig. 11. A switching converter with the 3-D distributed filter.

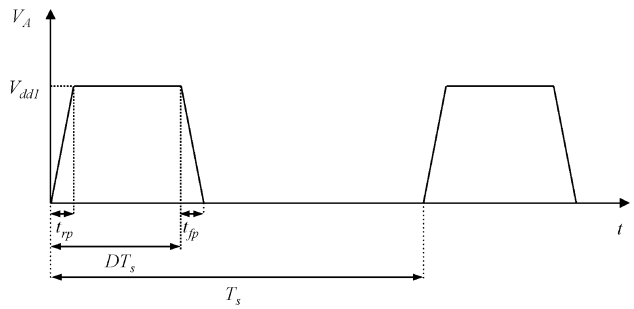

Fig. 12. Voltage signal at the input of the filter.

The average power consumed by the power MOSFETs (PMOS or NMOS) and driving buffers is composed of resistive and dynamic power losses, respectively

$$P_{\mathrm{PMOS/NMOS,res}} = \frac{R_0}{W} I_{\mathrm{rms}}^2 \tag{29}$$

$$P_{\mathrm{PMOS/NMOS,dyn}} = EWf_s \tag{30}$$

$$P_{\mathrm{PMOS/NMOS}} = \frac{R_0}{W} I_{\mathrm{rms}}^2 + EWf_s \tag{31}$$

where R_0 is the effective resistance of a 1 μm wide transistor (PMOS or NMOS), W is the width of the power MOSFET, I_{rms} is the root-mean-square current passing through the power MOSFET, f_s is the switching frequency, α is the tapering factor of the buffers, and $C_{\mathrm{ox}}, C_{\mathrm{gs}}, C_{\mathrm{gd}}$, and C_{db} are the gate oxide, gate-to-source, gate-to-drain, and drain-to-body capacitances, respectively, of a 1 μm wide transistor. E is the unit energy per 1 μm wide power MOSFET consumed during one switching cycle

$$E_{\mathrm{PMOS/NMOS}} \cong \frac{\alpha}{\alpha - 1} \left(C_{\mathrm{ox}} + C_{\mathrm{gs}} + 2C_{\mathrm{gd}} + C_{\mathrm{db}} \right) V_{\mathrm{dd1}}^2. \tag{32}$$

The total power consumption of both power MOSFETs is

$$P_{\mathrm{total,MOS}} = P_{\mathrm{PMOS}} + P_{\mathrm{NMOS}}. \tag{33}$$

As evident from (31), increasing the width of the power MOSFET reduces the resistive losses and increases the dynamic power losses. An optimum MOSFET width, therefore, exists that minimizes the total power of the drivers and the power MOSFET

$$W_{\mathrm{PMOS/NMOS,opt}} = \sqrt{\frac{R_0 I_{\mathrm{rms}}^2}{f_s E}} \; [\mu\mathrm{m}] \tag{34}$$

where

$$I_{\mathrm{rms,PMOS}} = \sqrt{(1 - D_{\mathrm{PWM}}) \left(I_{\mathrm{DC}}^2 + \frac{\Delta i^2}{3} \right)} \tag{35}$$

$$I_{\mathrm{rms,NMOS}} = \sqrt{D_{\mathrm{PWM}} \left(I_{\mathrm{DC}}^2 + \frac{\Delta i^2}{3} \right)} \tag{36}$$

assuming the ratio between the time when both transistors are off to the switching period T_s as compared to the duty cycle D_{PWM} is small. The effective output resistance of the optimal PMOS and NMOS transistors is

$$R_{\mathrm{PMOS/NMOS,opt}} = \frac{R_0}{W_{\mathrm{opt}}} \tag{37}$$

and the total effective resistance of the power MOSFETs is

$$R_{\mathrm{MOS,opt}} = \frac{R_{\mathrm{PMOS,opt}} + R_{\mathrm{NMOS,opt}}}{2}. \tag{38}$$

The overall efficiency of the 3-D switching converter is therefore

$$\eta_{\mathrm{switching,3-D}} = \frac{I_{\mathrm{DC}} \cdot V_{\mathrm{dd2}}}{I_{\mathrm{DC}} \cdot V_{\mathrm{dd2}} + P_{\mathrm{total,MOS}} + P_{\mathrm{filt}}}. \tag{39}$$

TABLE I
WIDTH OF THE TRANSISTORS WITHIN THE 3-D LINEAR CONVERTER

Transistor	Width [μm]
M_7, M_8	40,000
M_9	8,800

The optimal design of the drivers and power MOSFETs does not consider the power consumed by the distributed filter. As mentioned earlier and evident from (29) and (31), increasing the width of the power MOSFETs decreases the resistive power component while increasing the dynamic power. When both components are equal, minimum power is dissipated. Concurrently, decreasing the width of the power MOSFETs increases the effective output resistance of the power MOSFETs, reducing the power dissipated by the distributed filter, as evident in (27). Minimizing the power dissipation of the entire network, therefore, may result in differently sized power MOSFET than the optimal width (minimum dynamic and resistive loss) specified by (34).

VI. CASE STUDY

Based on the approach described in Section III and illustrated in Fig. 4, two case studies are presented in this section. Conversion from 3.3 V to 2.5 V and to 1.0 volt, based on the MIT Lincoln Laboratories (MITLL) 180-nm CMOS 3-D technology [14], is demonstrated, assuming current distribution from the first plane to the third plane. In both cases, the target voltage ripple at the output is $\pm 2.5\%$. Additionally, the current load profile has the following characteristics: $1/T_{\rm CLK} = 3$ GHz, t_{rc} and t_{cf} are $0.3T_{\rm CLK}/2$ and $0.7T_{\rm CLK}/2$, respectively, and I_0 and Δi are 0.5 and 2 A, respectively, resulting in 1 A DC current. An approach is employed to support a wide range of conversion ratios (in this example, 3.3 V to 1.0 volt).

The maximum current density in the MITLL 3-D technology is

$$J_{3-{\rm D},\max} = 3\ {\rm mA}/\mu{\rm m}^2. \tag{40}$$

To adhere to electromigration rules in this technology, the width of a single interconnect is chosen to be 2.5 μm, supporting a DC current of 5 mA. To conduct a maximum 2.5 A current $(I_0+\Delta i)$, 500 distributed filters are connected in parallel. In Section VI-A, a linear 3-D converter is used to convert from 3.3 V to 2.5 V (high conversion ratio). In Section VI-B, a switching converter with a distributed filter is used to convert from 3.3 V to 1.0 V (low conversion ratio).

A. 3.3 V to 2.5 V Conversion

The length of the interconnects on each plane is chosen to be 0.1 mm long. The source transistors (Fig. 6) have been designed with the transistor widths listed in Table I. The transistor channel lengths are 360 nm. Both resistors, R_1 and R_2, and the current bias $I_{\rm bias}$ are 5 kΩ and 100 μA, respectively. Note that transistors M_7 and M_8 conduct the majority of the current (800 mA) while transistor M_9 conducts the rest of the DC current (200 mA). The area occupied by all of the transistors is 17 689 μm^2, while the area of 500 minimum-spaced (0.35μm) parallel interconnects is 142 500 μm^2 per plane. To support an output voltage ripple of $\pm 2.5\%$, a 300 pF decoupling capacitor $C_{\rm dec}$ is chosen, achieving 104 mV ripple ($\pm 2.1\%$ of a 2.5 output voltage). The power efficiency of this linear converter is 74.2%, achieving 98.3% current efficiency. The simulated output voltage is shown in Fig. 13.

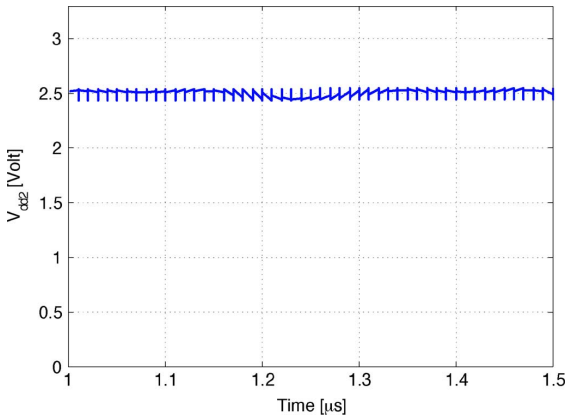

Fig. 13. Output voltage of the linear 3-D converter.

To examine the response of a linear 3-D converter to abrupt changes in the current load, consider Fig. 14. The response of the linear converter to an increase of 200 mA current load with a 20-A/μs slew rate is shown in Fig. 14(a). The output signal exhibits a voltage undershoot of 386 mV, settling to 2.5 V after 156 ns. The response of the linear converter to a decrease of 100 mA in the current load with a 20-A/μs slew rate is shown in Fig. 14(b). In this case, the output voltage exhibits an overshoot of 187 mV over a period of 523 ns. Note that the settling time when the current load is decreased by 100 mA is fairly long due to the relatively low gain of the amplifier.

B. 3.3 V to 1.0 V Conversion

To achieve maximum power efficiency for a conversion ratio of 0.3, the use of a switching converter with a distributed filter is required (Fig. 4). The same current load specifications as for the linear converter are assumed in this example. The methodology described in Section V-A is used to design the distributed filter.

Designing a switching converter with a distributed filter requires an iterative approach, since the effective output resistance of the power MOSFETs affects the magnitude of the duty cycle $D_{\rm PWM}$ which determines the output voltage. Concurrently, the duty cycle $D_{\rm PWM}$ affects the design of the drivers and power MOSFETs. The iterative approach converges within a few iterations.

To ensure the voltage ripple of the output power supply is 50 mV ($\pm 2.5\%$ of 1 V), the magnitude of the transfer function of the distributed filter, described by (23), switching at 100 MHz has to be equal to or less than 0.0149. To design the distributed filter, the resistance, inductance, and capacitance per unit length of the interconnects (Metal 3) and 3-D vias are extracted based on the predictive technology model (PTM) [19]–[21], as listed in Table II. The width of the interconnects is determined by the maximum current density of the MITLL 3-D technology. Assuming that both the interconnect and 3-D vias support the same current density of 3 mA/μm^2, the maximum cross-sectional area

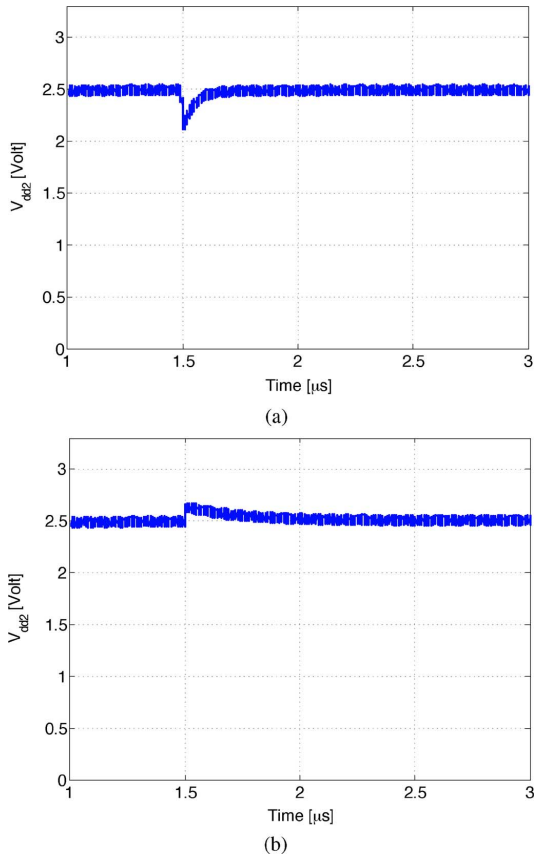

Fig. 14. Transient output voltage response: (a) 200 mA increase in current load and (b) 100 mA decrease in current load.

TABLE II
RLC INTERCONNECT AND 3-D VIA IMPEDANCES

	R [mΩ/μm]	L [pH/μm]	C [fF/μm]
Interconnects	14.5	1.3	0.5
3-D via [20]	20.40	0.55	0.37

of the interconnect is $1.5 \times 1.5\ \mu\text{m}^2$. The thickness of the interconnect for this technology is 630 nm, resulting in an approximately 2.5 μm wide line. Note that each 3-D via is 7.34 μm long, connecting three planes, as illustrated in Fig. 10.

The magnitude of the transfer function at ω_s for different capacitances and interconnect lengths, assuming $l = l_1 = l_2 = l_3$ and $C = C_1 = C_2 = C_3$, is depicted in Fig. 15. As the interconnect length increases, less capacitance is required, as evident in Fig. 15. To satisfy the required voltage ripple (50 mV), the interconnect length in this example is $l = 0.5$ mm with a capacitance $C = 67$ nF per plane. In this example, the required duty cycle of the signal driving the power MOSFETs is 0.46, as specified by (26).

The width of the power MOSFETs and the distributed filter structure are determined for maximum power efficiency. The MOSFET, filter, and total power dissipation as a function of the ratio between the effective output resistance of the power MOSFETs and the optimal power MOSFETs is shown in Fig. 16. To minimize the power dissipation, the effective output resistance of the power MOSFETs is four times $R_{\text{MOS,opt}}$, resulting in

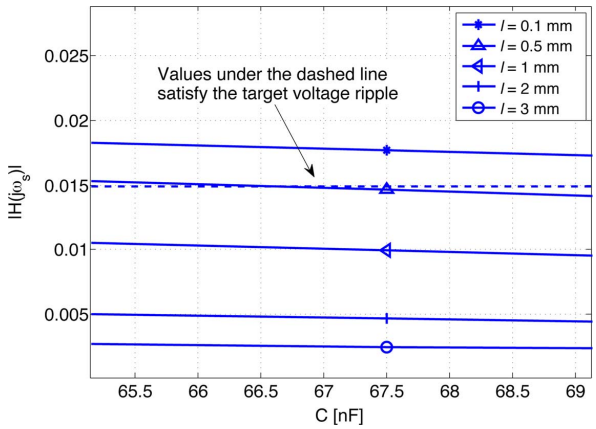

Fig. 15. Magnitude of the transfer function at ω_s for different line lengths and capacitances.

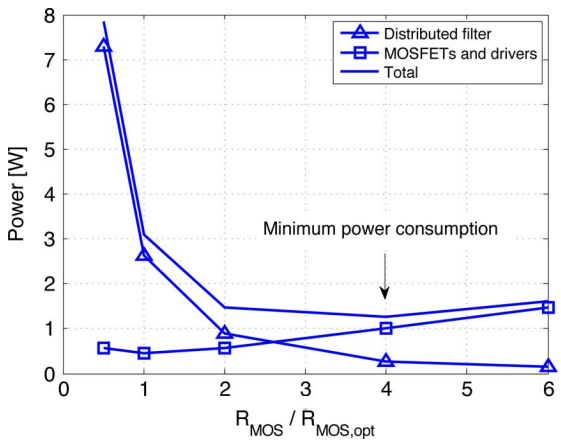

Fig. 16. Power components of the 3-D switching converter, distributing 2.5 A of peak current.

a width of 5.3 mm for the PMOS and 3.7 mm for the NMOS transistor.

Since this circuit is designed to provide 2.5 A maximum current, 500 filter circuits on each plane with 0.5 mm long interconnects are connected in parallel (assuming a single interconnect conducts 5 mA maximum current). Assuming a 10 fF/μm^2 capacitance density in the MITLL 3-D technology [14], the area of the switching converter is about 2.6×2.6 mm^2 (mostly occupied by on-chip capacitors) and the efficiency is 44%. Although this converter exhibits relatively low power efficiency, note the on-chip conversion from 3.3 V to 1.0 V while distributing 2.5 A maximum current. This capability is reported for the first time. As compared to other converters, the proposed 3-D converter exhibits superior performance, as described in Section VII. The output voltage produced by this converter, exhibiting 49.5 mV voltage ripple, is shown in Fig. 17.

The transient response of the switching 3-D converter to abrupt changes in the current load is shown in Fig. 18. In this example, the response of the switching converter response is shown for an increase of 200 mA current load with a 20-A/μs slew rate. The output signal exhibits a voltage overshoot of 100 mV, settling to 1.0 V after 1.04 μs. Note the smooth response of the switching converter as compared to the linear converter shown in Fig. 14.

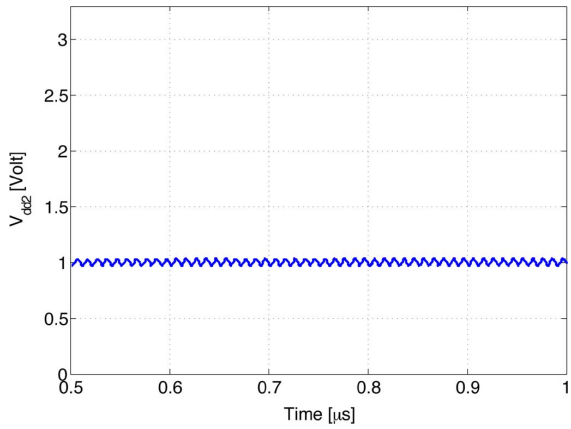

Fig. 17. Output voltage of the switching converter.

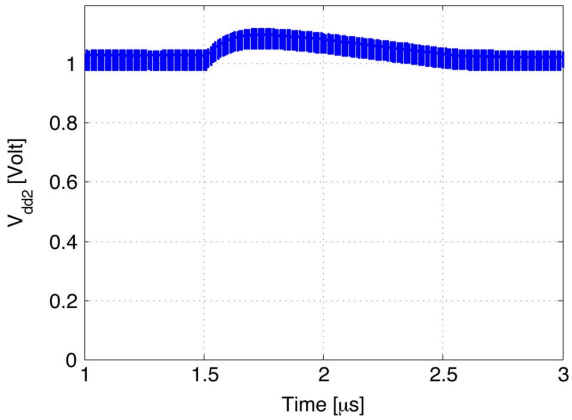

Fig. 18. Transient output voltage response of the distributed converter for an increase of 200 mA current load with a 20-A/μs slew rate.

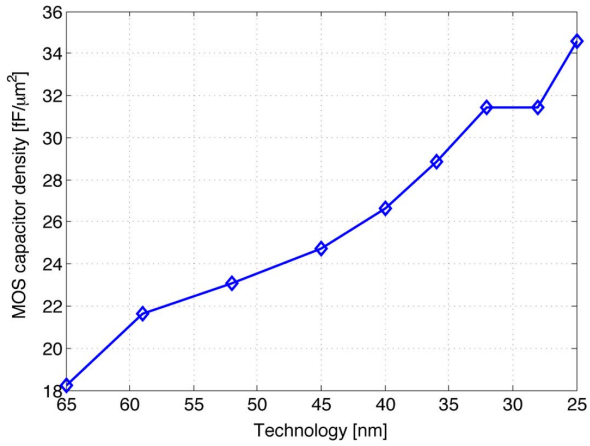

Fig. 19. MOS capacitor density for different technologies.

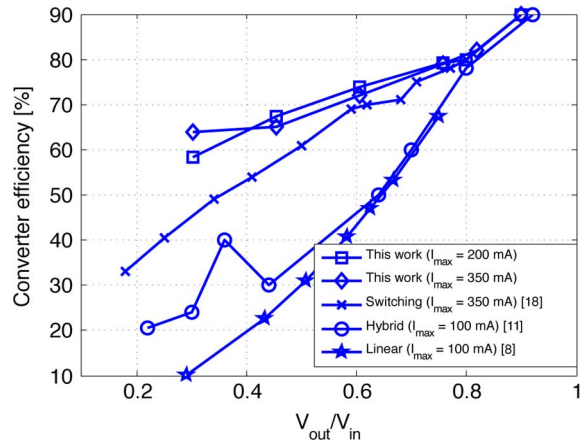

Fig. 20. Power efficiency of different approaches as a function of $V_{\rm out}/V_{\rm in}$.

VII. Performance Comparison and Discussion

The switching converter occupies a relatively large area due to the significant amount of capacitance to provide a stable power supply while delivering several amperes of current. The area occupied by the on-chip capacitors, however, is predicted to decrease with advanced technologies. The MOS capacitor density can be estimated as $\epsilon_{\rm ox}/t_{\rm ox}$, where $\epsilon_{\rm ox}$ and $t_{\rm ox}$ are the dielectric constant and MOS oxide thickness, respectively [23]. MOS capacitor densities as a function of technology are shown in Fig. 19. Note the expected doubling in density over the next several technology nodes. Furthermore, the feasibility of fabricating extremely large on-chip capacitances has been demonstrated [24], where a 250-nF on-chip MIM capacitor in 90-nm technology has been implemented. Alternatively, by exploiting the Miller effect, small area active circuit based capacitors can also be used, albeit requiring additional power [5].

The multiple plane structure in 3-D circuits suggests that area is less of a concern. Thus, several planes can be dedicated to accommodate the required capacitors. Note that a conventional *LC* filter not only requires integration of an inductor but also a significant amount of capacitance. For example, an on-chip 5-nH inductor requires a 35-nF capacitor to achieve 5% output voltage ripple at 100 MHz with 0.46-Ω output resistance of the power MOSFETs (which corresponds to conducting 2.5 A maximum current).

To evaluate the ability of providing a wide voltage conversion range, as required in 3-D circuits, the proposed converter is compared to three on-chip converters, as shown in Fig. 20. The proposed converter in this example distributes 200 mA maximum current. As evident from Fig. 20, the power efficiency of the proposed circuit is greater than the other converters. A primary reason for the improved power efficiency is that the proposed circuit eliminates the need for an on-chip inductor with associated losses. Additionally, the circuit is composed of a linear or switching converter with the distributed filter (depending on the required conversion ratio) further increasing the efficiency. The 3-D converter performance results are based solely on dynamic circuit simulation. To provide a fair comparison, note that the results described in [8], [11], and [18] are based on experimental measurements.

A performance comparison between the 3-D converters and six different approaches for on-chip DC–DC conversion is listed in Tables III and IV. In Table III, the performance characteristics of state-of-the-art linear, switched-capacitor, and switching converters in 2-D and 3-D technologies are compared. The performance of the 3-D converter with a 3.3 V input power supply, 100 MHz switching frequency, and 5% voltage ripple based on the MITLL CMOS/SOI 180-nm technology is listed in Table IV.

As can be observed from this comparison, the proposed circuit achieves superior performance. This buck converter efficiently distributes current in the ampere range as compared to

TABLE III
PERFORMANCE COMPARISON OF DIFFERENT PUBLISHED ON-CHIP DC–DC CONVERTERS

	Switching converter [18]	3-D switching [4]	Stacked switching [22]	Linear converter [8]	Linear converter [9]	Hybrid converter [11]
Technology [nm]	130, 2-D	180, 3-D	350, 3-D	90, 2-D	350, 2-D	250, 2-D
V_{out}/V_{in} [V/V]	0.9 / 1.2	0.9 / 1.8	2.3 / 3.3	0.9 / 1.2	3.15 / 5.5	1.62 / 2.5
Conversion ratio	0.75	0.50	0.70	0.75	0.57	0.65
I_{max} [mA]	350	500	70	100	200	100
Power efficiency [%]	77.9	64.0	62.0	70.7	57.1	61
Voltage ripple [%]	4.4	4.5	10	10	2	19
Switching frequency [MHz]	170	200	200	—	—	—
Area [mm^2]	1.5	6.9	4	0.098	0.264	0.42
χ [mA/mm^2]	242	92	15	952	757	223

TABLE IV
PERFORMANCE SUMMARY OF THE PROPOSED 3-D CONVERTER (THIS WORK)

	$I_{max} = 200$ [mA]					$I_{max} = 2500$ [mA]	
V_{out} [volt]	1.0	1.5	2.0	2.5	2.7	1.0 (switching)	2.5 (linear)
Conversion ratio	0.30	0.45	0.60	0.75	0.82	0.3	0.75
Power efficiency [%]	58	67	74	79	80	44	74
Area [mm^2]	1.7	1.34	1.0	0.55	0.35	6.65	0.14
χ [mA/mm^2]	227	222	246	383	557	551	17720

other approaches that only provide sub-ampere current loads while maintaining reasonable power efficiency.

To evaluate the relative performance of the individual DC–DC converters, a constant χ has been introduced

$$\chi = \frac{(w_{\text{power}}\eta_{\text{conv}})(w_{\text{current}}I_{\text{max}})}{C_r(w_{\text{area}}A_{\text{conv}})} \tag{41}$$

where η_{conv} and I_{max} are the converter power efficiency and maximum current load, respectively, and C_r and A_{conv} are the conversion ratio ($V_{\text{out}}/V_{\text{in}}$) and converter area, respectively. The weights $w_{\text{power}}, w_{\text{current}}$, and w_{area} represent the relative significance of the power efficiency, current load, and area of the DC–DC converter, respectively. In this manner, the most critical performance criteria, power efficiency, current load, conversion ratio, and converter area, are captured in one constant. From (41), this constant is proportional to the performance since high values of χ translate into high performance.

As observed in Tables III and IV (bottom row), for $w_{\text{power}} = w_{\text{current}} = w_{\text{area}} = 1$, the proposed 3-D distributed filter exhibits comparable or higher performance as compared to other circuits described in the literature. Note that as compared to switching converters, the 3-D converter (when used as a switching converter) exhibits superior performance. Similarly, as compared to linear converters [8] and [9], the 3-D converter (when used as a linear converter) exhibits significantly higher performance.

The proposed converter enables a wide voltage conversion range, achieving the highest power efficiency as compared to other approaches. Note that these results are obtained based on dynamic circuit simulation. The area required by the proposed circuit is comparable to other approaches. These properties and the distributed nature of the converter make the proposed converter highly suitable for 3-D integration, where multiple voltage domains are required. An evaluation of the 3-D DC–DC converter to current load variations and control loop compensation is described in the remainder of this section.

a) Current Load: A primary advantage of the proposed converter as compared to a conventional DC–DC converter is the ability to deliver a large amount of current to the load. This property is due to the parallel nature of the distributed filter structure. Thus, the current load scales linearly with the number of parallel connections. The current load and density of a specific 3-D technology constrains the number of parallel interconnects. Consequently, the on-chip capacitance increases in proportion to the number of parallel connections. Hence, the limiting performance factor is the area occupied by the on-chip capacitors. For a conventional DC–DC converter with an *LC* filter, the limiting performance component is the on-chip inductor. Issues related to the design of the on-chip inductor prevent conducting large amounts of current to the load.

To explore the power efficiency of the 3-D switching converter for different current loads, consider the efficiency expression (39). The terms that determine the power efficiency in (33) are $P_{\text{total,MOS}}$ and P_{filt}. Note that the term $P_{\text{total,MOS}}$ (33) is proportional to I_{rms}. The term P_{filt} (27) is inversely proportional to the effective output resistance of the power MOSFETs $R_{\text{MOS,eff}}$ and the input impedance $Z_{\text{in}}(j\omega)$ of the distributed filter. Both $R_{\text{MOS,eff}}$ and $Z_{\text{in}}(j\omega)$ are inversely proportional to I_{rms}. The overall efficiency of the 3-D switching converter therefore increases when the load current decreases. For example, in the case study of the 3-D switching converter, the efficiency is a function of the maximum current load for different conversion ratios, as depicted in Fig. 21. The general trend observed in Fig. 21 is that the power efficiency increases at low

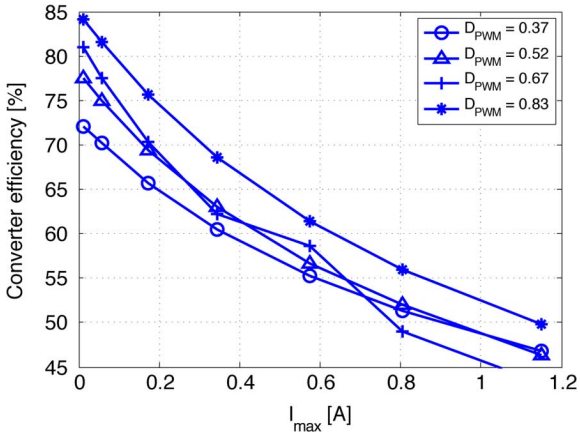

Fig. 21. Power efficiency as a function of maximum load current.

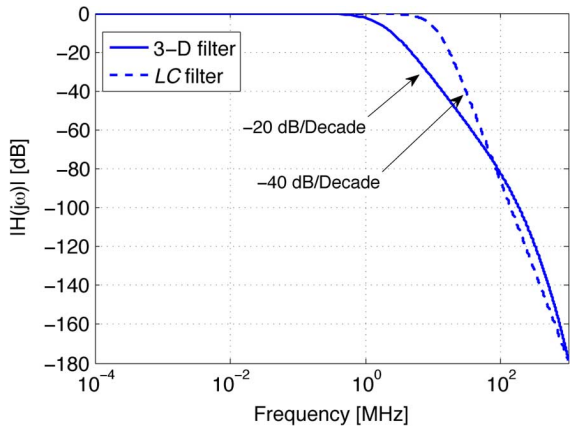

Fig. 22. Magnitude of the transfer function of a 3-D and ideal *LC* filter.

current loads for all conversion ratios. The primary reason for this trend is that the power dissipated by the distributed filter decreases at low current loads due to the increase in the effective output resistance of the power MOSFETs $R_{\mathrm{MOS,eff}}$ (due to the use of narrower width power MOSFETs).

b) Control Loop Compensation: As with every feedback loop, the stability of the system is of significant importance. Therefore, in a conventional buck converter, Type 2 or Type 3 compensation schemes are used to stabilize the control feedback loop in the voltage-mode converter [7]. Since the filter in the 3-D switching converter exhibits a distributed nature, additional poles and zeros exist. These poles and zeros, however, are significantly higher in frequency than the unity gain frequency (the crossover frequency) of the open loop transfer function and therefore do not affect the design of traditional compensation networks (Type 2 or Type 3). The nondominant poles and zeros within the 3-D filter are higher in frequency than the unity gain frequency due to the small total resistance of the parallel interconnects.

To justify this assumption, consider the transfer function of the distributed filter. It is intractable to extract a closed-form expression for the poles and zeros of the transfer function of the distributed filter. A graphical representation of the transfer function is therefore used from which the poles and zeros can be estimated, as described in the following example. In this example, the transfer function of the distributed filter used to convert from 3.3 V to 1.0 V (see Section VI-B) and an ideal *LC* filter is shown in Fig. 22. Note that the *LC* components are chosen to support the same conversion requirements as in the 3-D case. As expected, the transfer function of the *LC* filter exhibits a roll-off slope of -40 dB/decade while the distributed 3-D filter exhibits a roll-off slope of -20 dB/decade in the frequency range of interest (up to 100 MHz). The distributed 3-D filter therefore contributes one fewer pole to the open loop transfer function than a conventional *LC* filter, resulting in a simpler Type 2 compensation network. Summarizing, compensating the distributed filter is similar to compensating a conventional *LC* filter with a significant effective parasitic resistance (ESR) of the output capacitance C [7].

VIII. Conclusion

An approach using both a linear and switching DC–DC converter achieves the highest power efficiency as compared to other published methods. By incorporating the concept of an inductorless distributed filter in 3-D circuits, the efficiency is further increased. The proposed circuit provides a wide voltage conversion range, suitable for integration into 3-D heterogeneous systems, distributing 2.5 A maximum current to the load. With this current load, 0.75 and 0.3 conversion ratios with a simulated 74% and 44% power efficiency are, respectively, demonstrated.

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