Active Filter-Based Hybrid On-Chip DC–DC Converter for Point-of-Load Voltage Regulation

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***Abstract*— An active filter-based on-chip DC–DC voltage converter for application to distributed on-chip power supplies in multivoltage systems is described in this paper. No inductor or output capacitor is required in the proposed converter. The area of the voltage converter is therefore significantly less than that of a conventional low-dropout (LDO) regulator. Hence, the proposed circuit is appropriate for point-of-load voltage regulation for noise sensitive portions of an integrated circuit. The performance of the circuit has been verified with Cadence Spectre simulations and fabricated with a commercial 110 nm complimentary metal oxide semiconductor (CMOS) technology. The area of the voltage regulator is 0.015 mm^2 and delivers up to 80 mA of output current. The transient response with no output capacitor ranges from 72 to 192 ns. The parameter sensitivity of the active filter is also described. The advantages and disadvantages of the active filter-based, conventional switching, linear, and switched capacitor voltage converters are compared. The proposed circuit is an alternative to classical LDO voltage regulators, providing a means for distributing multiple local power supplies across an integrated circuit while maintaining high current efficiency and fast response time within a small area.**

***Index Terms*— Hybrid regulator, low-dropout regulator, on-chip voltage regulation, point-of-load voltage regulation.**

I. Introduction

THE POWER supply voltage aggressively scales with each technology generation, making the delivery of a high quality supply voltage to noise sensitive circuit blocks highly challenging [1]–[4]. The number of voltage domains within an integrated circuit is increasing to satisfy stringent power budgets. The increase in the number of voltage domains requires new techniques to generate these voltages close to the load circuitry while occupying a small area. The power savings is greater when the voltage regulators are close to the load devices (point-of-load voltage delivery), and size is therefore the primary issue for point-of-load voltage regulation. Classical power supplies occupy large on-chip area and are therefore not appropriate for point-of-load power delivery. Several topologies are commonly used to generate on-chip dc voltages. These DC–DC voltage converters are generally used as on-chip power supplies in high performance integrated circuits. Conventional DC–DC converters can be grouped into three primary categories: switching, switched capacitor (SC), and linear DC–DC converters [2].

Buck converters, which are step-down switching DC–DC converters, are popular because of their high power efficiency. A second order inductor–capacitor (LC) passive filter is commonly used in a buck converter. The passive LC components require significant on-chip area, therefore, the passive components have generally been implemented off-chip [2], [5]. As a consequence of placing these components off-chip, significant voltage drop and bounce are produced at the package level due to the parasitic resistance and inductance between the off-chip components of the voltage converter and the integrated circuit. Additionally, the parasitic interconnect impedance between the discrete components of the voltage converter can produce significant power loss. Furthermore, with power supply scaling, analog and digital circuits are less tolerant to fluctuations in the supply voltage [2], [5]. The parasitic impedance of the interconnect between the discrete components degrades the speed and accuracy of the load regulation, causing slow response times and changing output voltage levels.

As previously mentioned, the primary issue in the design of a conventional on-chip voltage converter is the physical area. The on-chip passive LC filter within a monolithic buck converter occupies a large area. Kursun *et al.* report 12.6 mm^2 die area for an on-chip buck converter using an 80 nm CMOS technology with a switching frequency of 477 MHz [5]. A 4 mm^2 on-chip LC filter is required in another buck converter which provides 70 mA current with a switching frequency of 200 MHz [6]. An on-chip passive LC filter is therefore infeasible due to the large area when multiple on-chip voltage converters are needed (such as in a multivoltage microprocessor).

A more area efficient voltage converter structure is a low-dropout voltage regulator (LDO) [7]–[14]. These regulators are implemented on-chip close to the load circuitry for fast and accurate load regulation. These regulators require a large output capacitance to achieve fast load regulation. This capacitor

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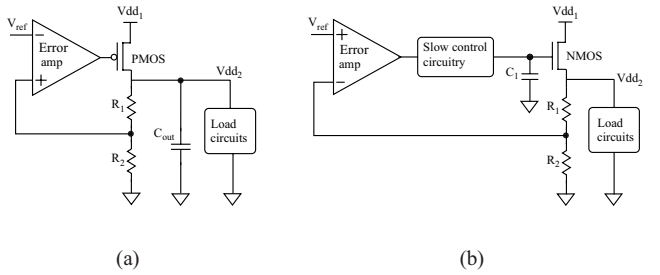


Fig. 1. LDO voltage regulators (a) with a PMOS output stage where R_1 and R_2 are adjusted to generate a different dc voltage at the output and (b) with an NMOS source follower output stage where C_1 is connected to the gate of the NMOS transistor to reduce coupling from the output to the gate terminal.

occupies significant on-chip area and is therefore generally implemented off-chip [7], [8]. The off-chip implementation of the output capacitor requires dedicated I/Os and produces higher parasitic losses. Alternatively, when the output capacitor is placed on-chip, the output capacitor dominates the total LDO regulator area [9]. A high bias current of 6 mA is used in [9] to deliver 100 mA current with a 600 pF output capacitor. This approach is not appropriate for low power applications and the output capacitor occupies a significant die area. Many techniques have been proposed to eliminate the need for the large off-chip capacitor without sacrificing the stability and performance of an LDO regulator [9]–[14]. Adaptively changing the bias current based on the output current demand is proposed in [10], [15], and [12]. These techniques, however, do not completely eliminate the need for an output capacitor. Furthermore, compensation circuitry that produces a dominant pole requires additional area. Due to the large area requirement, LDO regulators are not appropriate for a system of distributed point-of-load voltage regulators.

An ultra-small area efficient voltage converter is required for the next generation of multivoltage systems because these systems are highly sensitive to local power/ground (P/G) noise. The parasitic impedance of the power distribution network is a crucial issue when the voltage converter is far from the load circuitry. Voltage converters need to be placed close to the load circuitry since the $L\ dI/dt$ noise and IR voltage drops have become significant in deeply scaled circuits with aggressively scaled supply voltages [2], [5].

To produce a voltage regulator appropriate for distributed point-of-load voltage generation, the passive LC filter within a buck converter is replaced with a more area efficient active filter circuit [16]–[19]. A switching input voltage is used to generate the desired output voltage, and the converter uses a filter structure to produce the desired output voltage. The current supplied to the output node, however, does not originate from the input switching signal, rather, it originates from the operational amplifier (Op Amp) output stage, similar to a linear voltage converter. The proposed voltage converter is therefore a hybrid combination of a switching and linear DC–DC converter. The on-chip area of the proposed hybrid regulator is 0.015 mm^2, which is significantly smaller than state-of-the-art output capacitorless LDOs. The power efficiency, however, is limited to $V_{\text{out}}/V_{\text{in}}$, similar to an LDO.

The rest of this paper is organized as follows. A brief overview of a conventional buck converter is provided in Section II. In Section III, a low pass active filter-based converter is reviewed for different active filter topologies and types such as Butterworth, Chebyshev, and Bessel. Several tradeoffs among a number of active filter topologies are discussed. The design requirements of the Op Amp and related tradeoffs are also discussed in this section. The advantages and disadvantages of the proposed voltage regulator as compared to conventional switching and LDO regulators are discussed in Section IV. Experimental results are provided in Section V. A case study in which the proposed regulator provides power to a clock distribution network is described in Section VI. A distributed system of point-of-load voltage regulators is described in Section VII. This paper is concluded with Section VIII.

II. Conventional Low Voltage Power Supplies

A linear voltage regulator utilizes a tunable resistive circuit, applying resistive voltage division to generate an output dc voltage from a higher dc voltage. The on-chip area of a linear regulator can be quite small, but the power efficiency is intrinsically low due to the resistive voltage divider. The resistive components are tuned for input voltage and output current variations to provide a stable output voltage. An LDO regulator is the most common type of linear regulator due to the LDO voltage which improves power efficiency. LDO regulators with PMOS and NMOS output stages are depicted, respectively, in Fig. 1(a) and (b). The primary advantage of linear regulators is the lower complexity and faster load regulation as compared to SC and switching voltage converters [7], [14].

SC DC–DC converters utilize nonoverlapping switches to control the charge on the capacitors that transfer energy from the input to the output. When the switching frequency is sufficiently high, the output voltage is a multiple of the input voltage. The primary disadvantage of these converters is that the resistive switches dissipate high power. Additionally, the sensitivity of SC converters to changes in the output current is high and the feedback circuitry to maintain a stable dc output voltage is complex [2].

Switching DC–DC converters are the most commonly used type of power supplies due to the high power efficiency characteristics [2]. A switching DC–DC converter generating an output voltage greater than the input supply voltage is called a *boost converter*. Alternatively, the converter is a *buck converter* if the output voltage is less than the input voltage. A typical buck converter is shown in Fig. 2(a). The passive inductor and capacitor are generally implemented off-chip due to the significant on-chip area required by these elements. The PMOS and NMOS drive transistors generate a switching signal at Node$_1$, shown in Fig. 2(a). The low pass LC filter removes the high frequency harmonics of the switching signal, and generates

$$V\text{dd}_2(t) = V\text{dd}_2 + V_r(t) \tag{1}$$

where $V\text{dd}_2$ is the output dc voltage and V_r is the output voltage ripple due to the nonideality of the low pass filter. $V\text{dd}_2$ is the average value of the switching voltage at Node$_1$, which is

$$V\text{dd}_2 = V\text{dd}_1\left(D - \frac{t_r - t_f}{2T}\right) \tag{2}$$

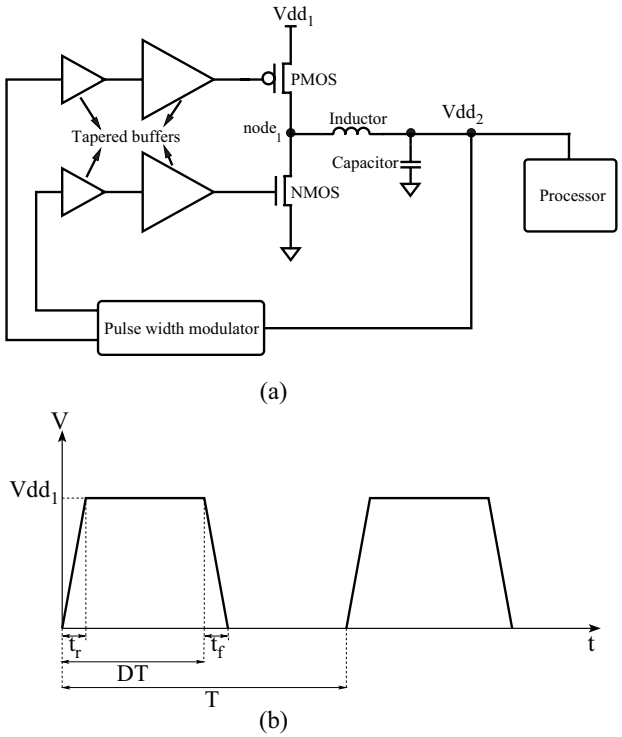


Fig. 2. Conventional buck converter. (a) Buck converter where the inductor and capacitor are typically implemented off-chip due to the large area. (b) Signal waveform at the output of the power MOSFETs (node_1) where D, t_r, t_f, and T are, respectively, the duty cycle, rise time, fall time, and period of the switching voltage.

where D, t_r, t_f, and T are, respectively, the duty cycle, rise time, fall time, and period of the switching voltage as illustrated in Fig. 2(b). When the rise and fall times of the switching signal are the same, the output voltage is

$$V\text{dd}_2 = DV\text{dd}_1. \tag{3}$$

The amplitude of the ripple voltage depends on both the filter characteristics and the variation of the output current demand. The amplitude of the ripple voltage becomes larger for a finite time when the output current demand changes abruptly. Additionally, the pulse width modulator (PWM), shown in Fig. 2, can be programmed to generate a different duty cycle to vary the output dc voltage.

III. Active Filter-Based Switching DC–DC Converter Design

In the proposed circuit, the bulky LC filter in a conventional buck converter is replaced with an active filter structure and the tapered buffers are replaced with smaller buffers, as shown in Fig. 3. The switching input signal generated at Node_1 is filtered by the active filter structure, similar to a buck converter, and a dc voltage is generated at the output. Increasing the duty cycle D of the input switching signal at Node_1 increases the generated dc voltage as in (2).

Large tapered buffers are required in a conventional buck converter to drive the large power transistors, PMOS and NMOS, as shown in Fig. 2. The current delivered to the load circuitry is provided by these large power transistors. In the proposed circuit, however, the current delivered to the load circuitry is supplied by an Op Amp. Small buffers are therefore sufficient for driving the active filter. Replacing the tapered buffers with smaller buffers significantly decreases the power dissipated by the input stage. Alternatively, the output buffers within the Op Amp dissipate power within the regulator. Another characteristic of the regulator is that the feedback required for line and load regulation is satisfied with separate feedback paths, as shown in Fig. 3. Feedback_1 is generated by the active filter structure and provides load regulation, whereas feedback_2 is optional and controls the duty cycle of the switching signal for line regulation. In most cases, feedback_1 is sufficient to guarantee fast and accurate load regulation. When only one feedback path is used, the switching signal is generated by simpler circuitry (e.g., a ring oscillator) and the duty cycle of the switching signal is compensated by a local feedback circuit (a duty cycle adjustor). The primary advantage of a single feedback path is the smaller area since feedback_1 is produced by the active filter and no additional circuitry is required for the compensation structure.

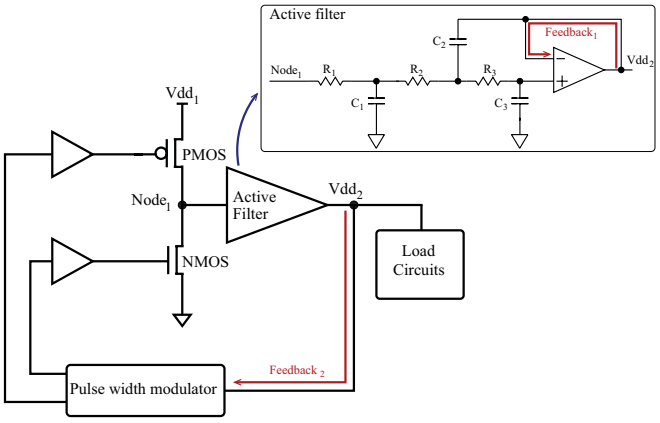


Fig. 3. Proposed DC–DC converter. Note that the passive LC filter is replaced with an active filter and the large tapered buffers are no longer necessary.

Utilizing active filters within a switching voltage regulator to replace the passive LC filter was first proposed in [16], however, several important design issues such as power efficiency, the sensitivity of the active filter, the importance of the output buffer stage of the Op Amp, and the type and topology of the active filter structure were overlooked. Additionally, the active filter-based regulator in [16] requires a 10 μF capacitor, which occupies significant on-chip area and is therefore inappropriate for point-of-load voltage regulation. Less than 8 pF capacitance is used within the active filter portion of the proposed voltage regulator for a cutoff frequency of 50 MHz.

Active filters have been well studied over the past several decades [20], [21]. The objective of this section is to review those properties of active filters that affect the design of the proposed voltage regulator while providing some relevant background material. Active filter configurations and topologies relevant to the proposed regulator are reviewed in Section III-A. In Section III-B, the design of the Op Amp circuit is reviewed.

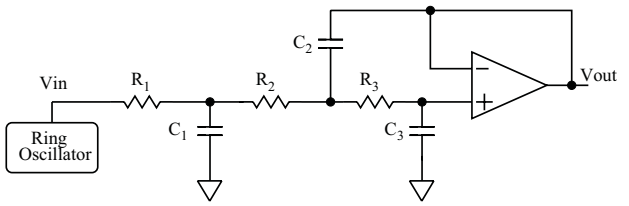


Fig. 4. Active low pass Sallen–Key filter circuit. No dc current path exists between the input and output nodes.

A. Active Filter Design

Active filter structures contain no passive inductors. The filtering function uses capacitors, resistors, and an active circuit (i.e., the Op Amp). Certain design considerations should be considered when utilizing an active filter as a voltage regulator since the appropriate active filter topology depends upon the application. For a voltage regulator, the on-chip area requirement, sensitivity of the active filter to component parameter variations (due to aging, temperature, and process variations), and the power dissipated by the active components should be low. Two topologies are popular for implementing an integrated low pass active filter, i.e., multiple feedback and Sallen–Key [20]. Multiple feedback low pass filters use capacitive and resistive components within the feedback path from the output to the input. A dc current path exists between the input and output nodes due to the resistive feedback. The dc current increases the power dissipated by the multiple feedback active filter. Multiple feedback active filters are therefore less suitable for an active filter-based on-chip voltage regulator. Alternatively, Sallen–Key low pass filters use only capacitive feedback. Hence, the static power dissipation of the Sallen–Key topology is significantly less than that in the multiple feedback topology.

A third order low pass unity gain Sallen–Key filter topology is shown in Fig. 4. The first section, R_1 and C_1, forms a first order low pass RC filter. The remaining components, i.e., R_2, R_3, C_2, C_3, and the Op Amp, form a second order Sallen–Key low pass filter. Note that no dc current path exists between the input and output. The gain of the active filter can be increased by inserting resistive feedback between the noninverting input and output nodes, forming a dc current path between the output and ground. Since low power dissipation is crucial to the proposed circuit, a unity gain topology is chosen.

The transfer function of the active filter shown in Fig. 4 is

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1}{a_1 s^3 + a_2 s^2 + a_3 s + a_4} \tag{4}$$

where

$$\begin{aligned} a_1 &= R_1 R_2 R_3 C_1 C_2 C_3 \\ a_2 &= R_1 C_1 C_3 (R_2 + R_3) + R_3 C_2 C_3 (R_1 + R_2) \\ a_3 &= R_1 C_1 + C_3 (R_1 + R_2 + R_3) \\ a_4 &= 1. \end{aligned}$$

Various filter types exist in the literature with zeros at infinity, e.g., Butterworth, Chebyshev type I, and Bessel [21]. Other filter types such as Elliptic and Chebyshev type II filters exhibit faster transition characteristics. Since the Elliptic and Chebyshev type II filters contain zeros in the transfer function, the Sallen–Key topology depicted in Fig. 4 cannot be used to implement these filters. Zeros can be produced with more complex feedback structures such as a twin-t or bridged-t circuit [21]. These structures, however, have resistors connected to ground, increasing the power dissipated by the active filter.

A Chebyshev type I filter is chosen for the active filter because of the steep roll-off factor as compared to the filter structures that do not require resistive components connected to ground to produce finite zeros. The active filter passes the switching signal at a constant frequency and generates a dc output voltage. A third order Chebyshev type I low pass Sallen–Key filter, shown in Fig. 4, is utilized in the proposed voltage regulator since no attenuation occurs at dc when the order of the Chebyshev filter is odd. The per cent change in the cutoff frequency and the Q factor of the third order Sallen–Key filter, shown in Fig. 4, are listed in Table I for an increase of 1% in the value of the individual parameters.

TABLE I
SENSITIVITY ANALYSIS FOR A THIRD ORDER SALLEN–KEY FILTER. PERCENT CHANGE IN CUTOFF FREQUENCY AND Q FACTOR WHEN INDIVIDUAL PARAMETER VALUES ARE INCREASED BY 1%

	R1	R2	R3	C1	C2	C3
Q	0	–0.4	0.4	0	–0.5	0.5
Cut-off frequency	–1	–0.5	–0.5	–1	–0.5	–0.5

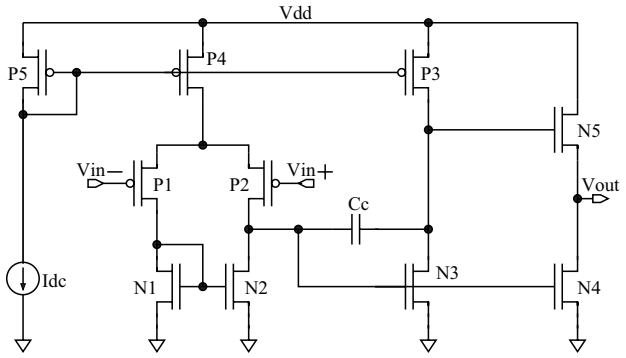


Fig. 5. Three stage Op Amp with PMOS input transistors. The PMOS input transistors are used in the first differential input stage. The second stage is a common-source gain stage and the third stage forms the output buffer that supplies the current to the load.

B. Op Amp Design

The performance of an active filter depends strongly on the Op Amp. The gain–bandwidth product of the Op Amp determines the bandwidth of the active filter. Most of the power loss takes place within the Op Amp structure, since the current provided to the output load is supplied by the Op Amp output stage. Hence, the Op Amp needs to provide tens of milliamps of current to the load devices while maintaining sufficient performance to reliably operate the active filter.

A three stage classical differential-input single-ended CMOS Op Amp structure is utilized in the proposed regulator, as shown in Fig. 5 [22]. The size of transistors in the output

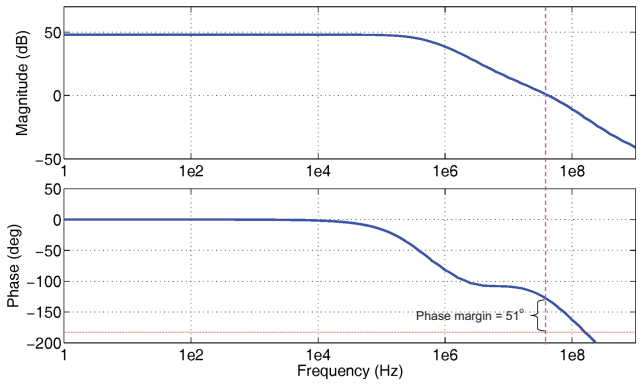


Fig. 6. Magnitude and frequency response of the Op Amp in the active filter. The phase margin is 51°.

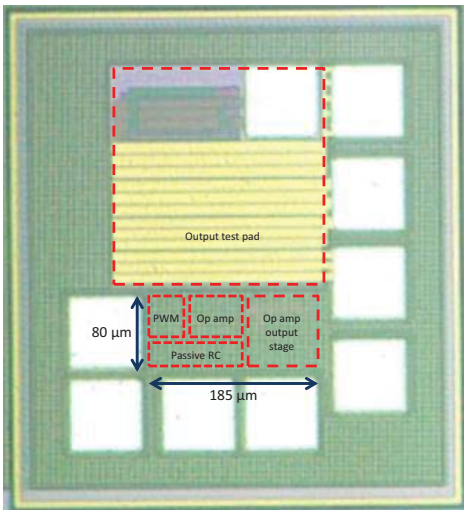


Fig. 7. Die microphotograph of the hybrid voltage regulator.

stage is considerably larger than the first two stages to supply sufficient current to the load circuits. The first and second stages are gain stages which provide a cascade gain of greater than 50 dB. The third stage exhibits a gain close to unity, so the overall three stage gain is close to 50 dB with a phase margin of 51°, as depicted in Fig. 6.

IV. Pros and Cons of Active Filter-Based Voltage Regulator

The proposed voltage regulator is a hybrid of a switching and linear voltage regulator and exhibits certain advantages and disadvantages from using a combination of a switching and LDO regulator topology.

Voltage Regulation: The line and load regulation of the proposed voltage converter is separated into two different feedback paths, as shown in Fig. 3. The response time for abrupt changes in the load current is faster than in a switching regulator and similar to that of an LDO regulator. The line regulation characteristics are, however, similar to those of a switching voltage regulator where the duty cycle of the input switching signal is altered by the PWM. The response time of the PWM significantly affects the line regulation. The bandwidth of the control loop should therefore be designed sufficiently high to provide effective line regulation.

Stability: The stability of a buck converter is typically determined by the effective series resistance (ESR) of the output capacitor. A buck converter can be unstable when the ESR is too small due to a double pole formed by a second order LC filter. The proposed regulator uses an NMOS transistor at the output stage of the Op Amp with a low output impedance, shifting the dominant pole at the output node to a higher frequency. During full load condition, i.e., when the effective load resistance is small, the stability is not significantly degraded because of the small effective output impedance. With an NMOS output stage, the proposed regulator is inherently stable since one of the poles is at a higher frequency. When the Op Amp within the proposed regulator is altered to provide a PMOS output stage to reduce the dropout voltage, the capacitors in the active filter structure (particularly C_2) maintain the stability while reducing the size of any additional output capacitor. In this manner, the stability of the proposed regulator is similar to that of an LDO but does not require a large output capacitor.

On-Chip Area: The physical area of the proposed regulator is smaller than both in a switching and an LDO voltage regulator since there is no large output capacitor. The frequency of the input switching signal can be increased without significantly degrading the power efficiency because the buffers delivering this switching signal can be small. With higher switching frequencies, the size of the proposed regulator can be further decreased. The primary advantage of the proposed regulator as compared to other regulator topologies is the small area requirement and further reduced size in highly scaled technologies without significantly degrading the power efficiency.

Power Efficiency: The power efficiency of a buck converter can theoretically approach 100% when the parasitic impedances are ignored. For an LDO or the proposed hybrid regulator, the maximum attainable power efficiency is limited to $V_{\text{out}}/V_{\text{in}}$, as previously mentioned.

Maximum Load Current: The maximum current that can be delivered to the load depends upon the size of the power transistors (PMOS and NMOS shown in Fig. 2) driving the LC filter. A higher current can be delivered with larger power transistors. The maximum load current of an LDO regulator depends upon the size of the pass transistor. Similarly, the maximum load current of the proposed voltage regulator is determined by the size of the output stage of the Op Amp, where this current can be increased depending upon the load current demand.

V. Experimental Results

The proposed active filter-based DC–DC voltage converter has been designed and fabricated in a 110 nm CMOS technology. The objective of the circuit is the realization of an ultra-small voltage regulator with an area smaller than 0.015 mm^2. A significant portion of this area is allocated to the Op Amp, as shown in Fig. 7. The active filter, Op Amp, and PWM are placed in the remaining available area. The active filter

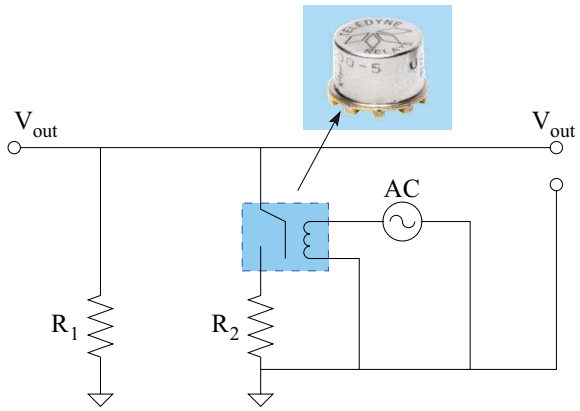
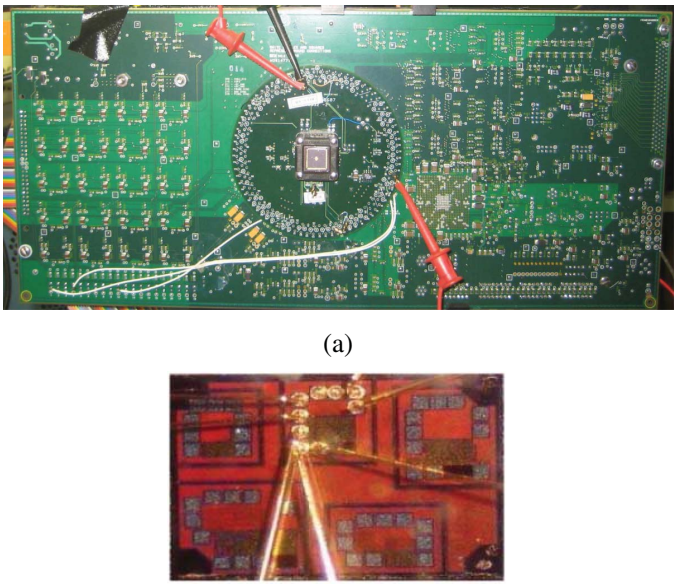


Fig. 8. Setup for load transient testing of the voltage regulator. A Teledyne relay (GRF303 series) is used to switch the output current.



(a)

(b)

Fig. 9. Setup for the chip. (a) Test board. (b) Test circuit with wirebonds.

is designed within the available area with a cutoff frequency of approximately 50 MHz. Note that the cutoff frequency increases when the area of the active filter is reduced. The frequency of the input switching signal should be greater than the cutoff frequency of the active filter so as not to generate high frequency ripple at the output. From simulation results, an 80 MHz input switching signal is observed to be sufficiently high to filter out the high frequency harmonics within the input switching signal. An input switching frequency greater than 80 MHz is not preferred because a higher switching frequency would increase the dynamic power dissipation. A ring oscillator supplies a 50% duty cycle switching signal to the input. Since there is no need for large tapered buffers, the power dissipated by the ring oscillator and output buffers is relatively small. The size of the transistors at the output stage of the Op Amp can be changed for different output voltage or load current demands. The on-chip area of the proposed regulator therefore depends upon the specific output voltage and load current characteristics. Boost circuitry is not utilized in the proposed regulator at the gate of the NMOS source follower because of sufficient margin between the input (1.8 V) and output (0.9 V). A charge pump circuit can be connected to the gate of the source follower to boost the voltage or, if available, a zero threshold NMOS transistor for the output source follower stage can be used to increase the gate voltage.

A 52% increase in regulator area results in more than a three times increase in the current supplied to the load circuitry or a four times reduction in the load regulation. The on-chip area provides up to 80 mA in less than 0.015 mm^2 (185×80 μm), as shown in Fig. 7. This on-chip area is significantly less than that of some recently proposed LDO regulators [7]–[9], [14] and SC voltage regulators [23], [24], as listed in Table II. No capacitor is required at the output node to maintain stability and load regulation, making the proposed circuit convenient for point-of-load voltage regulation.

A Teledyne GRF303 relay switches the output current of the regulator, as shown in Fig. 8. The test board and setup for the load transient testing are illustrated in Fig. 9. The output current is varied between 5 and 70 mA while generating 0.9 V. The experimental results are shown in Fig. 10(a). A zoomed view of the rise and fall transitions of the output voltage is illustrated, respectively, in Fig. 10(a) and (b). The transition time of the current transients is approximately 70 ns. When the output current demand transitions from 5 to 70 mA and from 70 to 5 mA, the output voltage settles in 72 and 192 ns, respectively. Note that no ringing or overshoot in the output voltage occurs during transient operation, exhibiting highly stable operation of the voltage regulator with abrupt changes in the output current demand.

The hybrid voltage regulator dissipates 0.38 mA quiescent current and delivers up to 80 mA current while generating 0.9 V from a 1.8 V input voltage. The current efficiency is over 99% when the output current demand is greater than 40 mA. When the output current demand changes, a dc voltage shift occurs in the generated voltage, as shown in Fig. 11. This dc voltage shift at the output of the regulator is 44 mV when the output current varies between 5 and 70 mA, exhibiting a load regulation of 0.67 mV/mA. With a 52% increase in the voltage regulator area (i.e., utilizing a larger output buffer), the load regulation can be reduced to ~0.17 mV/mA, which is a fourfold decrease in the dc voltage shift at the output voltage. The amplitude of this output dc voltage shift depends strongly on the current supplied to the load circuitry. When the load current demand increases, the effective voltage across N_5 decreases (see Fig. 5). This decrease limits the maximum current that N_5 can supply to the load for a specific output voltage (or limits the output voltage for a specific load current demand). Measurements of the load regulation characteristics of the regulator are illustrated in Fig. 12.

A performance comparison of the proposed circuit with other switching and linear DC–DC converters is listed in Table II. The on-chip area required by the proposed circuit is significantly less than previously proposed state-of-the-

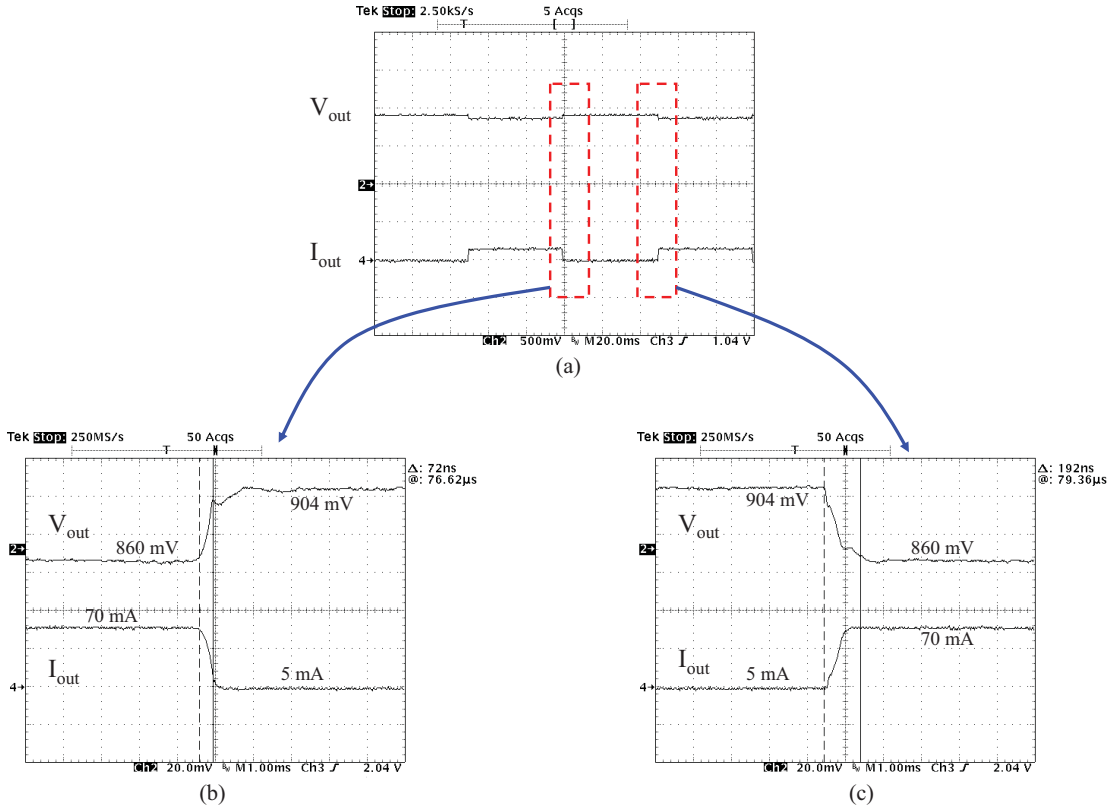


Fig. 10. Measured transient response of the active filter-based voltage regulator (a) when the output current changes from 5 to 70 mA, and a zoomed view of the transient response when the output current changes from (b) 70 to 5 mA and (c) 5 to 70 mA. The transition time for the output current is 70 ns.

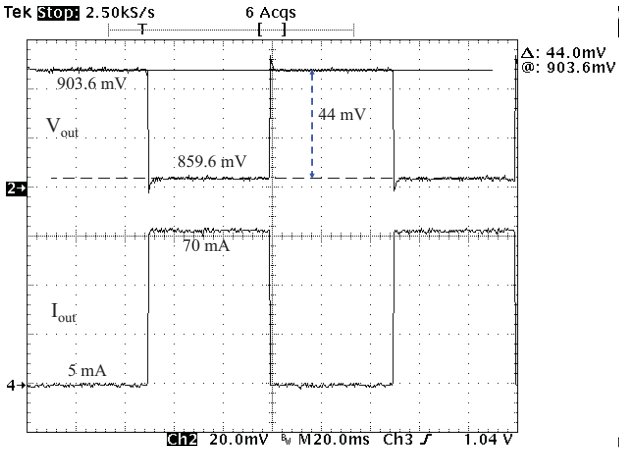


Fig. 11. Measured load regulation when the transient output current changes between 5 and 70 mA. The output dc voltage shift is 44 mV. The transition time of the output current is approximately 70 ns.

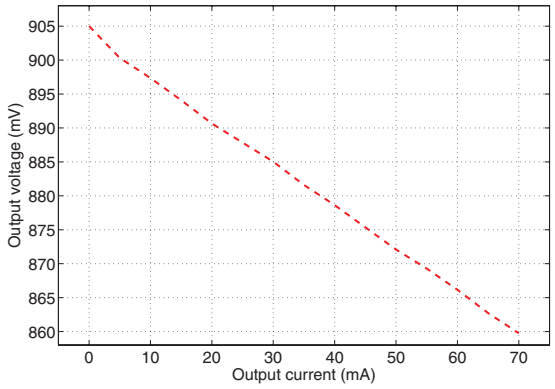


Fig. 12. Measured load regulation of the proposed circuit of approximately 0.67 mV/mA.

art buck converters [5], [6], LDO [7]–[15], and SC voltage regulators [23], [24].

A figure of merit (FOM) is proposed in [14] as

$$\text{FOM}_{\text{guo}} = K\left(\frac{\Delta V_{\text{out}} \cdot I_Q}{\Delta I_{\text{out}}}\right) \quad (V) \tag{5}$$

where K is

$$K = \frac{\Delta t \text{ used in the measurement}}{\text{Smallest } \Delta t \text{ among the compared circuits}} \tag{6}$$

and Δt is the transition time of the load current during test. FOM_{guo} does not, however, consider the speed of the load regulation, which is a primary issue in point-of-load voltage regulation.

A second FOM is therefore proposed that considers the response time and on-chip area of a voltage regulator

$$\text{FOM}_1 = K\left(\frac{\Delta V_{\text{out}} \cdot I_Q}{\Delta I_{\text{out}}}\right) \cdot R_t \cdot A \quad (V\ \mu\text{s mm}^2) \tag{7}$$

where R_t and A are, respectively, the response time and area of the voltage regulator. Since the required area is technology dependent, the fabrication technology can also be

TABLE II
PERFORMANCE COMPARISON AMONG DIFFERENT DC–DC CONVERTERS

	[5]	[25]	[9]	[7]	[8]	[14]	[23]	[24]	This paper
Year	2003	1998	2005	2007	2008	2010	2010	2010	2010
Type	Buck	LDO	LDO	LDO	LDO	LDO	SC	SC	Hybrid
Technology [nm]	80	500	90	350	350	90	45	32	110
Response time [ns]	87[a]	150,000	0.054[b]	270	300	3000–5000	120–1200	N/A	72–192
On-chip area [mm^2]	12.6	1	0.098	0.264	0.045[c]	0.019	0.16	0.374	0.015
Output voltage [V]	0.9	2–3.6	0.9	1.8–3.5	1	0.5–1	0.8–1	0.66–1.33	0.9
Input voltage [V]	1.2	5	1.2	2–5.5	1.2	0.75–1.2	N/A	N/A	1.8
Maximum current [mA]	9500	300	100	200	50	100	8	205	80
Maximum current efficiency	N/A	99.8	94	99.8	99.8	99.9	N/A	N/A	99.5
ΔV_{out} [mV]	100	300	90	54	180	114	N/A	N/A	44
Quiescent current [mA]	N/A	10–750	6	0.02–0.34	0.095	0.008	N/A	N/A	0.38
Load regulation [mV/mA]	0.014[a]	0.5	1.8	0.27	0.28	0.1	N/A	N/A	0.67
Transition time [ns]	N/A	N/A	0.1	100	~150	100	N/A	N/A	70
Transition time ratio (K)	N/A	N/A	1	1000	1500	1000	N/A	N/A	700
$\text{FOM}_1 = K\left(\frac{\Delta V_{\text{out}} \cdot I_Q}{\Delta I_{\text{out}}}\right) \cdot R_t \cdot A$	N/A	N/A	0.029[b]	6.544	6.926[c]	0.893	N/A	N/A	0.518
$\text{FOM}_2 = K\left(\frac{\Delta V_{\text{out}} \cdot I_Q}{\Delta I_{\text{out}}}\right) \cdot \frac{R_t \cdot A}{T}$	N/A	N/A	3.6[b]	53.4	56.5[c]	110.2	N/A	N/A	42.8

[a] Simulation results (not experimental data).

[b] Mathematical analysis (not experimental data).

[c] An off-chip capacitor of 1 nF to 10 μF is required.

included in the FOM_1, assuming a linear reduction in area with technology

$$\text{FOM}_2 = K\left(\frac{\Delta V_{\text{out}} \cdot I_Q}{\Delta I_{\text{out}}}\right) \cdot \frac{R_t \cdot A}{T} \qquad (V\ \mu\text{s}) \qquad (8)$$

where T is the technology node.

Smaller FOM_1 and FOM_2 of a voltage regulator imply a better choice for point-of-load voltage regulation. The regulator described in [9] exhibits the smallest FOMs, however, the response time in [9] is not a measurement result but originates from a mathematical analysis. The voltage regulator presented in this paper exhibits the smallest FOM among all of the remaining circuits despite the comparably high quiescent current (I_Q). By reducing I_Q, the FOM for the proposed regulator can be further reduced.

The LDO proposed in [25] has a source-follower output stage similar to the proposed active filter regulator, as shown in Fig. 1(b). A large capacitor C_1 and slow control circuitry behaving as a charge pump are connected to the gate of the NMOS transistor in the source follower as in [25]. C_1 decouples the gate voltage of the NMOS transistor from the output voltage where voltage variations occur at the source terminal of this transistor. A larger C_1 is therefore needed if the maximum output current demand of the regulator increases, whereas only the size of the output NMOS transistor is increased for the active filter regulator. To provide additional output current, the area is doubled in [25] as compared to the proposed regulator.

The primary disadvantage of the proposed circuit is that the power efficiency is limited to $V_{\text{out}}/V_{\text{in}}$ as in a linear voltage regulator. This power loss, however, is somewhat compensated by replacing the large tapered buffers with smaller buffers which drive the active filter. Additionally, the filter inductor and capacitor related power losses are eliminated by the active filter structure. The primary advantage of the proposed regulator is the smaller on-chip area. Considering the target application of distributed multi-voltage on-chip power supplies, where the local voltage differences are relatively small, this circuit provides a good tradeoff between physical area and power efficiency.

VI. CASE STUDY

Point-of-load voltage regulation can significantly improve the performance of high speed clock distribution networks since the jitter, skew, and delay characteristics of a clock signal depend strongly on the local P/G noise. A dedicated point-of-load voltage regulator can provide a clean power supply voltage to the clock generation circuitry [26]–[28]. The supply voltage connected to the clock generator should be isolated from the supply voltage of the other digital blocks to minimize high frequency switching noise. A dedicated power supply voltage for the clock distribution network has two advantages. First, a clean supply voltage is delivered to the clock distribution network, thereby reducing the jitter induced by the power noise. Second, noise coupling from the clock distribution network to the power distribution network due to high frequency switching is greatly reduced.

Two clock distribution networks with a ring oscillator as the clock source running at 1 GHz, as illustrated in Fig. 13, are presented to evaluate clock jitter. The clock source and buffers within the clock distribution network share the same power distribution network. A dedicated voltage

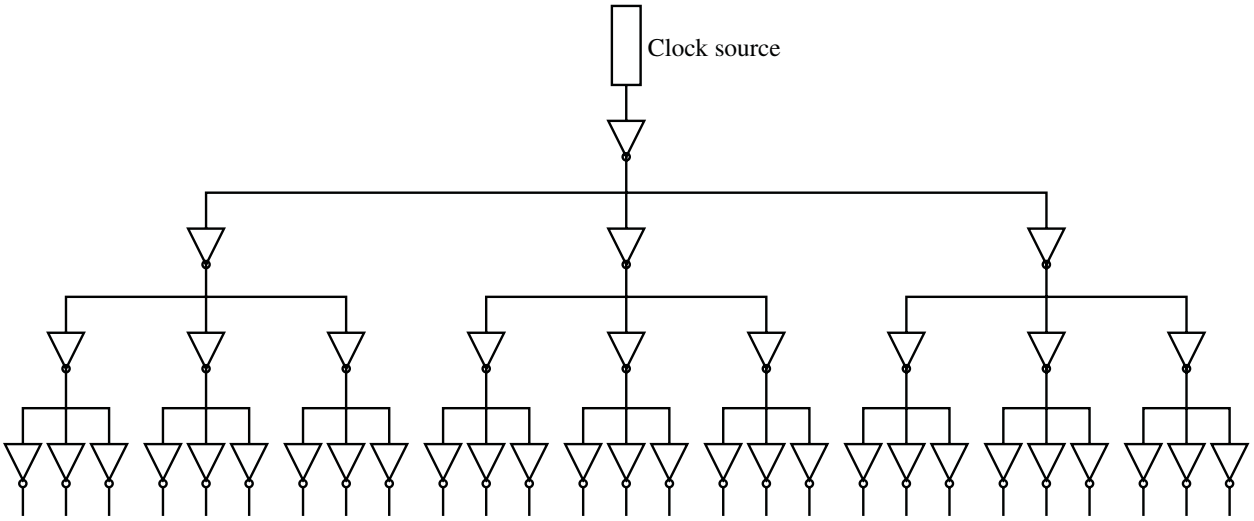


Fig. 13. Four-level clock distribution network with a clock source.

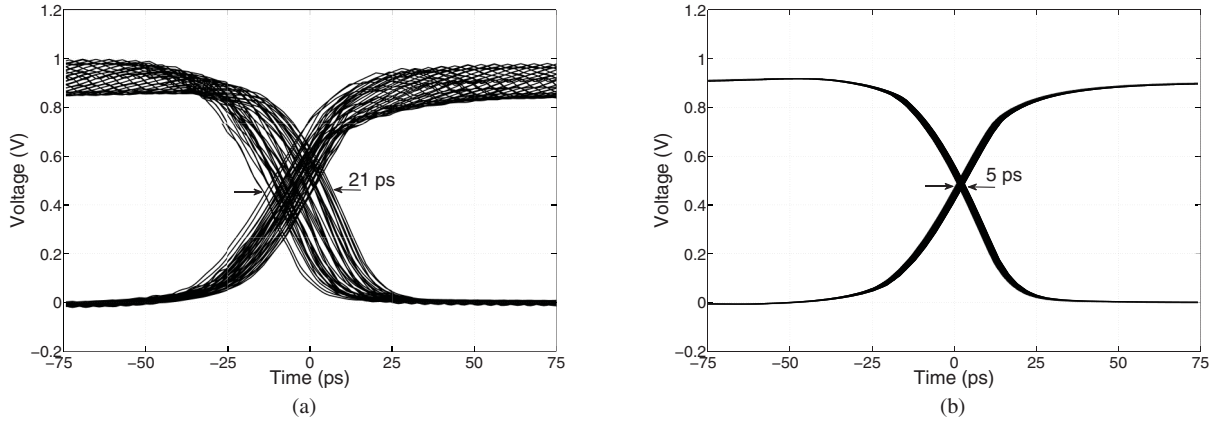


Fig. 14. Clock jitter at the output of the clock source. (a) Clock source and buffers within the clock distribution network sharing the same power network. (b) Dedicated local voltage regulators providing current to the clock source and buffers within the clock distribution network.

regulator provides the supply voltage for the clock source. The buffers within the clock distribution network are also supported by dedicated voltage regulators. The clock jitter at the output of the clock source is compared in Fig. 14 for these two scenarios. The clock jitter at the output of the clock source is approximately 21 ps, as illustrated in Fig. 14(a), where the clock source and buffers within the clock distribution network share the same power distribution network. The switching noise coupled from the clock buffers into the power network induces jitter at the clock source, which increases with greater power noise. The clock jitter at the output of the clock source, with dedicated point-of-load regulators to provide current to the clock generator and buffers within the clock network, is approximately 5 ps, as shown in Fig. 14(b).

The response time and load regulation characteristics of the proposed converter have also been evaluated as the power supply for a clock distribution network, as shown in Fig. 13. The response time is less than 2 ns, and no ringing occurs in the generated voltage after each clock transition, as depicted in Fig. 15. The number of voltage regulators placed throughout the clock distribution network depends upon the available area. The proposed regulator can also be sized to provide the required current for different sized buffers within the clock network.

The point-of-load voltage regulators should be placed close to these large buffers. The number of point-of-load voltage regulators dedicated to the clock distribution network therefore depends upon the jitter constraints on the clock signal and the available area for the voltage regulators.

VII. Distributed On-Chip Point-of-Load Voltage Regulation

Multiple distributed supply voltages provide an effective technique to manage the overall power consumed by an integrated circuit [29], [30]. An active filter-based voltage regulator is a favorable choice for point-of-load voltage regulation due to the small area and flexible drive current to satisfy local current demands. A representative integrated circuit with multiple voltage islands is illustrated in Fig. 16. Global power supplies provide the input voltage to the point-of-load voltage regulators. These point-of-load power

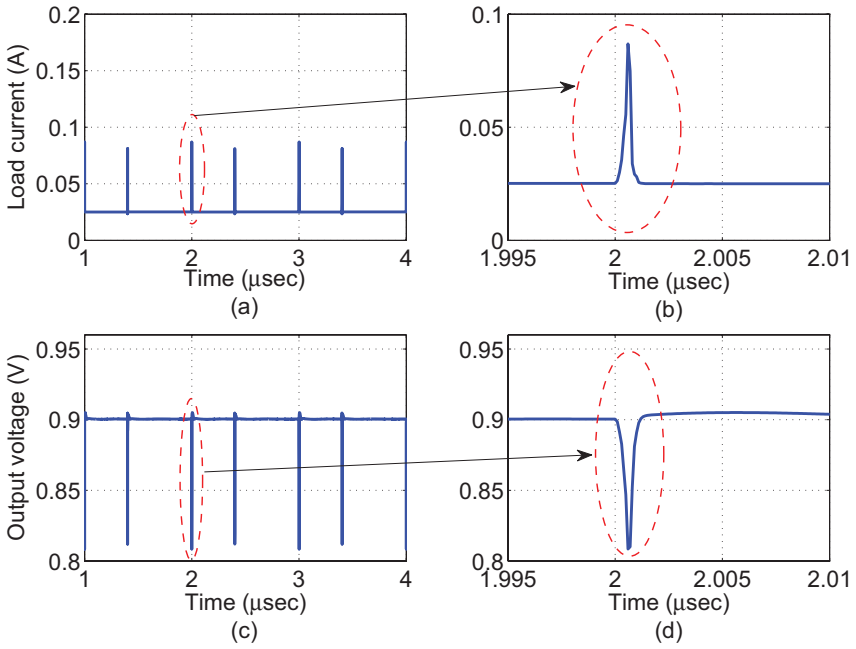


Fig. 15. Simulation of the load regulation of the proposed voltage regulator. (a) Current delivered to clock distribution network. (b) Zoomed view of the output current. (c) Generated voltage exhibiting fast load regulation. (d) Zoomed view of the generated voltage with a 2 ns recovery time. Note that the regulator can track changes in the supply voltage and regulates the supply voltage with no ringing.

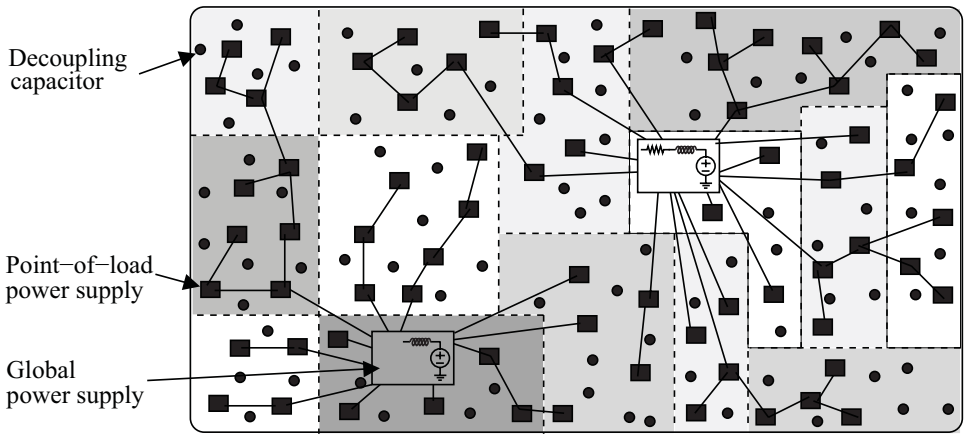


Fig. 16. Point-of-load voltage regulators distributed within different voltage islands to provide a high quality local supply voltage close to the load circuitry.

supplies generate the required voltages within the different voltage islands. The number and size of the voltage regulators depend on the load current demand and output voltage requirements.

The resistive IR and inductive $L\ di/dt$ voltage drops are minimized by generating the supply voltage close to the load circuitry and reducing the parasitic impedance between the power supply and load [31]. Additional power savings is also achieved by reducing the supply voltage within the different voltage islands. The disadvantage of the proposed circuit is the large dropout voltage, thereby reducing the power efficiency. A PMOS output stage, however, can effectively solve this issue without significantly increasing the area. In this case, the Op Amp structure should be modified to drive a PMOS output stage.

VIII. Conclusion

An active filter-based on-chip DC–DC power supply, appropriate for point-of-load voltage regulation, is proposed in this paper. The on-chip area for the proposed fully monolithic hybrid voltage regulator is 0.015 mm^2 and provides up to 80 mA output current. The load regulation is 0.67 mV/mA, and the response time ranges from 72 to 192 ns. The area required for the proposed regulator is significantly less than that of previously proposed state-of-the-art buck converters, LDO, and SC voltage regulators despite using a mature 110 nm CMOS technology. The area of the proposed regulator will therefore be significantly smaller with more advanced technologies. The need for an off-chip capacitor or advanced on-chip compensation techniques to satisfy stability and performance

requirements is eliminated in the proposed circuit. This circuit therefore provides a means for distributing multiple power supplies close to the load to reduce P/G noise while enhancing circuit performance by delivering a high quality supply voltage to the load circuitry. With the proposed voltage regulator, on-chip signal and power integrity will be significantly enhanced with the capability of distributing multiple power supplies.

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