The DML static mode demonstrated the lowest energy dissipation: 2.2× less than CMOS on average, and 5× less than the domino. We presented a basic proof-of-concept of the proposed DML logic by measurements of an 80-nm test chip.

Future work will include the optimization of the DML gates for operation with standard supply voltages, development of a standard library and designing of a benchmark design using a standard ASIC flow.

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Power Network Optimization Based on Link Breaking Methodology

Renatas Jakushokas and Eby G. Friedman

***Abstract*— A link breaking methodology is introduced to reduce voltage degradation within mesh structured power distribution networks. The resulting power distribution network combines a single power distribution network to lower the network impedance, and multiple networks to reduce noise coupling among the circuits. Since the sensitivity to supply voltage variations within a power distribution network can vary among various circuits, the proposed methodology reduces the voltage drop at the more sensitive circuits, while penalizes the less sensitive circuits. Each circuit can behave as an aggressor as well as a victim. The methodology utilizes two matrices describing the aggressiveness and sensitivity of a circuit. The proposed methodology is evaluated for multiple case studies, demonstrating a reduction in the voltage drop in the sensitive circuits. Based on these case studies, the voltage is improved by 5% at those nodes with the highest sensitivity. The voltage prior to application of the link breaking methodology is 96% of the ideal power supply voltage. Lowering the noise on the power network enhances the maximum operating frequency by 16% by utilizing the proposed link breaking methodology. The link breaking methodology has also been compared with a multiple voltage domain methodology, achieving 7% improvement in operating frequency.**

***Index Terms*— Power delivery, power distribution networks, sensitivity factor.**

I. INTRODUCTION

The increasing density and performance of integrated circuits (ICs) requires advancements in design methodologies for the global interconnects, particularly the on-chip power networks, clock networks, and long distance on-chip signals. The on-chip power distribution network typically provides many amperes to the load circuits while utilizing up to 40% of the overall metal resources [1], [2]. With advancements in technology, higher current is required; therefore, efficient on-chip power distribution networks have become an essential element of modern IC design flows.

The power distribution network is conventionally designed to achieve a target impedance over a wide range of frequencies [3]. This target impedance is based on the supply current, producing a maximum voltage drop within an on-chip power network [4]. The overall on-chip power distribution network is designed to satisfy a worst case scenario at a specific location within the grid.

A change in voltage at the power node of a gate can significantly increase the delay of a logic gate [5]–[7], degrading the overall performance of a system [8]. Since different circuits are affected differently by a drop in the power supply voltage, the power distribution network should be designed to satisfy multiple constraints. The voltage level for those gates along the critical path can tolerate the least voltage degradation, whereas the gates along a noncritical path may satisfy speed constraints despite a higher voltage drop [9]. Sertain circuits, for example, such as a phase-locked loop (PLL) and

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The authors are with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY 14627 USA (e-mail: jakushok@ece.rochester.edu; friedman@ece.rochester.edu).

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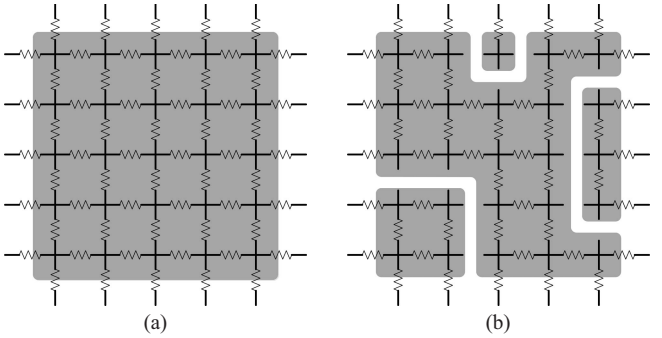


Fig. 1. Mesh structured power distribution network. (a) Single power distribution network focused on reducing the network impedance. (b) Multiple power distribution networks lower the noise at the expense of increasing the network impedance.

voltage controlled oscillator, are highly sensitive to changes in the power supply voltage [10], but digital logic circuits can tolerate much higher variations in the power supply voltage.

Separate power networks can be designed to independently supply current to different parts of a circuit, thereby shielding different parts of an IC from each other. Separate power networks are widely used in mixed-signal circuits, where the current is supplied to the analog and digital circuits by different power networks [11]. For systems requiring the same voltage, this approach may, however, inefficiently utilize metal resources due to additional area and routing constraints [9]. Input/output (I/O) pads are also a limited resource, preventing the use of an excessive number of separate power networks [12]. In Fig. 1, a single and multiple separate power networks are illustrated. With a single network, as shown in Fig. 1(a), the sensitive circuit (e.g., a PLL) and aggressor circuit (exemplified by a large digital logic circuit) share the same power network that lowers the network impedance. A sensitive circuit can, however, be highly affected by the noise generated from the aggressor circuit. With multiple power networks, as shown in Fig. 1(b), one network can be dedicated to the aggressor circuit while another network can be dedicated to the sensitive circuits, minimizing noise coupling between the aggressor and sensitive circuits. This approach, however, results in an increase in the power network impedance and additional routability constraints. The methodology proposed in this brief utilizes a single power network to provide a low network impedance and reduced routability constraints while disconnecting (or breaking) links within the on-chip power network between the aggressor and sensitive circuits, thereby reducing the noise coupling to the sensitive circuits.

This brief is organized as follows. The link breaking methodology is described in Section II. In this section, the optimization objective, sensitivity factor, and a general purpose algorithm are introduced. In Section III, several design cases are evaluated. The degradation in the supply voltage and propagation delay before and after applying the proposed link breaking methodology is summarized. Additional topics related to evaluating and enhancing the link breaking methodology are discussed in Section IV. The conclusions are summarized in Section V.

II. Link Breaking Methodology

A link breaking methodology for determining which links should be removed, thereby shielding the sensitive circuits, is described in this section. This section is composed of three subsections. The sensitivity factor is introduced in Section II-A. In Section II-B, the objective of improving the worst case delay is described. A general purpose algorithm for the link breaking methodology is presented in Section II-C.

Algorithm 1 Pseudocode for link breaking methodology.

LINK-BREAKING
1. Determine voltage drops over power network
2. Calculate initial $delay_{ini}$ function based on (2)
3. Generate x randomly perturbed systems
4. Determine voltage drops for x systems
5. Calculate $delay$ function based on (2) for x systems
6. For every x systems
7. Generate six different networks, where a link is broken at every direction
8. Determine new $delay$ values, maintaining network with lowest $delay$
9. Goto 7, if improvement is achieved
10. Select system with lowest $delay$
11. If $delay_{ini} > delay$, $delay_{ini} \leftarrow delay$ and goto 3

A. Sensitivity Factor

The sensitivity factor describes the relative importance of a change in voltage on the performance of a circuit. A method to describe the sensitivity factor is to investigate the sensitivity of the supplied voltage on the performance (e.g., the propagation delay) of a particular circuit. The sensitivity factor in this case is [13]

$$s = \left.\frac{(\Delta \text{delay}/\text{delay}(x))}{(\Delta V/V(x))}\right|_{x=V_{\text{dd}}} = \frac{\Delta \text{delay}}{\Delta V} \cdot \frac{V_{\text{dd}}}{\text{delay}_{\min}} \tag{1}$$

where Δdelay and $\text{delay}_{\min}$ are, respectively, the change in the delay and the minimum delay of a circuit. The minimum delay is achieved assuming a full V_{dd} at the power rail of the circuit. ΔV is the change in the supply voltage at the node supplied to the circuit. The sensitivity factor is dependent on the type of circuit.

B. Worst Case Delay

Each circuit within a network can be characterized as both an aggressor and a victim; therefore, each node of interest is associated with a matrix composed of two parameters $[i, s]$. Parameter i is an aggressor-related parameter, and is equal to the load current sunk by the circuit. Parameter s is related to the victim parameter, expressing the sensitivity of the circuit connected to the node. The objective is to enhance overall performance, such as minimize the worst case delay

$$\text{delay}_{\text{worst}} = \max\left(\text{delay}_1, \text{delay}_2, \ldots, \text{delay}_k\right) \tag{2}$$

where

$$\text{delay}_j = \text{delay}_{\min - j}\left[\frac{s_j}{V_{\text{dd}}}\Delta V_j + 1\right]. \tag{3}$$

ΔV_j is a change in the voltage at node j due to the load currents and power network impedance. $\text{delay}_{\min - j}$ is the minimum propagation delay of circuit j while applying the maximum supply voltage V_{dd}. s_j is the sensitivity factor of circuit j.

C. General Purpose Algorithm

Pseudocode of the link breaking algorithm for the proposed methodology is provided in Algorithm 1, with the objective of minimizing the worst case propagation delay. In line 1, the voltage drop across the power network is determined. Based on the voltage and sensitivity of the circuits, the initial value of the delay function $\text{delay}_{\text{ini}}$ is determined, as listed in line 2. Multiple power networks x are generated, where each network is perturbed by removing a random link. In lines 4 and 5, the voltage drop and delay are determined for each of the perturbed networks. A search for a local minimum is evaluated for each perturbed system in lines 6–9. The network with the lowest delay is selected in line 10. The process is repeated until the delay cannot be further reduced.

To approach the global minimum, a larger number of perturbed systems x is required. For the evaluated cases, x is set equal to 10%

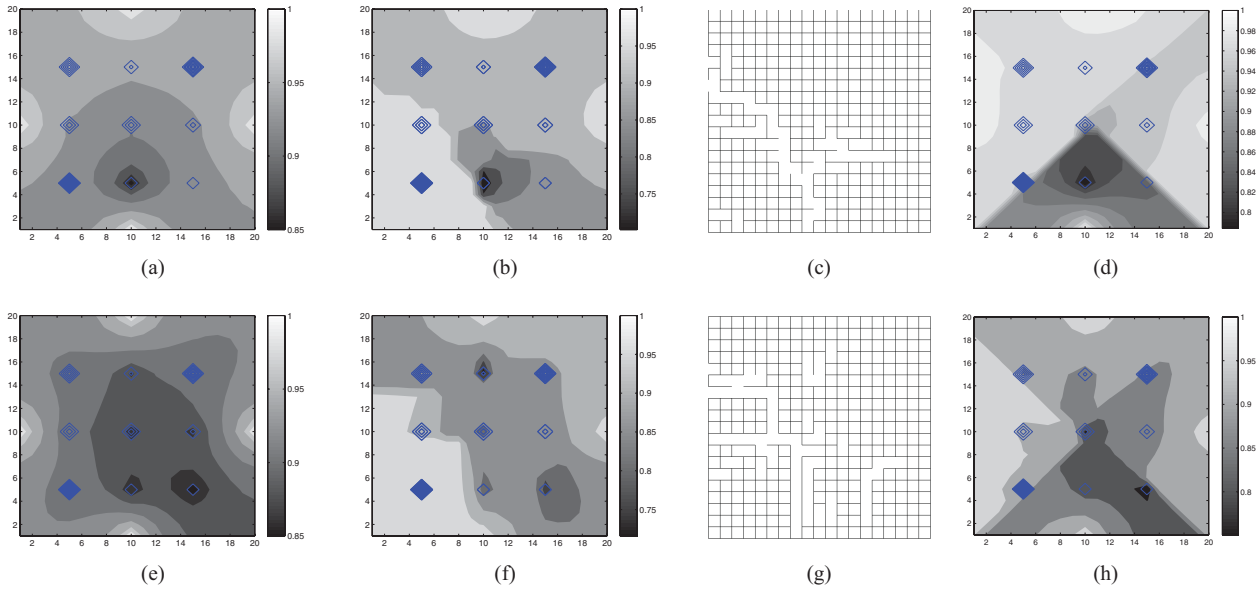


Fig. 2. Map of voltage variations for uniform grid, link breaking, and multiple voltage domains methodologies for two cases. The diamond shapes represent the location of the aggressor and victim circuit blocks. The size of the diamond represents the relative sensitivity factor of a particular block. The resulting power network after application of the link breaking methodology is also illustrated. Case 1 represents the case where a single block sinks significantly higher current than the other blocks. In Case 2, the sunk current, sensitivity factor, and delay are different for various blocks, representing a general design example. Case 1: (a) uniform grid, (b) link breaking methodology, (c) power network after link breaking methodology, and (d) multiple voltage domains. Case 2: (e) uniform grid, (f) link breaking methodology, (g) power network after link breaking methodology, and (h) multiple voltage domains.

of the nodes within the system. A lower runtime is also achieved by evaluating those nodes directly connected to the victim or aggressor circuits.

III. Case Studies

Two study cases are presented in this section. The circuit is composed of nine blocks in each example. The sensitivity factor and critical delay of each block are assumed to be different. For the first case, block number 2 is assumed to sink significantly greater current, representing the case of a single dominant aggressor. In the second case, the sunk current is varied among all of the blocks, representing a general type of circuit. The design objective is to minimize the worst case propagation delay, as expressed in (2).

A mesh structured power distribution network with 20×20 number of nodes is considered. Four 1 V power supplies are connected at the center of the four edges (left, right, top, and bottom). The maximum permitted degradation in supply voltage is 0.3 V.

The supply voltage map before and after application of the link breaking methodology, as well as the resulting power network, are illustrated in Fig. 2. The current sunk before and after application of the methodology, sensitivity, propagation delay, and improvement in the supply voltage and propagation delay are listed in Table I.

In the first case [see Fig. 2(a) and (b)], the current sunk by the aggressor is significantly higher than the other circuit blocks. The highest degradation in supply voltage is within the aggressor circuit. The supply voltage, however, is greater (the voltage drop is lower) in those circuit blocks with a higher sensitivity and minimum delay, resulting in a reduction in the worst case delay and an increase in the maximum operating frequency. The increase in the supply voltage at block 1 is 5%, achieving 97% of the ideal power supply voltage and resulting in an improvement in the propagation delay of 18%. Note that the improvement in the delay is greater than the supply voltage because of the high sensitivity factor. After applying the link breaking methodology, blocks $1, 4$, and 6 exhibit a similar worst case propagation delay, demonstrating the effectiveness of the proposed methodology.

In the second case [see Fig. 2(e) and (f)], the current is different among several blocks. After applying the link breaking methodology, the supply voltage at block 1 is increased by 5% and the maximum operating frequency is enhanced by 20%.

A multiple voltage domain methodology has been applied to both case studies for comparison with the link breaking methodology. In the multiple voltage domain methodology, the power distribution network is divided into four separate networks. The voltage variation map for multiple voltage domains is shown in Fig. 2(d) and (h). Based on these case studies, the maximum voltage drop occurs at blocks two and three, respectively, for the first and second case study. A comparison of the link breaking methodology with the multiple voltage domain methodology is also summarized in Table I. A 6% and 8% improvement in delay for these case studies is achieved by utilizing the link breaking methodology as compared with multiple voltage domains.

IV. Discussion

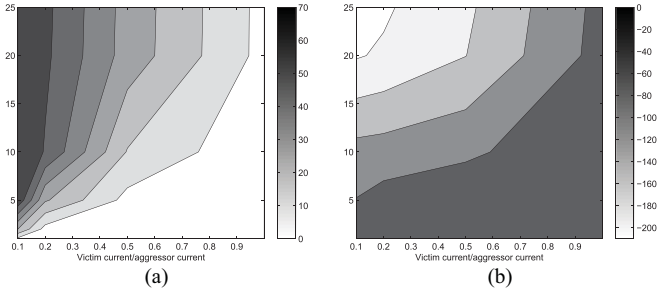
The voltage drop within a power distribution network is investigated for circuit blocks with different current levels and sensitivities. The minimum propagation delay, $\text{delay}_{\text{min}}$, is maintained. A 20×20 mesh structured power distribution network with two power supplies and two current sources (one aggressor and one victim) is considered. The voltage improvement at the victim and degradation at the aggressor are illustrated, respectively, in Fig. 3(a) and (b). Note that by assigning a higher sensitivity to the victim circuit, the voltage drop on the power network at the victim is reduced. Simultaneously, the voltage drop at the aggressor is increased, but the aggressor is less sensitive to voltage variations. The tradeoff between reducing the voltage drop at the victim while increasing the voltage drop at the aggressor is an important aspect of the proposed link breaking methodology.

In the current version of the link breaking methodology, an optimization step is performed to reduce the DC noise (or worst

TABLE I

SENSITIVITY FACTOR, SUNK CURRENT, MINIMUM DELAY, SUPPLY VOLTAGE, AND PROPAGATION DELAY UTILIZING UNIFORM GRID, LINK BREAKING, AND MULTIPLE VOLTAGE DOMAINS METHODOLOGY FOR THE NINE CIRCUIT BLOCKS. THE IMPROVEMENT OR DEGRADATION UTILIZING THE LINK BREAKING METHODOLOGY IN THE SUPPLY VOLTAGE, PROPAGATION DELAY, AND MAXIMUM OPERATING FREQUENCY ARE ALSO LISTED. CASE 1 REPRESENTS THE CASE WHERE A SINGLE BLOCK SINKS SIGNIFICANTLY HIGHER CURRENT AS COMPARED WITH THE OTHER BLOCKS. IN CASE 2, THE SUNK CURRENT, SENSITIVITY FACTOR, AND DELAY ARE DIFFERENT FOR VARIOUS BLOCKS, REPRESENTING A GENERAL DESIGN CASE

Block number		1	2	3	4	5	6	7	8	9	$f_{\max} = \frac{1}{\text{delay}_{\text{worst}}}$
Sensitivity factor (s)		5	1	1	2	2	1.3	3	1.2	4	——
Delay [ps] @ $V_{\text{dd}} = 1V$		670	300	650	710	200	690	300	300	300	——
Case 1 [see Fig. 2(a), (b), and (d)]											
Sunk current		1	10	1	1	1	1	1	1	1	——
Voltage	Uniform grid [mV]	924	850	924	936	920	933	943	940	942	——
	Link breaking [mV]	973	702	861	965	896	921	921	925	931	——
	Multiple voltage domains [mV]	955	784	843	967	908	946	953	964	938	——
Delay	Uniform grid [ps]	988	369	748	856	248	803	376	343	395	1.01 GHz
	Link breaking [ps]	829	422	807	834	263	828	403	356	417	1.20 GHz
	Multiple voltage domains [ps]	887	393	824	832	256	776	364	322	403	1.13 GHz
	Impr. versus uniform grid [%]	16.0	−15.0	−7.8	2.6	−6.1	−3.2	−7.2	−3.7	−5.7	18.8
	Impr. versus multiple voltage domains [%]	6.6	−7.5	2.0	−0.2	−2.9	−6.7	−10.9	−10.4	−3.4	6.2
Case 2 [see Fig. 2(e), (f), and (h)]											
Sunk current		1	5	5	2	2	3	1.3	4	1.2	——
Voltage	Uniform grid [mV]	907	861	850	901	874	875	907	876	901	——
	Link breaking [mV]	958	825	781	928	838	864	852	716	890	——
	Multiple voltage domains [mV]	936	818	751	941	789	868	890	881	876	——
Delay	Uniform grid [ps]	1050	366	800	910	268	860	411	369	448	952 MHz
	Link breaking [ps]	870	378	847	870	283	869	463	430	463	1.15 GHz
	Multiple voltage domains [ps]	947	380	868	851	303	866	426	367	482	1.06 GHz
	Impr. versus uniform grid [%]	17.1	−3.2	−5.8	4.5	−6.0	−1.1	−12.7	−16.5	−3.3	20.8
	Impr. versus. multiple voltage domains [%]	8.1	0.6	2.4	−2.3	6.7	−0.3	−8.6	−17.1	3.9	8.5



(a) (b)

Fig. 3. Change in voltage drop for (a) victim and (b) aggressor circuits. The darker shade represents a greater reduction in the voltage drop at the victim and a small increase in the voltage drop at the aggressor.

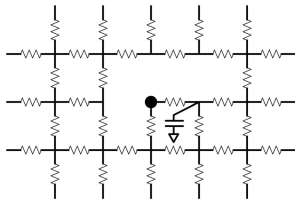


Fig. 4. Decoupling capacitor is placed in close electrical proximity to the sensitive node (shown as a black dot) and is kept electrically distant from other nodes (all nodes to the left of the black dot). In this configuration, the majority of the charge from the decoupling capacitor is devoted to the sensitive node.

case voltage drop) at the more sensitive nodes. The link breaking methodology, however, can be revised to also reduce AC noise within a power distribution network. This change increases the computational complexity, since transient load currents also need to be considered. The sensitivity of the circuits based on the AC noise or the integral of the voltage drop is also required. To further enhance this methodology, the power network can be modeled as an inductive and resistive impedance to also consider simultaneous switching noise.

The proposed algorithm, depicted in Algorithm 1, is a general purpose algorithm not chosen with computational complexity in mind. Computational complexity can be reduced by evaluating only those nodes in the power distribution network directly connected to the victim and aggressor circuits, or clustering victim and aggressor nodes into groups. In those cases, where the number of nodes is low, the random walk approach [14] can be used, significantly reducing the computational complexity since the matrix inversion step is no longer needed.

In large scale networks, the computational complexity can be reduced by hierarchical partitioning or applying multigrid techniques [15]. In either case, the power network is smaller, optimized locally, and later combined. Note that the link breaking methodology can be applied at each stage, initially within a small portion of the power network and at each higher hierarchical level, only breaking the links at the intersection of the partitioned power network.

The link breaking methodology can also be applied at two separate stages. Initially, at the floorplanning stage, based on current consumption expectations and the impedance of the power distribution network, the majority of the links may be broken to improve performance. At the final stage of the design process, the link breaking

methodology may again be applied to further refine the design of the power distribution network.

Decoupling capacitor allocation can also be integrated into the link breaking methodology, further improving power integrity. In Fig. 4, a decoupling capacitor is placed electrically close to a sensitive circuit and kept electrically distant from other circuits [16]. In this configuration, the majority of the charge from the decoupling capacitor is dedicated to the sensitive circuits. Including decoupling capacitor placement within this link breaking methodology or breaking the links while considering the placement of the decoupling capacitors can further optimize the overall power network.

V. Conclusion

The design of the power distribution network is an essential part of an IC design flow. The network is typically designed as a single network or multiple separate networks. The advantages of a single network are reduced network impedance and fewer routability constraints, while multiple separate networks have the advantage of lower noise coupling. The proposed link breaking methodology utilized a single network, disconnecting the links between the aggressive and sensitive circuits, thereby isolating the victim from the aggressor. This approach reduced the noise, while maintaining a low network impedance.

Sensitivity to changes in the supply voltage varies for different circuits. A smaller voltage drop is more important in long critical paths as compared with shorter, less critical logic paths. Voltage variations at the more sensitive circuits need to be reduced at the expense of increased voltage variations at the less sensitive circuits.

The proposed methodology is based on a mesh structured power distribution network. The aggressiveness and sensitivity of a circuits are considered during the link breaking process. The methodology is evaluated for several cases with a different number and magnitude of current and sensitivity factors. The objective for these cases is reduced worst case propagation delay by increasing the supply voltage at blocks with a high propagation delay. An average enhancement of 5% in power supply voltage at nodes with high sensitivity and high propagation delay is achieved, resulting in, on average, 96% of the ideal power supply voltage at these nodes. As a result, an average improvement of 16% in the maximum operating frequency is achieved when utilizing the proposed link breaking methodology. The link breaking methodology is also compared with a multiple voltage domain methodology, achieving an average 7% improvement in operating frequency.

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