Digitally Controlled Pulse Width Modulator for On-Chip Power Management

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***Abstract*— A digitally controlled current starved pulse width modulator (PWM) is described in this paper. The current from the power grid to the ring oscillator is controlled by a header circuit. By changing the header current, the pulse width of the switching signal generated at the output of the ring oscillator is dynamically controlled, permitting the duty cycle to vary between 25% and 90%. A duty cycle to voltage converter is used to ensure the accuracy of the system under process, voltage, and temperature (PVT) variations. A ring oscillator with two header circuits is proposed to control both duty cycle and frequency of the operation. Analytic closed-form expressions for the operation of a PWM are provided. The accuracy and performance of the proposed PWM is evaluated with 22-nm CMOS predictive technology models under PVT variations. An error of less than 3.1% and 4.4% in the duty cycle, respectively, with and without constant frequency control is reported for the PWM. A constant operation frequency with less than 1.25% period variation is demonstrated. The proposed PWM is appropriate for dynamic voltage scaling systems due to the small on-chip area and high accuracy under PVT variations.**

***Index Terms*— Current starvation, digital-controlled oscillators, pulse width modulation, ring oscillators.**

I. Introduction

VOLTAGE controlled oscillators (VCOs) are widely used to generate a switching signal where certain characteristics of this signal can be controlled. Two types of VCOs are primarily used in high performance integrated circuits (ICs), inductor-capacitor (LC) oscillators, and ring oscillators. LC oscillators can operate at high frequencies and exhibit superior noise performance. Alternatively, ring oscillators occupy significantly smaller on-chip area with a wider tuning range. Due to these advantages, ring oscillators have found widespread use in modern ICs [1]–[6].

A conventional ring oscillator consists of an odd number of inverters where the output of the last inverter is fed back to the input of the first inverter, as shown in Fig. 1. The delay provided by each inverter in this chain produces a phase shift in the switching signal. The sum of these individual delays (i.e., phase shifts) and the feedback from the last to the first inverter produces a total phase shift of 2π that causes the circuit to oscillate. The frequency of this oscillation depends upon the sum of the inverter delays within the chain [7].

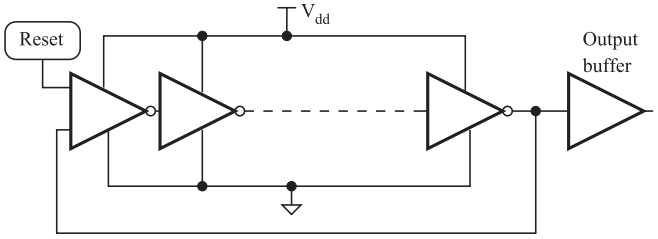

Fig. 1. Conventional ring oscillator. Note that an odd number of inverters is required for the system to oscillate.

The duty cycle of the generated switching signal is typically 50% for conventional ring oscillators where the pMOS and nMOS transistors within the inverters provide the same rise and fall transition times. The duty cycle of a ring oscillator can be tuned by controlling the transition time of the inverters within the ring oscillator. Header and footer circuits are widely used to control the current supplied to the pMOS and nMOS transistors within the ring oscillator inverter chain [8]. Although the header and footer circuits are typically used to control the frequency, these circuits can also control the duty cycle of a ring oscillator.

In this paper, a digitally controlled pulse width modulator (PWM) comprised of a header circuit, ring oscillator, and duty cycle to voltage (DC2V) converter is described. The duty cycle of the PWM is determined from proposed closed-form expressions, yielding a simple dependence on the header current. The high accuracy of the proposed expressions is confirmed by simulation results. The header circuit controls the amount of current delivered to the pMOS transistors within the ring oscillator. Contrary to conventional header circuits, where the header is connected to all of the inverters within the ring oscillator chain, the proposed header circuit is connected to every other inverter stage to dynamically control the pulse width of the output signal. This header circuit provides a high granularity duty cycle control with a step size of 2% of the period. An additional header circuit regulates the supply current delivered to the remaining inverter stages, providing improved control while maintaining a constant switching frequency. Additionally, a DC2V converter, based on the frequency to voltage converter proposed in [9], maintains the accuracy of the PWM under process, voltage, and temperature (PVT) variations. Under PVT variations, the maximum change in duty cycle is less than 2.7% of the period.

Manuscript received March 28, 2013; revised August 28, 2013; accepted November 24, 2013. Date of publication January 9, 2014; date of current version November 20, 2014.

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Digital Object Identifier 10.1109/TVLSI.2013.2294402

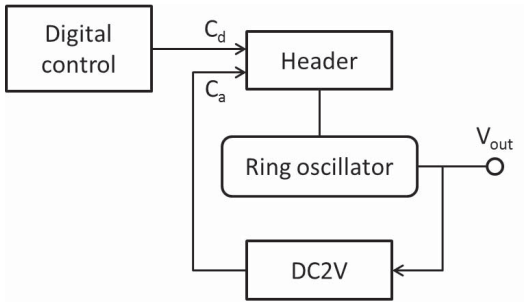


Fig. 2. Proposed PWM. The header circuitry has two input control signals, digital control (C_d) and analog control (C_a). C_d is used to dynamically change the individual transistors to provide a high granularity duty cycle control whereas C_a maintains a constant current from the header to the ring oscillator under PVT variations.

Owing to the small on-chip area, fast control circuitry, high accuracy under PVT variations, and dynamic duty cycle and frequency control governed by accurate closed-form expression, the proposed PWM is an effective circuit to dynamically change the duty cycle of the input switching signal for on-chip voltage regulators. This circuit enables high granularity dynamic voltage scaling at runtime and reduces the response time from milliseconds to nanoseconds.

The remaining part of this paper is organized as follows. The proposed PWM architecture is described in Section II, where the working principle of the header circuitry and DC2V converter is explained, and the analytic expressions for the proposed PWM timing parameters are provided. In Section III, the functionality and accuracy of the proposed circuit under PVT variations are validated with predictive technology models at the 22-nm technology node. Some concluding remarks are offered in Section IV.

II. Description of the Proposed PWM Architecture

A schematic of the proposed PWM is shown in Fig. 2. A header circuit is connected to the ring oscillator to current starve every other stage in the ring oscillator chain. Digital control circuitry provides multiple control signals (C_d) to dynamically change the duty cycle, and a DC2V converter ensures the accuracy of the duty cycle under PVT variations by providing an analog signal to the header circuit. The working principles of these circuits are explained in the following sections.

A. Header Circuitry

An addition based current source, as shown in Fig. 3, has been proposed in [10]. This circuit is used, as a header in [11] to compensate for temperature and process variations by maintaining a constant current to the ring oscillator. Note that this header circuit has one input voltage that controls the gate voltage of M_1 and M_2. By controlling this gate voltage, the sum of the current is maintained constant over a wide range of temperature and process variations [11].

Alternatively, in this paper, a modified version of this header circuit, as depicted in Fig. 4, is introduced to control the duty cycle by changing the transition time of the pMOS transistors at every other inverter stage within the ring oscillator.

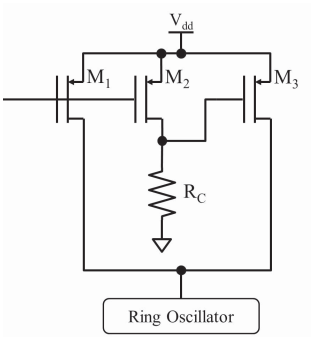


Fig. 3. Addition-based current source used as a header circuit [11].

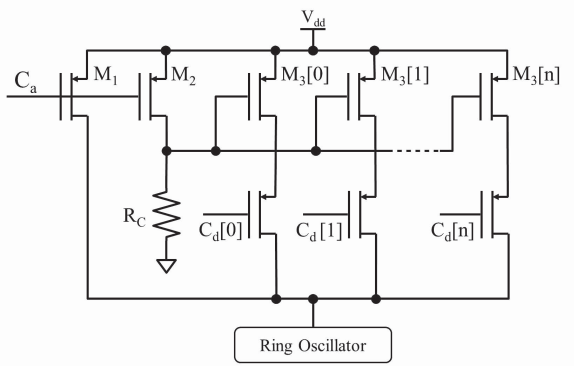


Fig. 4. Parallel pMOS transistors replace M_3 to improve the granularity of the current control as well as behave as switch transistors to turn on different sections of the header circuitry.

Gates M_1 and M_2 are controlled by the analog signal C_a. As opposed to a single transistor M_3 whose gate is connected to a resistor, as shown in Fig. 3, multiple parallel pMOS transistors $M_3[0:n]$ are added in place of M_3 in the proposed header circuit. The pMOS transistors are designed with increasing device size and individually tuned to provide both increased dynamic range and dynamic control of the duty cycle with 2% increments. All of these transistors have the same gate-to-source voltage, but the voltage at the drain terminals is controlled by other switch transistors. Additional pMOS transistors are connected in series with these transistors as switch transistors. The gate voltage of these switch transistors is controlled by a digital controller that turns on (and off) the individual header stages through control signals $C_d[0:n]$. Turning on the entire header stages produces the maximum current to the ring oscillator, which in turn minimizes the duty cycle. The variations in the leakage current are more prominent when the device size is small. To mitigate these variations, larger than minimum size transistors are used in sub-65-nm technology nodes [12]. The first two transistors in the header circuit (M_1 and M_2) are therefore comparably large to minimize any mismatches. A minimum channel length of 150 nm is used for these two input transistors as opposed to 40 nm for the other transistors.

B. Duty Cycle to Voltage Converter

The frequency to voltage converter proposed in [9] is used as a DC2V converter. A circuit schematic of this DC2V converter is shown in Fig. 5.

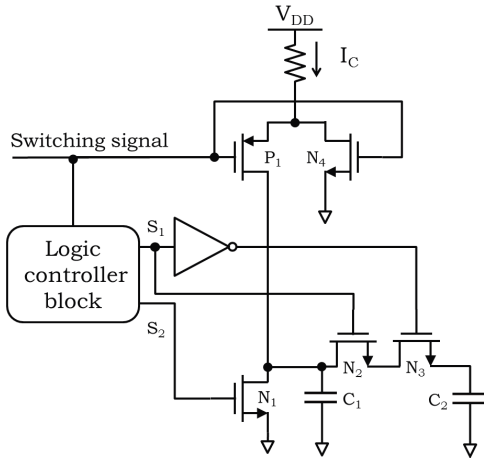


Fig. 5. Frequency to voltage converter proposed in [9] used as a DC2V converter.

There are primarily three different phases of this circuit. During the first phase, capacitor C_1 is charged through transistor P_1. In the second phase, transistors (i.e., switches) N_2 and N_3 are turned on to allow charge sharing between C_1 and C_2. During the last phase, C_1 is discharged through N_1. The charge time of C_1 depends upon the duty cycle of the input switching signal. A signal with a greater duty cycle causes more charge to accumulate on C_1, increasing the output voltage of the DC2V converter. The proposed DC2V converter controls the bias current from the header circuitry through negative feedback, mitigating PVT variations. Intuitively, when the header current is reduced, the duty cycle of the ring oscillator is greater, increasing the output voltage of the DC2V converter. As a result, the voltage at the gate of the M_2 transistor increases and the current IC through resistor R decreases, pulling down the gate voltage of the active header stages. Thus, the current flow through the header to the ring oscillator is increased, compensating for the original reduction in current. A more complete explanation of the working principles of this circuit as well as the logic controller block is available in [9].

C. Ring Oscillator Topology for Pulse Width Modulation

To create a single low-to-high oscillation at the output of the ring oscillator, the signal propagates twice through the entire ring oscillator stages. During the first pass, the pMOS transistor in the odd stages (P_{odd} transistors) and the nMOS transistor in the even stages (N_{even} transistors) are active, contributing to the T_{high} delay of the switching signal at the output of the ring oscillator. Alternatively, during the second round, the pMOS transistor in the even stages (P_{even} transistors) and the nMOS transistor in the odd stages (N_{odd} transistors) are active, determining the T_{low} delay. A periodic signal that switches between zero and 1 V with duty cycle D and constant frequency $1/P$ is considered in this paper. The period and duty cycle of a switching signal are defined in this paper, respectively, as

$$P \equiv T_{\text{high}} + T_{\text{low}} \tag{1}$$

$$D \equiv \frac{T_{\text{high}}}{T_{\text{high}} + T_{\text{low}}}. \tag{2}$$

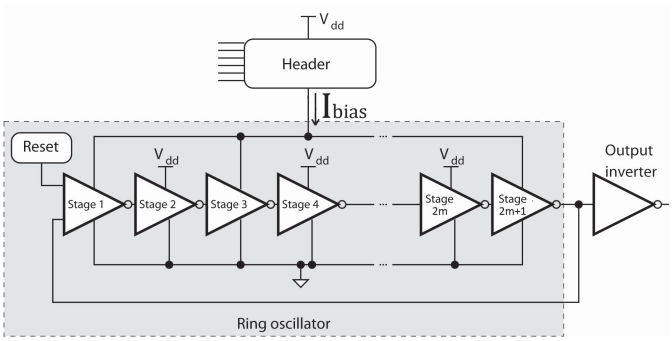


Fig. 6. Ring oscillator with current controlled P_{odd} transistors.

All of the MOSFET transistors are designed with similar rise and fall transition times, contributing equally to the high and low portions of the output signal. The half period of a conventional 50% duty cycle ($T_{0,\text{high}} = T_{0,\text{low}}$) ring oscillator with $2m + 1$ stages is therefore

$$T_0 = T_{0,\text{high}} = T_{0,\text{low}} = (2m+1)\frac{C_G \Delta V_{\text{out}}}{I_{\text{ave}}} \tag{3}$$

where C_G is the input gate capacitance of the next stage, ΔV_{out} is the voltage change at the output during a single rise/fall transition, and I_{ave} is the average current flowing through a single stage active transistor. The period and duty cycle of a conventional ring oscillator are, respectively, $P_0 = 2T_0$ and $D_0 = 1/2$.

The time required to charge the output capacitance of each ring oscillator stage, $C_G \Delta V_{\text{out}}/I_{\text{ave}}$, depends directly on the current flowing through the stage, affecting the response of the following stage and the frequency of the switching signal at the output. Lower (higher) than I_{ave} current through all of the P_{odd} and/or N_{even} transistors slows down (speeds up) the response of these stages, increasing (decreasing) the $T_{0,\text{high}}$ delay, duty cycle, and period of the switching signal at the output. Alternatively, current starvation (enhancement) of all of the P_{even} and/or N_{even} transistors slows down (speeds up) the response of these stages. The $T_{0,\text{low}}$ delay is therefore increased (decreased) in this configuration, decreasing (increasing) the duty cycle and increasing (decreasing) the period of the switching signal at the output. By connecting certain ring oscillator stages to a header circuit (in this case, the odd stages), the duty cycle of the ring oscillator can be controlled through starvation/enhancement of the current flowing to the ring oscillator stages. The effect of current starvation/enhancement on the ring oscillator timing behavior is illustrated in Table I.

Consider a ring oscillator with $2m + 1$ stages with a header connected to $m + 1$ P_{odd} transistors, supplying the current $I_{\text{bias}} = \alpha I_{\text{ave}}$, as shown in Fig. 6. During the first round, only the biased P_{odd} and the affected N_{even} transistors are active, contributing, respectively, T_{bias} and $T_{\text{bias\_affected}}$ delays to the $T_{\text{bias,high}} = T_{\text{bias}} + T_{\text{bias\_affected}}$ delay at the output of the ring oscillator. The delay contribution of the $m + 1$ biased stages to the ring oscillator period is

$$T_{\text{bias}} = \frac{(m+1)C_G \Delta V_{\text{out}}}{I_{\text{bias}}} = \frac{m+1}{2m+1}\frac{T_0}{\alpha}. \tag{4}$$

TABLE I
TIMING PARAMETERS OF THE CURRENT CONTROLLED (STARVED/ENHANCED) RING OSCILLATOR

Controlled stages	Affected stages	Current flow at the starved (enhanced) stage	Transition delay at the controlled and affected stages	T_{high}	T_{low}	Duty cycle	Period
P_{odd}	N_{even}	$\Downarrow$ ($\Uparrow$)	$\Uparrow$ ($\Downarrow$)	$\Uparrow$ ($\Downarrow$)	Unchanged	$\Uparrow$ ($\Downarrow$)	$\Uparrow$ ($\Downarrow$)
N_{even}	P_{odd}	$\Downarrow$ ($\Uparrow$)	$\Uparrow$ ($\Downarrow$)	$\Uparrow$ ($\Downarrow$)	Unchanged	$\Uparrow$ ($\Downarrow$)	$\Uparrow$ ($\Downarrow$)
P_{even}	N_{odd}	$\Downarrow$ ($\Uparrow$)	$\Uparrow$ ($\Downarrow$)	Unchanged	$\Uparrow$ ($\Downarrow$)	$\Downarrow$ ($\Uparrow$)	$\Uparrow$ ($\Downarrow$)
N_{odd}	P_{even}	$\Downarrow$ ($\Uparrow$)	$\Uparrow$ ($\Downarrow$)	Unchanged	$\Uparrow$ ($\Downarrow$)	$\Downarrow$ ($\Uparrow$)	$\Uparrow$ ($\Downarrow$)

Limiting the header current ($\alpha < 1$) to the P_{odd} transistors increases the transition delay of these stages, slowing the input transition time of the conventionally connected N_{even} transistors. Under these conditions, the conventionally connected N_{even} transistors switch more slowly. Alternatively, in those configurations, where the P_{odd} transistors are enhanced ($\alpha > 1$) rather than starved, the input at the driven N_{even} transistors approaches an ideal step input, yielding faster switching of these conventionally connected stages. The delay of a conventional ring oscillator stage driven by a biased stage is inversely proportional to the bias current. The contribution of the m conventionally connected N_{even} transistors to the period of the biased ring oscillator is therefore

$$T_{\text{bias\_affected}} = \frac{m}{(2m+1)}\frac{T_0}{\alpha}. \tag{5}$$

During the second round, only the P_{even} and N_{odd} transistors are active, contributing to the $T_{\text{bias,low}}$ delay at the output of the ring oscillator. These transistors are not biased and are therefore unaffected by the biased stages of the ring oscillator. Thus, the $T_{\text{bias,low}}$ delay remains unchanged $T_{\text{bias,low}} = T_{0,\text{low}} = T_0$, determining the duty cycle of the proposed ring oscillator

$$D_{\text{bias}} = \frac{T_{\text{bias,high}}}{T_{\text{bias,high}} + T_{\text{bias,low}}} = \frac{1}{1+\alpha}. \tag{6}$$

The period of the proposed ring oscillator is therefore

$$P_{\text{bias}} = T_{\text{bias,high}} + T_{\text{bias,low}} = T_0\left(1+\frac{1}{\alpha}\right) = \frac{T_0}{1-D}. \tag{7}$$

The duty cycle of a biased ring oscillator is a function of the bias parameter $\alpha = I_{\text{bias}}/I_{\text{ave}}$ and does not depend on the number of stages $2m+1$. For $\alpha = 1$, a duty cycle of 50% in (6) corresponds to a duty cycle of a conventional ring oscillator with balanced rise and fall times. Alternatively, the theoretical 100% duty cycle limit is achieved as $\alpha \to 0$.

The proposed approach allows configuring a ring oscillator with a wide range of duty cycles. The period of a biased ring oscillator, however, depends on α [see (7)] and varies with the bias current. Thus, α is constrained by the minimum and maximum period $T_0 < P_{\text{min}} \le P_{\text{bias}} \le P_{\text{max}}$

$$\frac{T_0}{P_{\text{max}} - T_0} \le \alpha \le \frac{T_0}{P_{\text{min}} - T_0}. \tag{8}$$

Note that the frequency of the switching signal generated at the output of the ring oscillator changes while varying the duty cycle of the signal. An improved version of the aforementioned ring oscillator with two header circuits is proposed in the following section to maintain a constant frequency under varying duty cycle ratios.

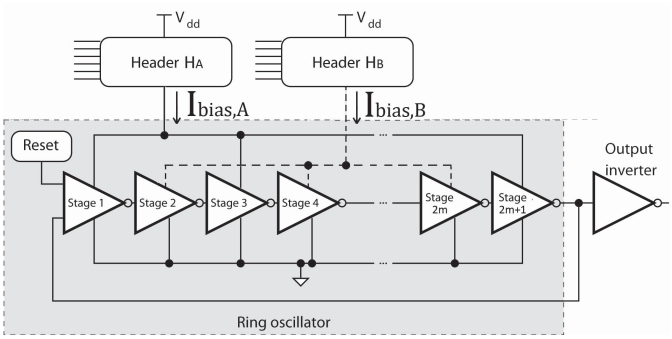


Fig. 7. Ring oscillator with current controlled P_{odd} and P_{even} transistors.

D. Ring Oscillator Topology for Pulse Width Modulation With Constant Frequency

The duty cycle of a switching signal can be controlled by changing the current to the odd (or even) stages of a conventional ring oscillator, as demonstrated in Section II-C. The period of the switching signal in the proposed topology, however, scales with the duty cycle (7), affecting the operational frequency of the ring oscillator. To provide a wide range of duty cycle while maintaining a constant frequency, an additional level of control over the timing parameters of the ring oscillator is required.

Consider a ring oscillator with $2m+1$ stages and two headers H_A and H_B that supply, respectively, the current $I_{\text{bias},A} = \alpha I_{\text{ave}}$ to the $m+1$ P_{odd} transistors and $I_{\text{bias},B} = \beta I_{\text{ave}}$ to the m P_{even} transistors, as shown in Fig. 7.

The current flowing through the P_{odd} and P_{even} transistors affect, respectively, the operating speed of the N_{even} and N_{odd} transistors, as described in Section II-C. Alternatively, the P_{odd} and N_{even} transistors are active during the first pass through the ring oscillator independent of the P_{even} and N_{odd} transistors that are active during the second pass. Thus, the timing parameters of the ring oscillator shown in Fig. 7 are similar to the parameters used in Section II-C, yielding the duty cycle of the ring oscillator

$$D_{\text{bias}} = \frac{1/\alpha}{1/\alpha + 1/\beta} = \frac{1}{1+\alpha/\beta} \tag{9}$$

and period

$$P_{\text{bias}} = T_0(1/\alpha + 1/\beta). \tag{10}$$

To maintain a constant period, the constraint $P^{(2)}_{\text{bias}} = 2T_0$ is used in (10), yielding $\beta = \alpha/(2\alpha - 1)$ and therefore

$$D_{\text{bias}}\,(P = 2T_0) = \frac{1}{2\alpha}. \tag{11}$$

Substituting the period, (10), and duty cycle, (11), of the controlled ring oscillator in Fig. 7, and the half period of a

conventional ring oscillator with a 50% duty cycle, (3), the expressions for the currents $I_{\text{bias},A}$ and $I_{\text{bias},B}$ shown in Fig. 7 are, respectively

$$I_{\text{bias},A} = \frac{I_{\text{ave}}}{2D} \tag{12}$$

$$I_{\text{bias},B} = I_{\text{bias},A} \cdot \frac{D}{1-D} = I_{\text{ave}} \cdot \frac{1}{2(1-D)}. \tag{13}$$

Thus, to design a switching signal with a specific duty cycle D and period P, the proposed ring oscillator topology shown in Fig. 7 should be used with the bias currents $I_{\text{bias},A}$ and $I_{\text{bias},B}$ described by, respectively, (12) and (13). The currents $I_{\text{bias},A}$ and $I_{\text{bias},B}$ are generated independently, and produce a variation insensitive duty cycle and frequency with properly compensated currents. A constant duty cycle under PVT variations is therefore a useful indicator for PVT mitigation in the proposed PWM.

III. Simulation Results

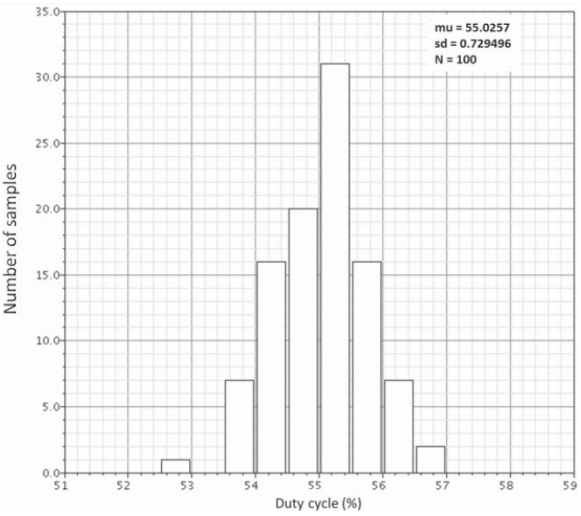
A seven stage ring oscillator is described in this paper to provide a switching signal with a wide duty cycle range. The proposed circuit is designed in a 22-nm CMOS predictive technology model (PTM) [13]. Certain parameters in the technology model file are modified based on [14] to include process corners such as typical-typical (TT), slow-slow (SS), fast-fast (FF), fast-slow (FS), and slow-fast (SF). Simulation results characterizing the accuracy of the proposed PWM are shown in Section III-A for different duty cycle ratios under PVT variations. The effect of the bias current on the duty cycle of the ring oscillator output is discussed in Section III-B without constraints on the period of the output signal and in Section III-C under a constant period constraint.

A. Proposed PWM Under PVT Variations

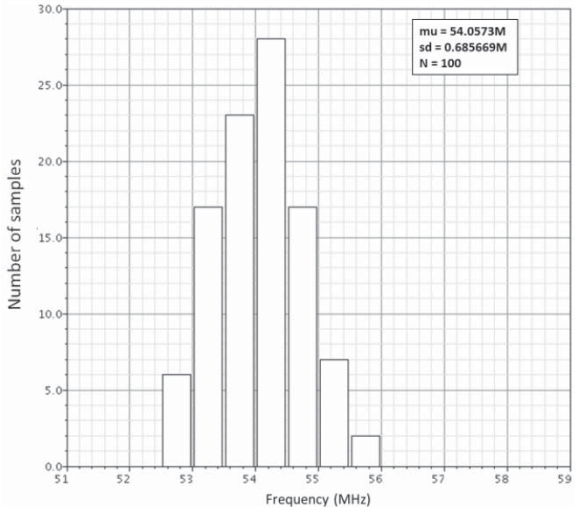
To evaluate the effect of PVT variations on the proposed PWM, the current flowing through the P_{odd} transistors in the first, third, fifth, and seventh stages is controlled by the header circuit, as shown in Fig. 6 for $m = 3$. The remaining pMOS and nMOS transistors in this section are conventionally connected directly to, respectively, V_{dd} and ground. The supply voltage varies $\pm 5\%$ from the nominal 0.95 V and the temperature varies from 27 °C to 80 °C. The simulations have been performed for TT, SS, FF, FS, and SF process corners. The per cent deviation for different duty cycle ratios is listed in Table II. The deviation of the duty cycle under PVT variations is less than 2.7% of the targeted duty cycle.

The Monte Carlo simulations that consider process and mismatch variations are shown in Fig. 8 for a duty cycle of 55% and frequency of 55 MHz, yielding a standard deviation of, respectively, 0.73% and 0.69 MHz.

Transistors with smaller dimensions are more sensitive to PVT variations [15], [16] and exhibit greater leakage current variations [12] than the wider transistors. The narrower transistors within the header circuitry turn on if a switching signal with a greater duty cycle is required. The effect of PVT variations is therefore more prominent on those signals with a wider duty cycle. This trend can be observed in Table II, where the deviation for signals with a 50% duty cycle is smaller than for those signals with a 90% duty cycle.



(a)



(b)

Fig. 8. Monte Carlo simulation. (a) Duty cycle. (b) Frequency distribution.

B. Duty Cycle Controlled PWM

The accuracy of the analytic expressions of the duty cycle presented in Section II-C is evaluated in this section for a wide 25% to 90% range of duty cycle. The circuit shown in Fig. 6 is used with an ideal current source replacing the header. The current I_{bias} flowing through the P_{odd} transistors is therefore controlled by an ideal current source. The rise time at the output of the P_{odd} transistors degrades with a longer charge time, increasing the duty cycle of the switching signal at the output of the ring oscillator.

The expressions for the duty cycle in (6) are verified with simulations for bias currents between 2 and 50 μA, as shown in Fig. 9. Note the good agreement between the theoretical and simulation results (error $< 4.4\%$).

When the current through the controlled stages is neither starved nor enhanced, the simulated circuit oscillates

TABLE II

CHANGE IN THE DUTY CYCLE OF THE PROPOSED PWM UNDER PVT VARIATIONS FOR THE 22-nm PREDICTIVE CMOS MODEL [13]. NOTE THAT THE CORNERS (TT, FF, SS, FS, AND SF) HAVE BEEN GENERATED BY MODIFYING THE RELATED PARAMETERS IN THE MODEL FILES [14]

V_{dd}	Process	Temperature	Duty cycle (55%)	Duty cycle (65%)	Duty cycle (75%)	Duty cycle (85%)
1.0	TT	27	55.03	64.79	74.58	85.79
1.0	TT	80	55.13	65.00	74.02	85.08
1.0	FF	27	55.01	64.86	74.67	85.83
1.0	FF	80	55.29	65.36	74.01	84.08
1.0	SS	27	55.17	65.01	74.87	85.75
1.0	SS	80	55.15	64.88	74.57	85.07
1.0	FS	27	55.15	65.34	75.60	87.06
1.0	FS	80	55.23	65.49	75.71	86.64
1.0	SF	27	55.51	65.37	74.52	84.36
1.0	SF	80	55.51	65.25	74.01	82.85
0.9	TT	27	55.10	65.00	74.77	86.02
0.9	TT	80	55.09	64.92	74.58	85.76
0.9	FF	27	55.00	64.90	74.66	86.28
0.9	FF	80	55.10	65.06	74.74	85.57
0.9	SS	27	55.30	65.34	75.21	86.08
0.9	SS	80	55.21	65.03	74.73	85.44
0.9	FS	27	55.26	65.81	76.18	87.40
0.9	FS	80	55.25	65.68	75.97	87.16
0.9	SF	27	55.61	65.40	74.38	84.26
0.9	SF	80	55.49	65.07	73.88	83.54
Maximum variations [%]			± 0.55	± 0.78	± 1.53	± 2.68

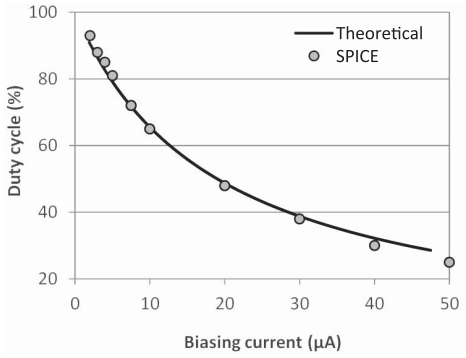


Fig. 9. Duty cycle varies between 25% and 90% when the header current changes from 50 to 2 μA (error $< 4.4\%$).

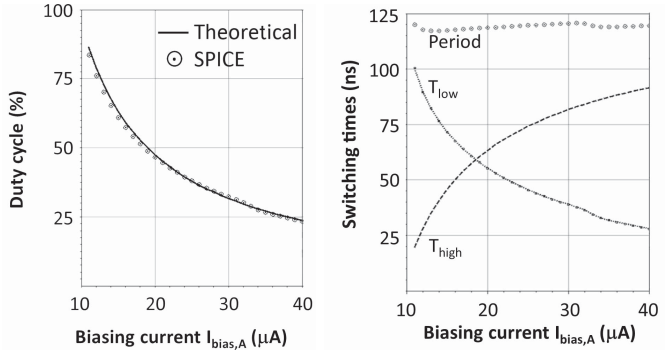


Fig. 10. Header current $I_{\text{bias},A}$ changes from 40 to 11 μA. (a) Duty cycle varies between 25% and 90% (error $< 3.1\%$). (b) Period remains approximately constant (error $< 1.25\%$).

with a 50% duty cycle, yielding $\alpha = 1$, where $I_{\text{bias}} = I_{\text{ave}} = 19$ μA. Using the analytic expression in (6), the duty cycle can be tuned with a digitally programmable control block.

C. Duty Cycle and Frequency Controlled PWM

The accuracy of the analytic expressions for the duty cycle under the constant frequency constraint (see Section II-D) is evaluated in this section at 8.33 MHz for a wide 25% to 90% range of duty cycle. The current supply to the ring oscillator is controlled with two headers, exhibiting a frequency of 8.33 MHz ± 1.25% for all the values of duty cycle. The circuit shown in Fig. 7 is modeled by ideal current sources replacing the headers H_A and H_B. The currents $I_{\text{bias},A}$ and $I_{\text{bias},B}$ flowing, respectively, through the P_{odd} and P_{even} transistors are assumed to be controlled by ideal current sources. Intuitively, the rise time at the output node of the P_{odd} transistors increases with a longer charge time, increasing the duty cycle of the switching signal. To mitigate the effect of the longer $T_{\text{bias,high}}$ delay on the period of the switching signal, the rise time at the output of the P_{even} transistors, based on (13), is decreased. The analytic expression for the duty cycle and period, respectively, (10) and (11), are verified by the simulation for $I_{\text{bias},A}$ currents between 11 and 40 μA, as shown in Fig. 10. Note the good agreement between the theoretical and simulation results (error $< 3.1\%$).

IV. CONCLUSIONS

A digitally controlled PWM with a wide pulse width range of 25% to 90% is proposed in this paper. An enhanced header circuit is proposed to provide a greater range of header current. The proposed header circuit is connected to every other stage of the ring oscillator to significantly improve the dynamic range of the pulse width. The parallel configuration of the M_3 transistors within the header circuit is used to control the duty cycle with high granularity. To efficiently control

both the duty cycle and the period of the switching signal, a more advanced version of the PWM is also proposed. Every other stage in this topology is controlled by a header circuit. An additional header circuit, however, is connected to the remaining ring oscillator stages to provide enhanced control over the frequency of the switching signal. A DC2V converter samples the duty cycle of the output signal and generates an analog voltage to control the header current. The PVT variations are compensated by the feedback loop generated by the DC2V converter. Under PVT variations, deviations in the pulse width are less than 2.7% of the switching signal period. Both the duty cycle and the period of the proposed circuit are analytically determined as a function of the header current, simplifying the control over the PWM timing parameters. The accuracy of the duty cycle analytic expressions is evaluated with simulation results, yielding less than 3.1% and 4.4% error, respectively, with and without the controlled frequency for the PWM. A constant frequency with less than 1.25% variation is reported for different values of the duty cycle. The proposed pulse width modulator provides means for dynamically changing the voltage in adaptive systems using fast control circuitry, providing high accuracy under PVT variations and dynamic duty cycle and period control.

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