Noise Coupling Models in Heterogeneous 3-D ICs

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***Abstract*— Models of coupling noise from an aggressor module to a victim module by way of through silicon vias (TSVs) within heterogeneous 3-D integrated circuits (ICs) are presented in this paper. Existing TSV models are enhanced for different substrate materials within heterogeneous 3-D ICs. Each model is adapted to each substrate material according to the local noise coupling characteristics. The 3-D noise coupling system is evaluated for isolation efficiency over frequencies of up to 100 GHz. Isolation improvement techniques, such as reducing the ground network inductance and increasing the distance between the aggressor and victim modules, are quantified in terms of noise improvements. A maximum improvement of 73.5 dB for different ground network impedances and a difference of 38.5 dB in isolation efficiency for greater separation between the aggressor and victim modules are demonstrated. Compact, accurate, and computationally efficient models are extracted from the transfer function for each of the heterogeneous substrate materials. The reduced transfer functions are used to explore different manufacturing and design parameters to evaluate coupling noise across multiple 3-D planes.**

***Index Terms*— 3-D integrated circuit (IC), heterogeneous 3-D system, noise coupling, substrate coupling, through silicon via (TSV) noise coupling model.**

I. Introduction

NOISE coupling is of increasing importance within the integrated circuits (ICs) community [1]–[6]. This issue is of fundamental concern in 3-D circuits, where signals are distributed among multiple different layers using through silicon vias (TSVs), creating an *electronic storm* within the 3-D system. Different types of signals (power, clock, and data) can propagate within these vertical interconnects. Different TSV processes are used in 3-D integration, including via-first, via-middle, and via-last [7]. In each of these processes, the TSV penetrates the substrate of a layer and connects to either the first or last metal within that layer. TSVs, a seminal component of 3-D technology, are short vertical interconnections (e.g., 20 μm in length and 2 μm in diameter [8]) between the different layers that can alleviate global signaling issues [9]. The TSVs, however, also pose novel obstacles. In particular, the noise is coupled through the TSV into the substrate of each layer. This noise propagates through the substrate and affects the victim circuits surrounding a TSV.

Manuscript received May 7, 2015; revised September 9, 2015, November 30, 2015, and February 10, 2016; accepted February 18, 2016. Date of publication March 15, 2016; date of current version July 22, 2016. This work was supported in part by the Binational Science Foundation under Grant 2012139, in part by the National Science Foundation under Grant CCF-1329374, in part by the Intelligence Advanced Research Projects Activity under Grant W911NF-14-C-0089, and in part by Grants from Cisco Systems and Intel. The associate editor coordinating the review of this manuscript and approving it for publication was Prof. Ibrahim M. Elfadel.

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Digital Object Identifier 10.1109/TVLSI.2016.2535370

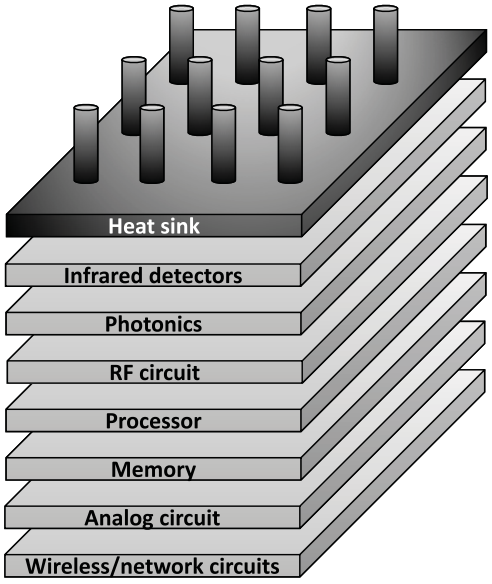

Fig. 1. Heterogeneous 3-D IC.

TABLE I
COMMON CIRCUITS AND COMPATIBLE SUBSTRATE TYPES

Circuits	Substrate materials	Electrical resistivity $\Omega \cdot$ cm	Thermal conductivity $\frac{W}{m^\circ C}$
Processor/ memory	Silicon (Si)	1 to 10	138
RF/analog	Gallium Arsenide (GaAs)	$4 \cdot 10^7$	40
Photonics	Germanium (Ge)	$1 \cdot 10^{-3}$	45
Space applications/ detectors	Mercury Cadmium Telluride (HgCdTe)	2	0.2

Modern applications employ diverse functionalities. Mobile devices are capable of sensing light, capturing images and videos, high-performance processing, storing large amounts of data, and much more. A 3-D structure is an effective platform for integrating these heterogeneous circuits within a single system, as shown in Fig. 1. Each layer of a 3-D IC is typically independently optimized and often designed using different substrate materials for different applications. Common circuits and compatible substrate materials are listed in Table I. The electrical resistivity and the thermal conductivity of each substrate material are also listed. Some commonly used materials in modern ICs are silicon (Si), gallium arsenide (GaAs), germanium (Ge), and mercury cadmium (MerCad)

TABLE II
COMPARISON OF LUMPED, DISTRIBUTED, AND SHORT-CIRCUIT MODELS FOR Si, GaAs, AND Ge SUBSTRATES FOR DIFFERENT VALUES OF INDUCTANCE OF THE GROUND NETWORK

Model	Ground inductance nH	Si		GaAs		Ge	
		Peak noise mV	Settling time nsec	Peak noise mV	Settling time nsec	Peak noise mV	Settling time nsec
Short circuit	0.1	-	-	-	-	11.1	0
	1	-	-	-	-	645.5	1.46
	10	-	-	-	-	954.4	8
Lumped	0.1	159.8	1.57	$3.8 \cdot 10^{-8}$	0	8.5	0
	1	162.4		$3.8 \cdot 10^{-8}$		638.5	1
	10	186.3		$3.8 \cdot 10^{-8}$		950.8	6
Distributed (3 sections)	0.1	161.8	1.55	$3.9 \cdot 10^{-8}$	0	8.7	0
	1	164.5		$3.9 \cdot 10^{-8}$		637.5	1
	10	188.6		$3.9 \cdot 10^{-8}$		950.1	6

telluride (HgCdTe) [10]–[12]. Noise coupling from the TSVs into the victim layers for these common substrates is discussed here. Previous work has addressed noise coupling from TSVs into the substrate in homogeneous circuits (processor/memory stacks), typically on a silicon substrate [13], [14]. The purpose of this paper is to provide noise coupling models for heterogeneous 3-D systems composed of different substrate materials.

It is suggested here to change the acronym TSV from TSV to through-substrate-via, since the substrate penetrated by the vertical interconnect in a heterogeneous 3-D system can be composed of different types of materials. A similar example is the acronym MOS that stands for metal–oxide–semiconductor and not for metal–oxide–silicon.

The rest of this paper is organized as follows. Through-substrate-via models are proposed in Section II. A frequency analysis of the isolation efficiency and isolation improvement techniques, as well as extraction of the transfer function of the noise coupling system, are discussed in Section III. Design methods to lower coupling noise between layers are provided in Section IV. Finally, some conclusions are drawn in Section V.

II. THROUGH-SUBSTRATE-VIA MODELS

Existing models for noise coupling from TSVs to victim circuits in 3-D ICs [13]–[15] have to date only addressed homogeneous systems. In these models, the layers are exclusively silicon, including dual-well bulk CMOS and partially depleted silicon-on-insulator [14]. The noise coupling model proposed in [13] is shown in Fig. 2(a). A distributed RC model composed of four sections is used to characterize the TSV impedance and capacitive coupling into the silicon substrate. The substrate is modeled using distributed lateral and vertical resistors. The ground network is modeled as a resistive–inductive impedance [16].

Silicon is the most common substrate material for ICs and is used for many applications. The model shown in Fig. 2(a) suggests the use of a distributed model for the RC impedances. The resistance of a TSV, based on the following expression [13], is

$$R_{\text{tsv}} = \frac{1}{N_{\text{tsv}}} \cdot \frac{\rho_c D}{\pi (W/2)^2}. \tag{1}$$

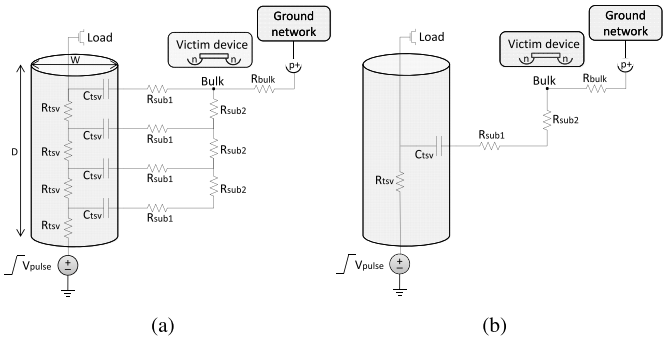

Fig. 2. Noise coupling from a TSV to a victim through a silicon substrate as (a) previously proposed in [13], and (b) proposed in this paper.

The number of distributed sections of the TSV is N_{tsv}, the resistivity of the conductive material within the TSV is ρ_c, and the depth (length) and the diameter of the TSV are D and W, respectively. With a copper resistivity of 2.8 $\mu\Omega \cdot$ cm [17], a depth of 20 μm, and a diameter of 2 μm [8], a resistance of 0.18 Ω for $(1/N_{\text{tsv}}) = 1$ is produced. This resistance is relatively small as compared with the resistance of a typical digital buffer [18]. It is proposed, therefore, to use a lumped RC model for the TSV [1], [19], as shown in Fig. 2(b). Another important aspect is the model of the ground network. The victim device is commonly connected to the ground network through the bulk contact; the inductive behavior of this network, therefore, also has to be considered.

A comparison of a lumped model versus a distributed model with three sections is listed in Table II for Si, GaAs, and Ge. For Ge, a third short-circuit model [shown in Fig. 3(a)] is also compared. This model completely omits the resistors of the substrate, since the resistance of the substrate is negligible and the model, therefore, only exhibits a coupling capacitance from the TSV to the substrate [19]. The models have been evaluated using SPICE. A 10-ps input ramp from 0 to 1 V (Vpulse) is applied to simulate switching the aggressive digital circuits. The voltage is evaluated at the victim device node. Both the peak noise voltage and the settling time (2% of the final value) have been recorded for three different inductance values of the ground network. Note that unlike coupling between adjacent interconnects where the analysis of the propagating waves is required [6], in this paper, coupling from a signal propagating

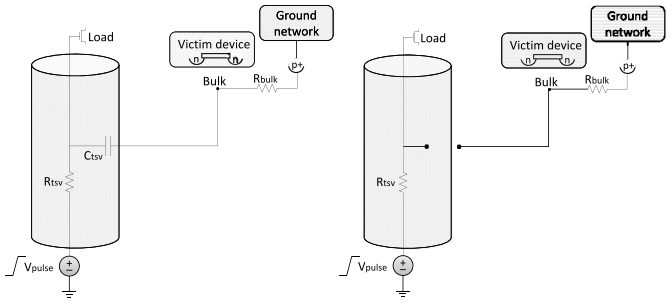

Fig. 3. Noise coupling from a TSV to a victim through (a) short-circuit Ge substrate model, and (b) open-circuit GaAs substrate model.

within an aggressor TSV to the substrate is described. The peak noise and settling time are, therefore, sufficient metrics for evaluating coupling noise in transient analysis.

The error of the lumped model as compared with the distributed model for Si is 1.2%. A lumped model can, therefore, be used to accurately characterize a silicon substrate. As observed from the results listed in Table II, the inductance of the ground network can significantly affect the peak noise voltage. In the worst case (from 0.1 to 10 nH), a difference of 26.5 mV (14.2%) is noted.

The peak noise voltage for both lumped and distributed models for GaAs is in the range of picovolts and is, therefore, negligible in most applications. The proposed model in this case is an open-circuit model that ignores the capacitive coupling, as shown in Fig. 3(b). It is also observed from Table II that the inductance of the ground network has no effect on the peak noise voltage. This behavior is due to the resistivity of the substrate, which is sufficiently large to shunt the inductance of the ground network.

The accuracy of the short-circuit, lumped, and distributed models is shown in Table II. Ge is highly dependent on the inductance of the ground network. Comparing the lumped and distributed models, a distributed model provides negligible accuracy improvement as compared with a lumped model. The worst case difference in the peak noise voltage is 0.2 mV (2.3%), while the settling time is similar. The lump model that incorporates fewer nodes is, therefore, preferable. The short-circuit model deviates from the lump model by 2.6 mV (23.4%) and 2 ns (25%) for, respectively, the peak noise voltage and settling time. A lump model, similar to the model for silicon [shown in Fig. 2(b)], should, therefore, be used. If the circuit specifications are not particularly strict (a higher peak noise voltage and longer settling times are allowed), a short-circuit model can be used to reduce the computational effort.

MerCad telluride is commonly used as a detector material for infrared arrays in space-related applications [20]. The electrical resistivity of this material is similar to silicon. The same model, as shown in Fig. 2(b), can, therefore, be used in the noise coupling analysis process.

III. Analysis of Frequency Response

A technology specific analysis of the frequency response of the lump noise coupling model is offered in this section. The analysis is limited to frequencies of up to 100 GHz to maintain a near field coupling mode. Noise isolation improvement techniques are also suggested. The model is simulated in SPICE, and the transfer function of the system is extracted based on the characteristics of each substrate material. In Section IV, the extracted transfer functions are simulated in MATLAB and compared with SPICE. Note that due to similar electrical properties of HgCdTe and Si, only Si, GaAs, and Ge as the substrate materials are considered.

A. Isolation Efficiency of Noise Coupled System

Isolation efficiency is the magnitude of the signal observed at the victim for a 1 V aggressor signal (in decibel). The isolation efficiency of a noise coupled system for different substrate materials and ground network inductances is shown in Fig. 4. The results shown in Fig. 4 are obtained from the SPICE simulations. The isolation efficiency of Ge is strongly dependent on frequency, followed by Si, and GaAs exhibits almost no dependence on frequency due to the high resistivity of the substrate. Although Ge is strongly dependent on frequency for a wide range of frequencies (up to approximately 10 GHz), the isolation efficiency of Ge is higher than GaAs. The frequency dependent components of the Ge system lower the coupled noise at the victim. As shown in Fig. 4(c), GaAs is independent of the inductance of the ground network. The effect of the inductance of the ground network on Si and Ge is discussed later in this section.

For Ge circuits, the resonant frequency is within a practical range of frequencies. To avoid high coupling noise for these circuits, special techniques to improve noise isolation should be considered. For Si circuits, the isolation techniques are highly dependent on the operational frequency of the circuit and noise toleration specifications. For a typical frequency range of signal transitions in digital CMOS circuits (under 10 GHz), the isolation efficiency is high. For those circuits that require fast transitions with strict noise tolerance specifications, isolation enhancement methods should be considered. For GaAs, the isolation efficiency is -15.9 dB. Isolation techniques that operate independent of frequency should be applied to further improve noise isolation.

B. Techniques to Improve Noise Isolation

Several techniques are offered here to improve noise isolation in heterogeneous 3-D circuits.

1) Ground Network Inductance: The tradeoff between thinner and more resistive, and thicker and more inductive metal interconnect should be considered when considering power distribution networks in ICs. In 3-D ICs, identifying the inductive return paths is more complicated as compared with 2-D circuits, since these paths can span the entire 3-D structure. Special emphasis should, therefore, be placed on low inductance ground lines. As shown in Fig. 4, low inductance ground networks directly improve the isolation efficiency of the coupled noise system for both Si and Ge. For Ge, low inductive ground networks are particularly important. The worst case difference in isolation efficiency for an inductive ground network is 73.5 dB. For a ground network with an

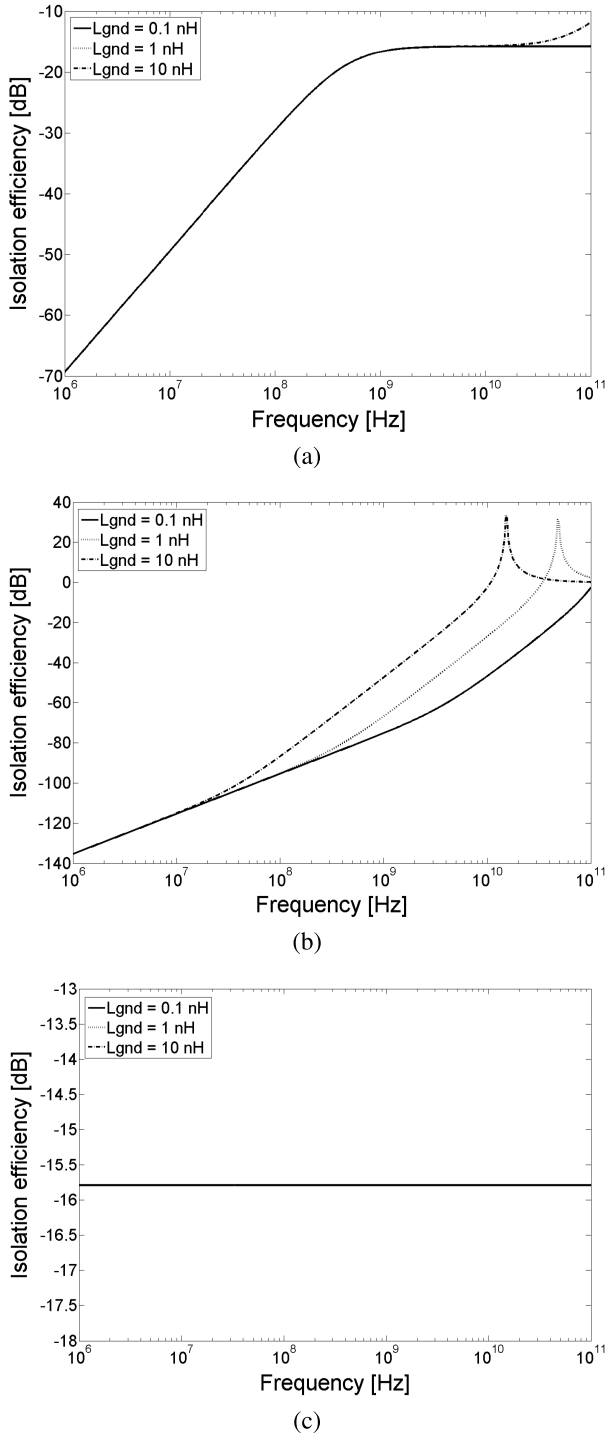

Fig. 4. Isolation efficiency of a noise coupled system for (a) silicon, (b) germanium, and (c) gallium arsenide substrate materials.

inductance of 10 nH, the resonance frequency is 15.1 GHz, while for an inductance of 0.1 nH, the resonance frequency is above the practical range of frequencies (>100 GHz). The resonance frequency $f_{\text{res}} = (1/2\pi(LC)^{1/2})$, where the capacitance of the system is C and the inductance of the ground network is L. As shown in Fig. 4(b), a lower ground network inductance can shift the resonance frequency out of the practical range of frequencies.

To further validate this technique, a tradeoff between inductance and resistance is considered for each

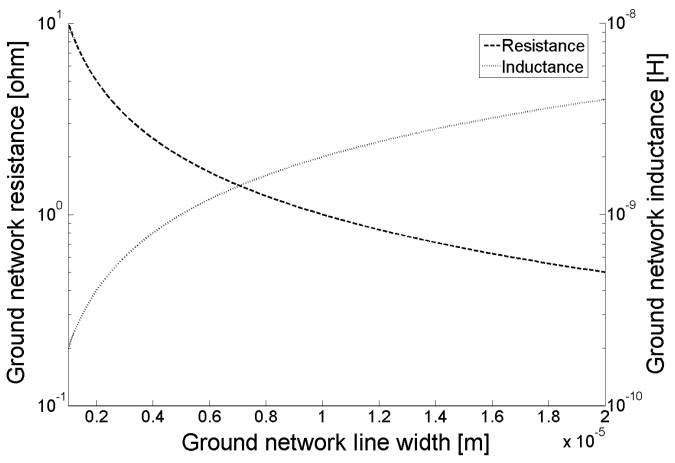

Fig. 5. Resistance and inductance versus linewidth of ground network. The ground network is copper.

substrate material. The resistance and inductance as a function of the linewidth of the ground network are extracted according to [21] and shown in Fig. 5.

SPICE simulations of the isolation efficiency for each of the substrate materials are shown in Fig. 6. For a Si substrate, the results indicate that within the practical range of frequencies (below 100 GHz), the linewidth has no effect on the ground network inductance, and therefore, a minimum linewidth should be used. For Ge, a tradeoff exists between the resistance and inductance of the ground network. For wide lines, the peak isolation efficiency is lower than for narrow lines. The worst case difference between a linewidth of 2 and 20 μm is 8.2 dB. For frequencies below 56 GHz, the isolation efficiency of a narrow line (2 μm) is better than a wide line (20 μm). The linewidth of the ground network should, therefore, be chosen according to the transition frequency of the signals. For GaAs, the isolation efficiency is independent of the linewidth. The smallest allowable width should, therefore, be used.

2) Distance Between Aggressor and Victim Circuit: This dimension is measured from the aggressor module A on layer m to the victim module V on layer n, as shown in Fig. 7. The depth (length) of a single TSV and the horizontal distance (on layer n) from the TSV to the victim circuit are, respectively, D and l. The distance between modules A and V is therefore

$$d_{\text{AV}} = \sqrt{(D \cdot |\text{m} - \text{n}|)^2 + l^2}. \quad (2)$$

The effect of d_{AV} on the isolation efficiency of Ge, evaluated using the Ge model in SPICE, is shown in Fig. 8. Substrate thicknesses, ranging from 20 to 60 μm, have been evaluated to determine the effect of different manufacturing processes of heterogeneous substrate materials. Similarly, lateral distances, ranging from 10 to 1,000 μm, have been evaluated. An improvement of 38.5 dB in isolation efficiency is demonstrated for $d_{\text{AV}} = 1,000.2$ μm as compared with the case of $d_{\text{AV}} = 60.8$ μm. Placing the victim circuits farther from those TSVs carrying aggressor signals significantly improves the noise isolation characteristics. Alternatively, a thicker

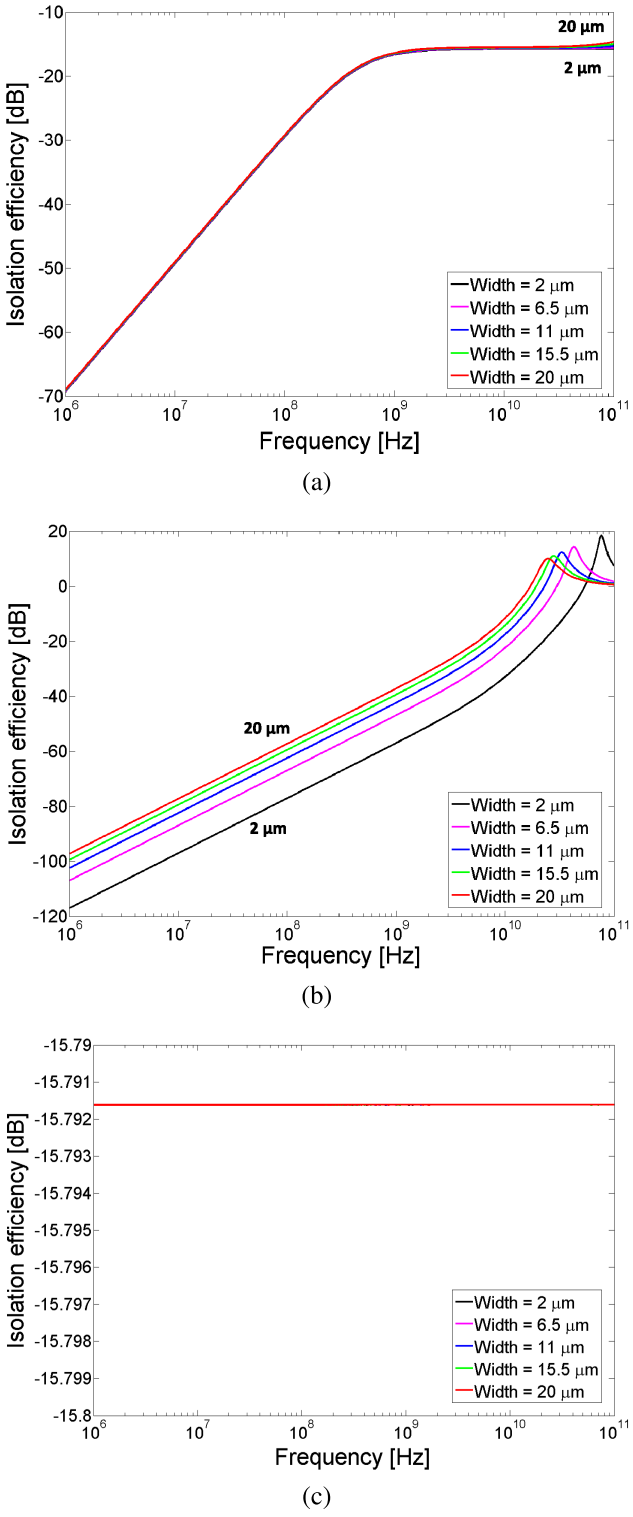

Fig. 6. Isolation efficiency of a noise coupled system as a function of linewidth of the ground network for (a) silicon, (b) germanium, and (c) gallium arsenide substrate materials.

substrate or a larger number of layers between the aggressor and victim modules only slightly improves the isolation efficiency due to the low impedance of the TSVs.

C. Transfer Function of Noise Coupled System

To better evaluate the noise coupling mechanism, a heterogeneous system is represented as a transfer function.

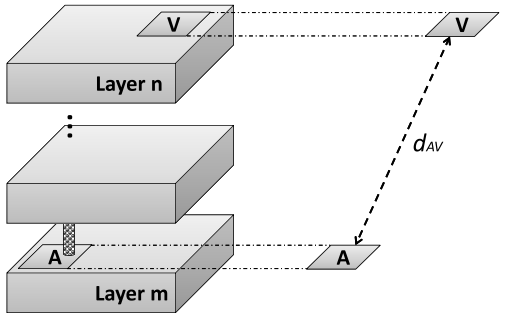

Fig. 7. Distance from aggressor module A on layer m to victim module B on layer n.

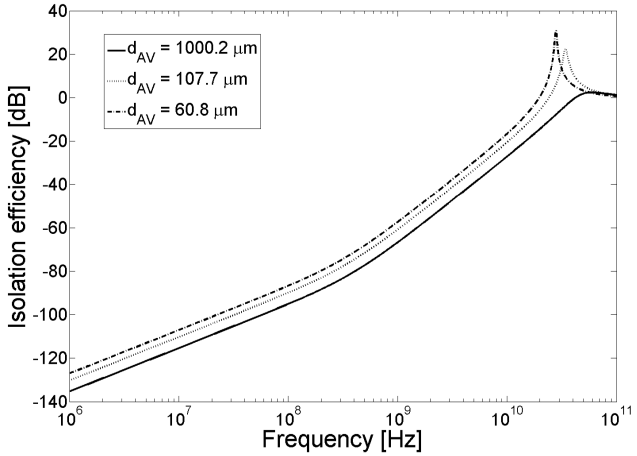

Fig. 8. Effect of distance between the aggressor and the victim on the isolation efficiency for a Ge substrate. The resonant frequency is observed at the peak isolation efficiency due to the increasing reactance of the ground network.

This system consists of an input (aggressor signal) and output (signal at victim module). The isolation efficiency of the system [13], [22] is determined, and the noise mitigation techniques are offered. The small signal equivalent circuit of the noise coupled system is shown in Fig. 9. The following relations are used.

1) *Substrate Impedance:* $R_{\text{sub}} \equiv R_{\text{sub1}} + R_{\text{sub2}}$.
2) *TSV Coupling Reactance:* $X_{C_{\text{tsv}}} \equiv (1/\omega C_{\text{tsv}})$.
3) *TSV Coupling Impedance:* $Z_{C_{\text{tsv}}} \equiv -j \cdot X_{C_{\text{tsv}}}$.
4) *Ground Network Reactance:* $X_{\text{gnd}} \equiv \omega L_{\text{gnd}}$.
5) *Ground Network Impedance:* $Z_{\text{gnd}} \equiv R_{\text{gnd}} + j \cdot X_{\text{gnd}}$.
6) *Load Reactance:* $X_L \equiv (1/\omega C_L)$.
7) *Load Impedance:* $Z_L \equiv -j \cdot X_L$.

The transfer function is analyzed in this section for a heterogeneous system according to the substrate materials discussed in Section II. The transfer function of the lumped model is

$$H(\omega) = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{(R_{\text{bulk}} + Z_{\text{gnd}})Z_L}{(R_{\text{tsv}} + Z_L)(R_{\text{sub}} + R_{\text{bulk}} + Z_{C_{\text{tsv}}} + Z_{\text{gnd}}) + R_{\text{tsv}} \cdot Z_L}. \quad (3)$$

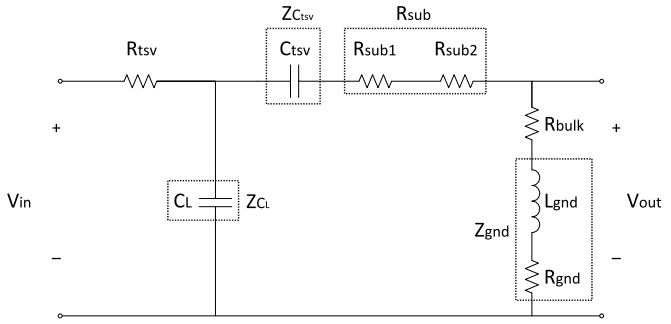

Fig. 9. Equivalent small signal model of a noise coupled system.

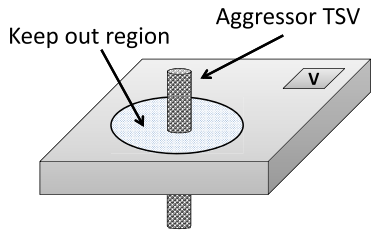

Fig. 10. Keep out region around an aggressor TSV. The victim modules (V) should be placed outside this region.

Reducing the transfer function can produce a simpler model requiring less computational effort. The simulated load capacitance (100 fF) is relatively small. The model can, therefore, be treated as an open circuit assuming a small signal model (Fig. 9) within a practical range of frequencies (1 MHz–100 GHz). The transfer function $H(\omega)$ is

$$H(\omega) = \frac{R_{\text{bulk}} + Z_{\text{gnd}}}{R_{\text{sub}} + R_{\text{bulk}} + Z_{C_{\text{tsv}}} + Z_{\text{gnd}} + R_{\text{tsv}}}. \tag{4}$$

Further reductions of (4) are dependent on the substrate material for a specific layer.

1) Si Substrate: The substrate and bulk resistances in Si and HgCdTe are three to five orders of magnitude larger than the TSV and ground network resistances ($R_{\text{sub}}, R_{\text{bulk}} \gg R_{\text{tsv}}, R_{\text{gnd}}$) for l as low as 10 μm. Therefore, (4) reduces to

$$H(\omega) = \frac{R_{\text{bulk}} + j \cdot X_{\text{gnd}}}{R_{\text{sub}} + R_{\text{bulk}} + j(X_{\text{gnd}} - X_{C_{\text{tsv}}})}. \tag{5}$$

2) Ge Substrate: For Ge, the substrate and bulk impedances are of the same relative magnitude as the other components of the transfer function; therefore, (4) cannot be further reduced. The transfer function for Ge is therefore

$$H(\omega) = \frac{R_{\text{bulk}} + Z_{\text{gnd}}}{R_{\text{sub}} + R_{\text{bulk}} + Z_{C_{\text{tsv}}} + Z_{\text{gnd}} + R_{\text{tsv}}}. \tag{6}$$

3) GaAs Substrate: The substrate and bulk resistances in GaAs are significantly larger (approximately six orders of magnitude) than all other components of the noise coupled system. The transfer function, therefore, reduces to

$$H(\omega) = \frac{R_{\text{bulk}}}{R_{\text{sub}} + R_{\text{bulk}}}. \tag{7}$$

Substituting the substrate and bulk parameters and worst case distance from the aggressor TSV to the victim ($l = 10$ μm) leads to $H(\omega) \approx 0.16$. In units of decibel, $20\log H(\omega) \approx -15.9$ dB, which corresponds to the isolation efficiency for GaAs, as shown in Fig. 4(c).

IV. Design Considerations

After obtaining the reduced transfer function of the system for each substrate type, some design considerations for decreasing the coupling noise are offered in this section. The objective is to minimize $|H(\omega)|$ by adjusting different manufacturing and design parameters and to lower the noise coupled from the aggressor to the victim.

An example of a design parameter that greatly affects $|H(\omega)|$ is the horizontal distance from an aggressor TSV to a victim module l. A keep out region (shown in Fig. 10) is a circular area around an aggressor TSV, in which a victim should not be placed to achieve noise coupling lower than $N_{\max}$ (maximum allowed noise coupling level in decibel). The radius of the keep out region is l, such that $20\log|H(\omega, l)| < N_{\max}$. The magnitude of the transfer functions in (5)–(7) for Si, Ge, and GaAs are, respectively, (8), (9), and (10), as shown at the bottom of this page, respectively.

Although (8)–(10) are dependent on l, it is difficult to provide a closed-form expression in l. A design space for each of the substrate materials is, therefore, generated according to the

$$|H(\omega, l)| = \left[\left(\frac{R_{\text{bulk}}(R_{\text{sub}}(l) + R_{\text{bulk}}) + X_{\text{gnd}}(X_{\text{gnd}} - X_{C_{\text{tsv}}})}{(R_{\text{sub}}(l) + R_{\text{bulk}})^2 + (X_{\text{gnd}} - X_{C_{\text{tsv}}})^2} \right)^2 + \left(\frac{X_{\text{gnd}}(R_{\text{sub}}(l) + R_{\text{bulk}}) - R_{\text{bulk}}(X_{\text{gnd}} - X_{C_{\text{tsv}}})}{(R_{\text{sub}}(l) + R_{\text{bulk}})^2 + (X_{\text{gnd}} - X_{C_{\text{tsv}}})^2} \right)^2 \right]^{1/2} \tag{8}$$

$$|H(\omega, l)| = \left[\left(\frac{(R_{\text{bulk}} + R_{\text{gnd}})(R_{\text{sub}}(l) + R_{\text{bulk}} + R_{\text{tsv}} + R_{\text{gnd}}) + X_{\text{gnd}}(X_{\text{gnd}} - X_{C_{\text{tsv}}})}{(R_{\text{sub}}(l) + R_{\text{bulk}} + R_{\text{tsv}} + R_{\text{gnd}})^2 + (X_{\text{gnd}} - X_{C_{\text{tsv}}})^2} \right)^2 + \left(\frac{X_{\text{gnd}}(R_{\text{sub}}(l) + R_{\text{bulk}} + R_{\text{tsv}} + R_{\text{gnd}}) - (R_{\text{bulk}} + R_{\text{gnd}})(X_{\text{gnd}} - X_{C_{\text{tsv}}})}{(R_{\text{sub}}(l) + R_{\text{bulk}} + R_{\text{tsv}} + R_{\text{gnd}})^2 + (X_{\text{gnd}} - X_{C_{\text{tsv}}})^2} \right)^2 \right]^{1/2} \tag{9}$$

$$|H(\omega, l)| = \frac{R_{\text{bulk}}}{R_{\text{sub}} + R_{\text{bulk}}} \tag{10}$$

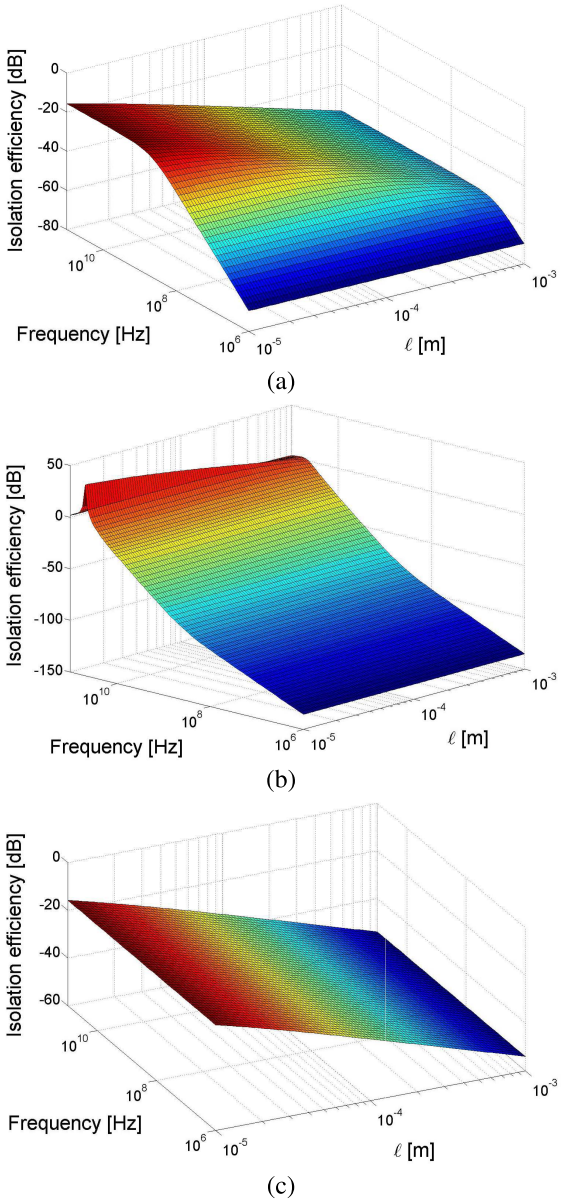

Fig. 11. Isolation efficiency versus frequency and radius of keep out region for (a) Si, (b) Ge, and (c) GaAs substrate materials.

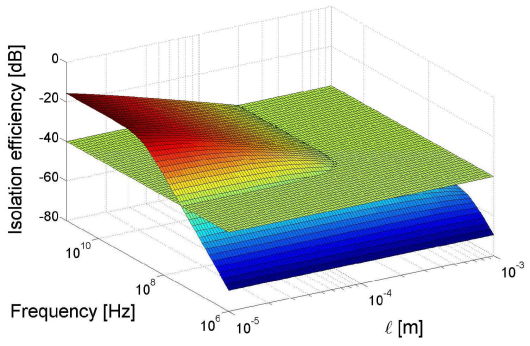

Fig. 12. Keep out region around aggressor TSV for $N_{\max} = -40$ dB. The victim circuits should be placed on the isolation efficiency surface below the base surface.

relevant expression, as shown in Fig. 11. Both the frequency and l are based on the maximum coupling noise ($N_{\max}$). The design space for Si, Ge, and GaAs generated from (8) to (10)

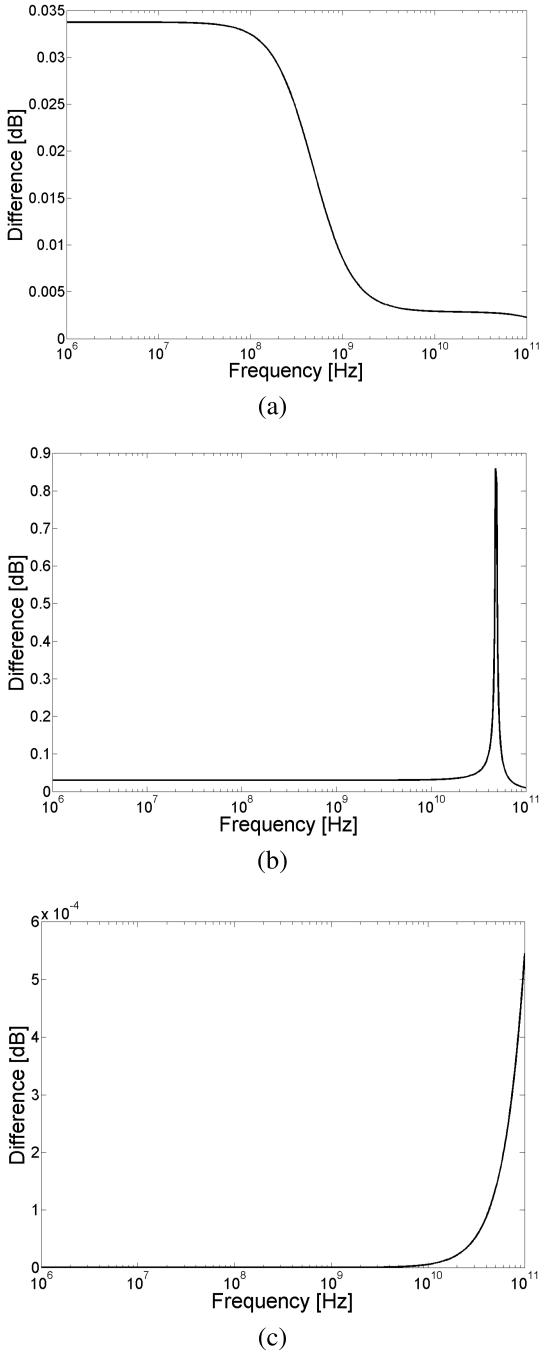

Fig. 13. Comparison between SPICE model and extracted transfer function for (a) Si, (b) Ge, and (c) GaAs substrate materials.

is shown in Fig. 11. Each plot describes the isolation efficiency of the coupled noise system with respect to frequency and l.

As shown in Fig. 11, the noise at the victim is less at low frequencies and increasing l. An increase in l rapidly lowers the noise coupling for both Si and GaAs. Alternatively, in Ge, the dependence of the isolation efficiency on l is weak. This behavior is due to the negligible substrate resistivity, leading to a stronger dependence on the frequency of the noise coupled system. The resonance frequency for Ge is shown in Fig. 11(b). The design space around the resonance frequency should be avoided.

To quantify the keep out region within the design space, a horizontal surface, described here as the base surface, can be added at $N_{\max}$. An example of a Si substrate is shown in Fig. 12. In this case, $N_{\max} = -40$ dB and the keep out region is above the horizontal surface. This surface can be used to determine the minimum distance between the aggressor and the victim to maintain the isolation efficiency below $N_{\max}$ for any frequency within the relevant range. Similar design spaces can be generated based on the transfer function for the other design parameters (e.g., TSV diameter, TSV filling material, impedance of the ground network, and size of victim device).

A comparison between the transfer function and the SPICE simulated model for Si, Ge, and GaAs is shown in Fig. 13. This comparison is obtained by observing the plots in Fig. 11 at $l = 10$ μm and a ground network inductance of 1 nH, the same distance and inductance used in the SPICE analysis. The results show discrepancies smaller than 1 dB for all substrate materials.

V. Conclusions

A complex electronic storm exists within heterogeneous 3-D systems. Models of noise coupling in heterogeneous 3-D ICs are presented in this paper. These models consider the different substrate materials within a heterogeneous 3-D system. A lump model is sufficient for the Si and Ge substrates, with a peak noise voltage error, as compared with a distributed model, of, respectively, 26.5 and 0.2 mV. For Ge, a short-circuit model can be used for less stringent noise constraints. The electrical properties of HgCdTe are similar to silicon; the model used for silicon is, therefore, proposed for this type of substrate. GaAs substrates are highly resistive, efficiently isolating the victim from the aggressor. An open circuit model is, therefore, used for GaAs substrates.

The noise coupled system is represented as a transfer function to evaluate the isolation efficiency characteristics. Minimizing the magnitude of the transfer function, hence, lowering the coupled noise, is the objective. Isolation improvement techniques are offered. The transfer function can be reduced based on material specific parameters. Each reduced transfer function can be utilized to generate a design space for different manufacturing and design parameters. A keep out region, the horizontal distance between an aggressor TSV and a victim, and the maximum coupling noise are evaluated in terms of the relevant design space. The reduced transfer functions are compared with the SPICE models, and good agreement is observed within a practical range of frequencies (up to 100 GHz).

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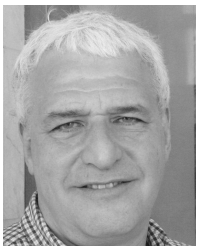

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