Power Efficient Level Shifter for 16 nm FinFET Near Threshold Circuits

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***Abstract*— Since the minimum feature size has shrunk beyond the sub-30-nm node, power density has become the major factor in modern microprocessors. Techniques such as dynamic voltage scaling operating down to near threshold voltage levels and supporting multiple voltage domains have become necessary to reduce dynamic as well as static power. A key component of these techniques is a level shifter that serves different voltage domains. This level shifter must be high speed and power efficient. The proposed level shifter translates voltages ranging from 250 to 790 mV, and exhibits 42% shorter delay, 45% lower energy consumption, and 48% lower static power dissipation. In addition, the proposed level shifter exhibits symmetric rise and fall transition times with up to 12% skew at the extreme conditions over the maximum range of voltages.**

***Index Terms*— CMOS, level shifter, low power, near threshold circuits.**

I. Introduction

Energy efficiency is a primary concern in modern sub-30-nm CMOS microprocessors [1]. A standard method to reduce dynamic power consumption is to lower the supply voltage due to the quadratic dependence of dynamic power on voltage. A negative temperature coefficient has, therefore, become an attractive methodology for sub-30-nm CMOS circuits [2]. This mode of operation is characterized by a balance between speed and power. By operating a circuit near the threshold voltage (as compared with a much lower voltage deep within the subthreshold region), a balanced approach to managing power is achieved while maintaining a reasonable circuit delay. This concept is shown in Fig. 1 [3], [4]. Circuits operating in the near threshold region consume only two times more energy as compared with the subthreshold region, while remaining energy efficient (ten times less energy than nominal voltage operation). Alternatively, the circuits operating in the near threshold region exhibit ten times longer delay as compared with circuits operating at a nominal voltage. This delay penalty is a hundred to a thousand times lesser than the delay of circuits operating deep within the subthreshold region. Several parts of a microprocessor, however, need to operate at nominal voltages. A 6T SRAM, for example, cannot reliably operate at voltages much lower than the full supply voltage [5]. These high voltage memory cells combined with near threshold logic are often integrated into the same multivoltage domain microprocessor [6], [7].

These techniques require an efficient level shifter that converts the voltage between multivoltage domains [8]. A novel power efficient level shifter topology operating over a wide voltage range is the focus of this brief. The circuit supports voltages ranging from a low voltage near the threshold voltage (~250 mV) to a high voltage domain (for example, 790 mV).

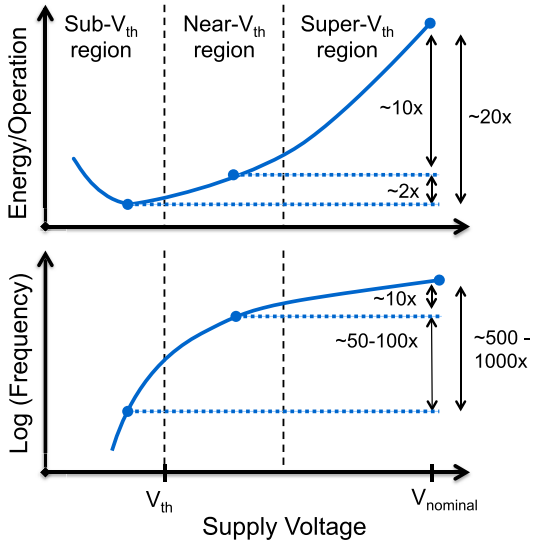

Fig. 1. Energy and delay in different operating regions.

This brief is structured as follows. In Section II, the operation of existing standard and advanced level shifter circuits is reviewed. The proposed wide voltage range level shifter circuit is described in Section III. The simulation environment and results are summarized, respectively, in Sections IV-A and IV-B. Finally, some conclusions are drawn in Section V.

II. Previous Work

Level shifter circuits are typically based on one of three approaches. One approach is based on a differential cascade voltage switch (DCVS) level shifter. This approach is discussed in this section to exemplify the basic principles used by the proposed level shifter. A second approach uses a Wilson current mirror in the amplifying stage [9], [10]. The third approach utilizes a specialized circuit topology [8].

A. Standard Level Shifter

A standard level shifter topology is typically based on a DCVS gate [11]–[14]. A DCVS level shifter circuit is shown in Fig. 2.

The input NMOS transistors are controlled by a low voltage input signal, which is shifted to a high voltage at the output of the level shifter. The DCVS level shifter operates as follows. For the case when $in = 1$ (e.g., 250 mV) and $\overline{in} = 0$ (e.g., 0 V), $out = 1$ (e.g., 790 mV) and $\overline{out} = 0$ (e.g., 0 V). When the input transitions to $in = 0$ (e.g., 0 V) and $\overline{in} = 1$ (e.g., 250 mV), the NR transistor enters the OFF state, while the NL transistor begins to conduct current, discharging node out. The gate of the PL PMOS transistor is, however, connected to node $\overline{out}$, which remains at 0 V, maintaining PL on to resist the NL transistor by simultaneously charging node out. Note that the gate of NR and NL is connected to the low input signal.

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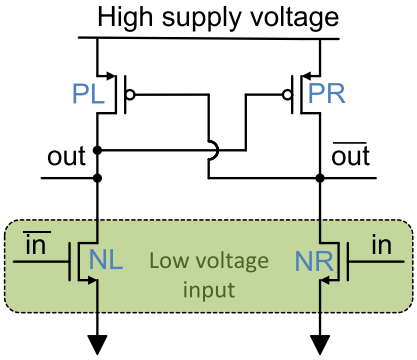

Fig. 2. Standard level shifter based on simple DCVS gate.

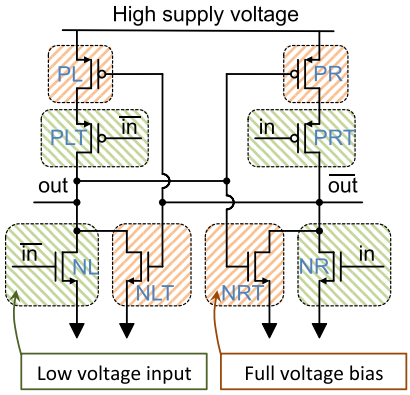

Fig. 3. Advanced level shifter based on DCVS gate with additional logic to improve speed.

These transistors operate near the cutoff region. The gate of PR and PL is connected to the high voltage supply. In this configuration, NL and NR struggle to sink more current than the PMOS pull-up transistors source. If NL sinks greater current than the PMOS pull-up transistor sources, node *out* discharges. The PR transistor toggles from the OFF state to the ON state, and charges node $\overline{out}$ (e.g., 790 mV), which cuts off the pull-up transistor PL, completing the transition.

A common approach to ensure NL and NR sink more current than PL and PR source is to size the NMOS pull-down transistors much larger than the corresponding PMOS pull-up transistors. This method leads to large NMOS transistors with widths typically ten times wider than the PMOS transistors. Section II-B describes a more advanced level shifter circuit that uses smaller NMOS pull-down transistors.

B. Advanced Level Shifter

Additional logic is added to improve the performance and decrease the size of the NMOS pull-down transistors [5]. The additional transistors are NRT, NLT, PRT, and PLT (Fig. 3). This circuit structure improves on the standard level shifter in two ways. First, the NMOS transistors NLT and NRT are biased at a nominal voltage (V_{ddh}); NL and NR can, therefore, be smaller than a standard level shifter. NL and NR should, however, be sufficiently large to force the transition within the differential structure. When the differential input is sufficiently shifted, the significantly stronger NLT and NRT transistors complete the transition. Second, the PMOS transistors, PLT and PRT, are controlled with corresponding input voltage to limit the current flowing through the full voltage pull-up transistors, PL or PR. For high input in ($\overline{in}$), PLT (PRT) is fully ON, providing the desired charging current, while PRT (PLT) limits the current, allowing the NR (NL) and NRT (NLT) NMOS pull-down network to discharge the $\overline{out}$ (out) node.

These changes improve the performance of the level shifter while maintaining the same structure as a standard level shifter. Additional logic allows the NMOS pull-down network to sink more current than the high voltage PMOS pull-up logic sources. This approach is limited, however, by the speed of the additional NMOS pull-down transistors and the current supplied by the PMOS transistors.

A novel level shifter that overcomes this issue of a strong PMOS pull-up network is introduced in this brief. This circuit is discussed in Section III.

III. Proposed Wide Voltage Range Level Shifter for Near Threshold Circuits

The proposed level shifter is based on DCVS, similar to the standard level shifting circuit described in Section II. Rather than increasing the size of the NMOS transistors, however, the proposed circuit dynamically changes the current sourced by the relevant PMOS pull-up transistor (PL/PR) to ensure that the weak NMOS pull-down transistor (NL/NR) sinks more current than the PMOS pull-up (PL/PR) network sources. The proposed low voltage level shifter is shown in Fig. 4.

A. Structure of the Proposed Wide Voltage Range Level Shifter

The novelty of this circuit topology is the feedback loop. The feedback loop consists of a delay element that connects the output node D (high voltage domain) to the input of two multiplexers, MUX_L and MUX_R. The delay element is based on two minimum sized serially connected inverters. These inverters are supplied with a high voltage (790 mV) and receive a high voltage signal D as an input. This delay element does not affect the delay of the proposed level shifter, since the delay element is within the feedback loop that sets up the circuit for the next transition. The MUXs are based on two sets of pass gates, as shown in Fig. 4. The output of MUX_L (high voltage domain) is connected to the gate of the PMOS pull-up transistor PL. When select is high (high voltage domain), the gate of PL is connected to the intermediate voltage V_{ddm}, which temporarily weakens PL. When select is low, the gate of PL is connected to node $\overline{D}$, which preserves the differential operation. Similarly, the output of MUX_R is connected to the gate of the PMOS pull-up transistor PR. When select is high, the gate of PR is connected to node D, which preserves the differential operation. When select is low, the gate of PR is connected to the intermediate voltage V_{ddm}, which temporarily weakens PR. An example of this operation is described in Section III-B.

This configuration eliminates the need for the large NMOS pull-down transistors, NL and NR, because the relevant PMOS pull-up transistor is maintained at a low voltage bias for the upcoming transition. This approach also greatly lowers the transition time as compared with other level shifters.

Symmetric operation of the proposed level shifter is preserved over the maximum operating range. Only minor balancing of the differential branches and the input inverter is required due to the low contention between the pull-up PMOS transistors and the pull-down NMOS transistors. During the falling transition, the input signal propagates through a skewed inverter with a wider PMOS transistor to minimize the charge time of the NL gate. Node D is discharged with low contention from PL, which quickly turns on PR (as opposed to a standard high contention level shifter) to charge the output. Alternatively, the rising input produces a faster transition, since the rising input lacks an inversion delay. This inversion delay is applied during the rising transition by sizing NR smaller than NL (to maintain symmetry). Symmetric operation of the proposed level shifter is exhibited mostly when operating close to the maximum

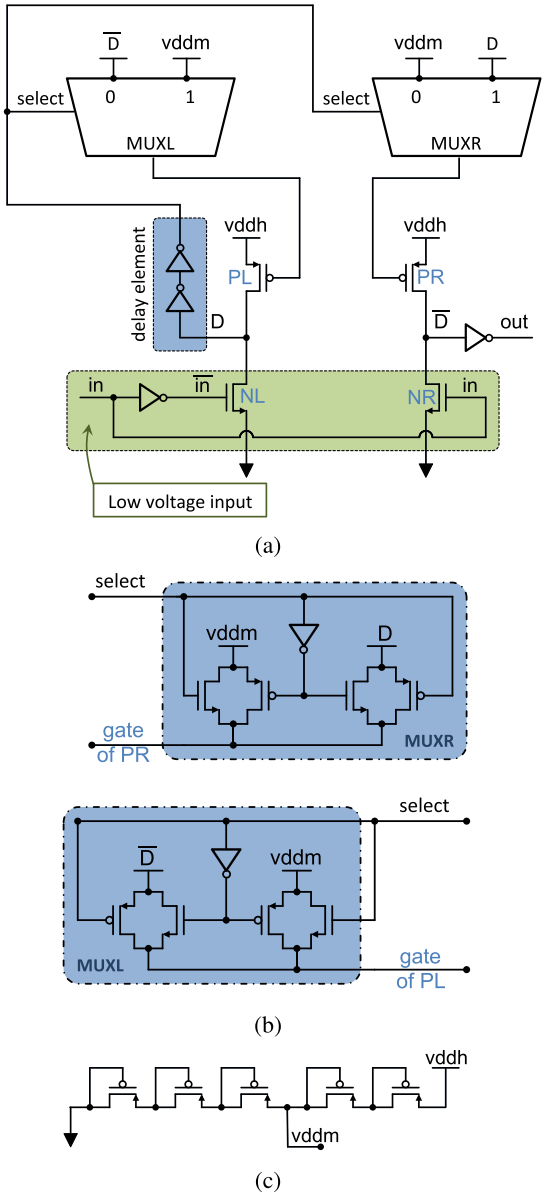

Fig. 4. Structure of the proposed wide voltage range level shifter, including (a) level shifter circuit, (b) internal MUX structures, and (c) intermediate voltage generator.

voltage range. With smaller voltage ranges (e.g., 0.5 to 0.79 V and less), the symmetry degrades. The low contention between PMOS and NMOS transistors also contributes to the higher dynamic energy efficiency of the proposed circuit as compared with the other level shifters.

The intermediate voltage V_{ddm} is generated by a voltage divider, as shown in Fig. 4, which consists of five minimum sized diode connected PMOS transistors. In this configuration, a stable bias voltage of 450 mV is generated to weaken, as needed, the pull-up PMOS transistors.

The area overhead is comparable with the reference level shifters due to the smaller area of the pull-down NMOS transistors. While the addition of the MUXs, delay elements, and intermediate voltage generator introduces additional transistors, this area is similar to the area required by the more complex pull-up network of the reference level shifters.

As described in this section, the proposed level shifter exhibits higher performance as compared with the other level shifters.

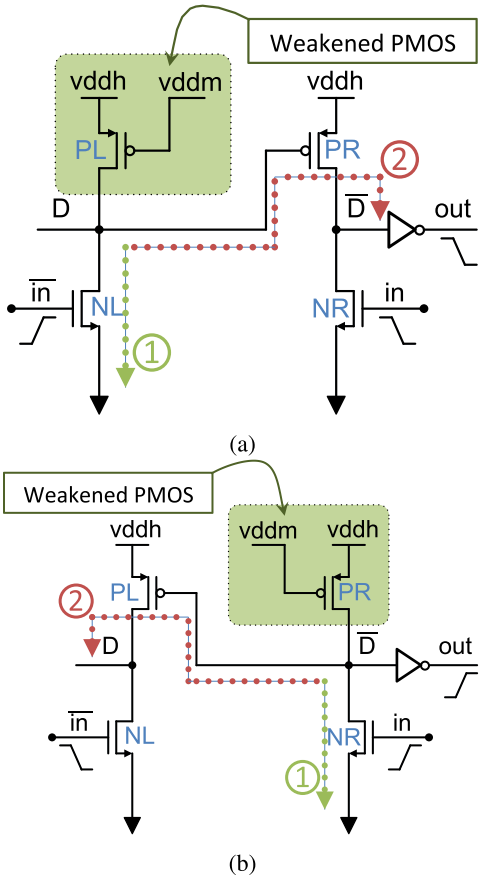

Fig. 5. Operation of proposed level shifter when (a) output is high and the next transition is falling, and (b) output is low and the next transition is rising.

The speed improvement is due to the feedback loop that sets up the circuit for the next transition. The dynamic energy consumption is less due to the low contention between the PMOS and NMOS transistors.

B. Example of Operation

The following example is intended to further clarify the aforementioned circuit operation. Only two possible transition states exist for this level shifter, when the output is high and the next transition is falling, or when the output is low and the next transition is rising.

1) For the first case, when the output is high, the falling transition is shown in Fig. 5. To setup this transition, the gate of PL is connected to the intermediate supply voltage V_{ddm} and the gate of PR is connected to node D. This connection biases PL into the near cutoff region of operation, which degrades the drive strength of PL. Without contention from PL, as shown in the figure, node D discharges through the pull-down network NL. As shown in Fig. 5, node $\overline{D}$ is charged to the full voltage by the pull-up network PR. After a delay, the feedback signal from node D propagates to the select input of MUX_L and MUX_R (the feedback path shown in Fig. 4), which is connected to the gate of PL and PR. This event sets up the state of the level shifter for the next transition.
2) The second case is presented in Fig. 5. In this transition, the level shifter operates in the same way, as described in the first case; however, each operation is mirrored to the other differential branch. Node $\overline{D}$ is discharged through NR, while the current supplied by transistor PR is less due to the intermediate supply voltage V_{ddm} (connected to the gate of PR).

TABLE I
DELAY AND ENERGY OF LEVEL SHIFTER FOR DIFFERENT PROCESS AND TEMPERATURE VARIATIONS

			250 mV → 790 mV				350 mV → 790 mV				500 mV → 790 mV			
			Delay [ps]		Energy [fJ]		Delay [ps]		Energy [fJ]		Delay [ps]		Energy [fJ]	
			Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
Best cases	SF @ 125 °C	Mean	70	74.7	0.94	1.94	25	30.3	1.8	1.0	10.2	20.4	1.6	1.1
		SD	5	8.6	0.049	0.11	1.2	0.9	0.02	0.02	2.4	0.7	0.14	0.02
	TT @ 125 °C	Mean	60.4	59.9	0.9	1.8	22.4	28.7	0.9	1.7	11.3	20.7	1.6	1.1
		SD	3.4	5.1	0.032	0.051	1.2	0.9	0.02	0.02	1.9	0.6	0.12	0.02
	FS @ 125 °C	Mean	55.6	52.4	0.9	1.75	20.4	28.4	1.7	0.9	11.7	20.8	1.7	1.1
		SD	3.4	4.1	0.027	0.042	1.2	1.1	0.02	0.02	0.7	0.7	0.05	0.02
Worst cases	SF @ -30 °C	Mean	400.1	372.8	1.7	0.76	44.3	49.4	1.6	0.9	15.9	27.5	1.4	0.9
		SD	72.2	47	0.15	0.21	3.5	2.6	0.03	0.01	0.8	0.9	0.06	0.01
	TT @ -30 °C	Mean	389.8	369.4	1.5	0.7	41.6	47.1	1.6	0.8	12.3	22.1	1.5	1.0
		SD	71.1	56.9	0.2	0.1	3.2	2.6	0.03	0.01	2.1	0.9	0.09	0.01
	FS @ -30 °C	Mean	567.1	572.4	1.5	0.6	45	51.6	1.5	0.8	13.1	23	1.5	1.0
		SD	127.7	114	0.25	0.16	4.5 7	3.87	0.04	0.01	1.3	1.1	0.07	0.02

IV. EVALUATION OF PROPOSED LEVEL SHIFTER

Evaluation of the proposed level shifter is described in this section. This evaluation demonstrates the high speed and low energy consumption of the proposed level shifter operating over a wide voltage range. In addition, the proposed level shifter is compared with other published level shifters.

A. Simulation Setup

The speed and tolerance to variations at low voltage levels are arguably the most important issues in near threshold circuits [5], [15]. To demonstrate the feasibility of this level shifter for low voltage operation, the proposed circuit is validated against statistical Monte Carlo analysis with 1,000 iterations. The Monte Carlo analysis is applied for a range of standard corners, typical–typical (TT), slow–fast (SF), and fast–slow (FS), at 125 °C and −30 °C. The low voltage input of the level shifter is buffered with a pair of low voltage inverters to isolate the ideal voltage source and to introduce variations. These input buffers also contribute a nonideal input slew equal to 60 ps, on average, for the maximum conversion range. The output of the level shifter is connected to a fan-out load of four, which consists of four identical inverters supplied with a nominal voltage of 0.79 V. The Monte Carlo analysis at different process corners, as reported in Table I, is performed on a prelayout circuit; the simulation is, therefore, supplied with a preextraction netlist. The simulation at nominal operating conditions, as reported in Table II, is performed on a postlayout circuit and includes extracted parasitic impedances.

B. Simulation Results

Extensive Monte Carlo analysis is carried out on the level shifter and includes the intermediate voltage generator as an internal block. The results of the statistical analysis are summarized in Table I. In this table, the delay and energy are described separately for both rise and fall transitions. The delay is the time from the 50% input transition to the 50% output transition. The energy per transition is measured from the 10% input transition to the 90% output transition. For the rising transition, the input of the level shifter changes from 0 to 250, 350, and 500 mV (low voltage domain), while the output, correspondingly, changes from 0 to 790 mV. Similarly, during the falling transition, the input of the level shifter changes from 250, 350, and 500 mV to 0, while the output changes from 790 to 0 mV. Three voltage conversions are reported in Table I, 250 to 790, 350 to 790, and 500 to 790 mV, respectively. In addition, the proposed level shifter can translate input voltages < 200 mV. For these low voltages, however, part of the 1,000 Monte Carlo simulations fail to demonstrate the correct output voltage at the end of the 1-ns period. These failed runs are not included in Table I. The static power dissipation is also not listed, since the proposed level shifter does not dissipate significant short-circuit power, and the intermediate voltage generator leaks an insignificant amount of current due to the large number of serially connected transistors. As an example, two Monte Carlo simulations at a maximum operating temperature of 125 °C for the nominal TT corner and the worst SF corner are presented in Fig. 6. The proposed level shifter exhibits good symmetry between the rise and fall transition times over all corner cases for the maximum voltage conversion range with an average difference of 4% and a worst case difference of 7%. This symmetry degrades for shorter conversion ranges. For the 500 to 790 mV conversion range, the fall time is up to twice longer than the rise time. With respect to the maximum voltage conversion range, the standard deviation is within 12% for the best case corners and within 23% for the worst case corners. With the best case corners, the mean energy per rising transition is close to 0.9 fJ, approximately double the falling transition. The worst case corners exhibit a falling transition energy of 0.7 pJ with an approximate doubling in the rising transition energy.

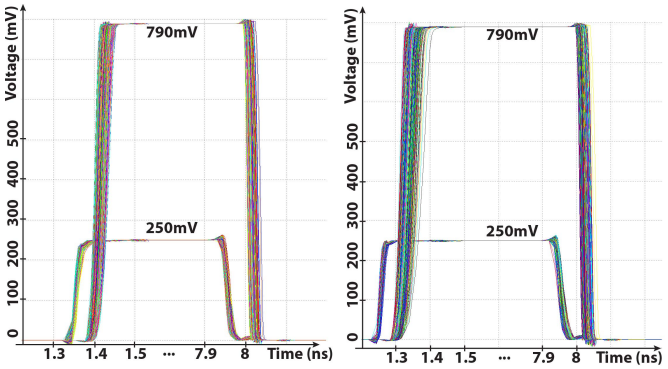

Fig. 6. Input and output waveforms of 1,000 Monte Carlo simulations at (a) nominal TT at the 125 °C corner, and (b) SF at the 125 °C corner.

C. Comparison With Previous Works

The proposed level shifter is compared in Table II to the latest published level converters [11], [13], [16]. To provide a fair comparison, these level shifters are compared in two different ways. In the top part

TABLE II
COMPARISON OF DELAY, ENERGY, AND POWER OF THE LEVEL SHIFTER TO PREVIOUSLY PUBLISHED CIRCUITS

	Process	Delay	Energy per transition	Static power	EDP (normalized)	Voltage range
[10]	90 nm	21.8 ns	74 fJ @ 0.20 V, 1 MHz	6.4 nW	16418	0.18 to 1 V
[12]	90 nm	32 ns	17 fJ @ 0.18 V, 1 MHz	2.5 nW	5537	0.18 to 1 V
[15]	90 nm	16.6 ns	77 fJ @ 0.20 V, 1 MHz	8.7 nW	13009	0.2 to 1 V
[10]*	16 nm FinFET	225 ps	3.21 fJ @ 0.25 V, 2 GHz	548 nW	7	250 to 790 mV
[12]*	16 nm FinFET	2.75 ns	5.22 fJ @ 0.25 V, 0.16 GHz	108 nW	146	250 to 790 mV
[15]*	16 nm FinFET	104.3 ps	2.45 fJ @ 0.25 V, 4.3 GHz	559 nW	3	250 to 790 mV
This work (extracted)**	16 nm FinFET	71.2 ps	1.38 fJ @ 0.25 V, 6.3 GHz	307 nW	1	250 to 790 mV

* replicated in this work to minimize technology biases
** results from simulation with 16 nm FinFET PTM [16] model rather than commercial model

of Table II, the reference converters are presented with the originally published specifications. In the bottom part of Table II, the scaled versions of the same converters are presented. The reference level shifters provide an added dimension to the comparison, demonstrating that the performance gains of the proposed circuit are not only due to the advanced technology. These converters are scaled to 16-nm FinFET technology and analyzed with 16-nm FinFET PTM models [17] under the same conditions as the proposed level shifter. The 16-nm FinFET PTM model does not support triple threshold voltage transistor models, as used in [12] and [15]; the replicated circuits are, therefore, evaluated with dual threshold voltage transistor models. The same W/L ratios, as published in the referenced papers [10], [12], [15], are maintained, while the transistor length is scaled to 16-nm technology. The energy and delay data in Table II are obtained using the same measuring technique, as reported in Section IV-B. The static power is the average of the instantaneous power measured during the idle time after the transition.

The proposed level shifter exhibits enhanced performance as compared with the other published level shifters, as summarized in Table II. In this table, the original version of the referenced circuits presents a tradeoff among delay, energy, and static power. The circuit described in [11] exhibits average speed and energy, while the circuit described in [13] is slower but more energy efficient, and the circuit described in [16] is faster but less energy efficient. When the reference circuits are replicated using a 16-nm FinFET technology, the best reference circuit is the circuit described in [16] (other than static power). As compared with the level shifter published in [16], the proposed level shifter exhibits 42% shorter delay, 45% lower energy consumption, and 48% lower static power dissipation. The proposed level shifter, therefore, provides significant performance advantages as compared with these circuits.

V. CONCLUSION

The proposed level shifter is shown to be suitable for integration in sub-30-nm multivoltage domain microprocessors. Extensive Monte Carlo analysis demonstrates that the proposed circuit reliably level shifts voltages between 250 and 790 mV. The proposed converter, therefore, supports near threshold circuits despite the increased sensitivity to process variations. The converter maintains symmetric rise and fall transition times over the maximum voltage conversion range across different statistical corners (TT, FS, and SF at 125 °C and −30 °C). In addition, the proposed converter is compared with recently published level shifters and exhibits significant improvements in speed, energy, and power efficiency.

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